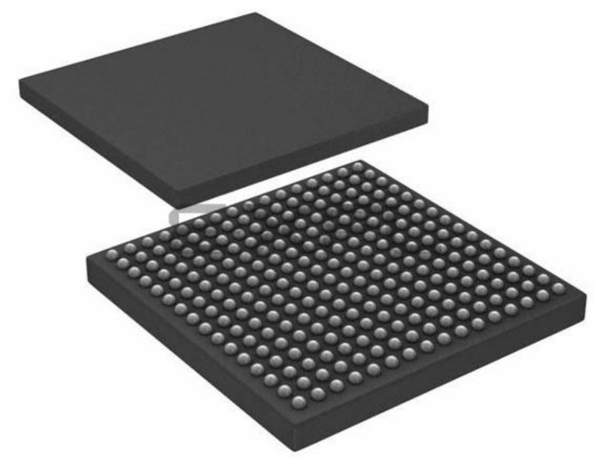

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	27696
Total RAM Bits	1130496
Number of I/O	138
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-FPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl025ts-1vfg256i

2.2 References

The following documents are recommended references:

- *PB0121: IGLOO2 Product Brief*
- *DS0124: IGLOO2 Pin Descriptions*
- *PB0115: SmartFusion2 SoC FPGA Product Brief*
- *DS0115: SmartFusion2 Pin Descriptions*

All product documentation for IGLOO2 and SmartFusion2 is available at:
http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga
http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#overview

2.3 Electrical Specifications

2.3.1 Operating Conditions

The following table lists the stress limits. Stress applied above the specified limit may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table are not implied.

Table 3 • **Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Unit
DC core supply voltage. Must always power this pin.	V_{DD}	–0.3	1.32	V
Power supply for charge pumps (for normal operation and programming). Must always power this pin.	V_{PP}	–0.3	3.63	V
Analog power pad for MDDR PLL	MSS_MDDR_PLL_VDDA	–0.3	3.63	V
Analog power pad for MDDR PLL	HPMS_MDDR_PLL_VDDA	–0.3	3.63	V
Analog power pad for FDDR PLL	FDDR_PLL_VDDA	–0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_MSS_MDDR_VDDA	–0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_HPMS_MDDR_VDDA	–0.3	3.63	V
Analog power pad for PLL0–5	CCC_XX[01]_PLL_VDDA	–0.3	3.63	V
High supply voltage for PLL SerDes[01]	SERDES_[01]_PLL_VDDA	–0.3	3.63	V
Analog power for SerDes[01] PLL lane0 to lane3. This is a 2.5 V SerDes internal PLL supply.	SERDES_[01]_L[0123]_VDDAPLL	–0.3	2.75	V
TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply.	SERDES_[01]_L[0123]_VDDAIO	–0.3	1.32	V
PCIe/PCS power supply	SERDES_[01]_VDD	–0.3	1.32	V
DC FPGA I/O buffer supply voltage for MSIO I/O bank	V_{DDIx}	–0.3	3.63	V
DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks	V_{DDIx}	–0.3	2.75	V
I/O Input voltage for MSIO I/O bank	V_I	–0.3	3.63	V
I/O Input voltage for MSIOD/DDRIO I/O bank	V_I	–0.3	2.75	V
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to V_{PP}.	V_{PPNVM}	–0.3	3.63	V
Storage temperature[1]	T_{STG}	–65	150	°C
Junction temperature	T_J	–55	135	°C

Table 4 • **Recommended Operating Conditions *(continued)***

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
3.3 V DC supply voltage	V_{DDIx}	3.15	3.3	3.45	V	
LVDS differential I/O	V_{DDIx}	2.375	2.5	3.45	V	
B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O	V_{DDIx}	2.375	2.5	2.625	V	
LVPECL differential I/O	V_{DDIx}	3.15	3.3	3.45	V	
Reference voltage supply for FDDR (Bank0) and MDDR (Bank5)	V_{REFx}	0.49 × V_{DDIx}	0.5 × V_{DDIx}	0.51 × V_{DDIx}	V	
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to V_{PP}.	V_{PPNVM}	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range

1. Programming at Industrial temperature range is available only with V_{PP} = 3.3 V.

Note: Power supply ramps must all be strictly monotonic, without plateaus.

Table 5 • **FPGA Operating Limits**

Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Digest Temperature	Digest Cycles	Retention (Biased/ Unbiased)
Commercial	FPGA	Min T_J = 0 °C Max T_J = 85 °C	Min T_J = 0 °C Max T_J = 85 °C	500	Min T_J = 0 °C Max T_J = 85 °C	2000	20 years
Industrial[1]	FPGA	Min T_J = –40 °C Max T_J = 100 °C	Min T_J = –40 °C Max T_J = 100 °C	500	Min T_J = –40 °C Max T_J = 100 °C	2000	20 years

1. Programming at Industrial temperature range is available only with VPP = 3.3 V.

Note: The retention specification is defined as the total number of programing and digest cycles. For example, 20 years of retention after 500 programming cycles.

Note: The digest cycle specification is 2000 digest cycles for every program cycle with a maximum of 500 programming cycles.

Note: If your product qualification requires accelerated programming cycles, see *Microsemi SoC Products Quality and Reliability Report* about recommended methodologies.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIO I/O bank at V_{OH}/V_{OL} Level.

Table 26 • **I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank**

	R(WEAK PULL-UP) at V_{OH} (Ω)		R(WEAK PULL-DOWN) at V_{OL} (Ω)	
V_{DDI} Domain	**Min**	**Max**	**Min**	**Max**
3.3 V	9.9K	17.1K	9.98K	17.5K
2.5 V[1, 2]	10K	17.6K	10.1K	18.4K
1.8 V[1, 2]	10.4K	19.1K	10.4K	20.4K
1.5 V[1, 2]	10.7K	20.4K	10.8K	22.2K
1.2 V[1, 2]	11.3K	23.2K	11.5K	26.7K

1. R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX).
2. R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN).

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIOD I/O bank at V_{OH}/V_{OL} Level.

Table 27 • **I/O Weak Pull-up/Pull-down Resistances for MSIOD I/O Bank**

	R(WEAK PULL-UP) at V_{OH} (Ω)		R(WEAK PULL-DOWN) at V_{OL} (Ω)	
V_{DDI} Domain	**Min**	**Max**	**Min**	**Max**
2.5 V[1, 2]	9.6K	16.6K	9.5K	16.4K
1.8 V[1, 2]	9.7K	17.3K	9.7K	17.1K
1.5 V[1, 2]	9.9K	18K	9.8K	17.6K
1.2 V[1, 2]	10.3K	19.6K	10K	19.1K

1. R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX).
2. R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN).

The following table lists the hysteresis voltage value for schmitt trigger mode input buffers.

Table 28 • **Schmitt Trigger Input Hysteresis**

Input Buffer Configuration	Hysteresis Value (Typical, unless otherwise noted)
3.3 V LVTTL/LVCMOS/ PCI/PCI-X	0.05 × V_{DDI} (worst-case)
2.5 V LVCMOS	0.05 × V_{DDI} (worst-case)
1.8 V LVCMOS	0.1 × V_{DDI} (worst-case)
1.5 V LVCMOS	60 mV
1.2 V LVCMOS	20 mV

Table 82 • LVCMOS 1.2 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

	T_{PY}		T_{PYS}		
On-Die Termination (ODT)	**–1**	**–Std**	**–1**	**–Std**	**Unit**
None	4.154	4.887	4.114	4.84	ns
50	6.918	8.139	6.806	8.008	ns
75	5.613	6.603	5.533	6.509	ns
150	4.716	5.549	4.657	5.479	ns

Table 83 • LVCMOS 1.2 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		
		–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
2 mA	Slow	6.713	7.897	5.362	6.308	6.723	7.909	7.233	8.51	6.375	7.499	ns
	Medium	5.912	6.955	4.616	5.43	5.915	6.959	6.887	8.102	6.009	7.069	ns
	Medium fast	5.5	6.469	4.231	4.978	5.5	6.471	6.672	7.849	5.835	6.865	ns
	Fast	5.462	6.426	4.194	4.935	5.463	6.427	6.646	7.819	5.828	6.857	ns
4 mA	Slow	6.109	7.186	4.708	5.539	6.098	7.174	8.005	9.418	7.033	8.274	ns
	Medium	5.355	6.299	4.034	4.746	5.338	6.28	7.637	8.985	6.672	7.849	ns
	Medium fast	4.953	5.826	3.685	4.336	4.932	5.802	7.44	8.752	6.499	7.646	ns
	Fast	4.911	5.777	3.658	4.303	4.89	5.754	7.427	8.737	6.488	7.632	ns
6 mA	Slow	5.89	6.929	4.506	5.301	5.874	6.911	8.337	9.808	7.315	8.605	ns
	Medium	5.176	6.089	3.862	4.543	5.155	6.065	7.986	9.394	6.943	8.168	ns
	Medium fast	4.792	5.637	3.523	4.145	4.765	5.606	7.808	9.186	6.775	7.97	ns
	Fast	4.754	5.593	3.486	4.101	4.728	5.563	7.777	9.149	6.769	7.963	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 84 • LVCMOS 1.2 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		
		–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
2 mA	Slow	6.746	7.937	7.458	8.774	8.172	9.614	9.867	11.608	8.393	9.874	ns
4 mA	Slow	7.068	8.315	6.678	7.857	7.474	8.793	10.986	12.924	9.043	10.638	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 3.0 V

Table 91 • **PCI/PCIX AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)**

	T_{PY}		T_{PYS}		
On-Die Termination (ODT)	**–1**	**–Std**	**–1**	**–Std**	**Unit**
None	2.229	2.623	2.238	2.633	ns

Table 92 • **PCI/PCIX AC switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)**

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
2.146	2.525	2.043	2.404	2.084	2.452	6.095	7.171	5.558	6.539	ns

2.3.6 Memory Interface and Voltage Referenced I/O Standards

This section describes High-Speed Transceiver Logic (HSTL) memory interface and voltage reference I/O standards.

2.3.6.1 High-Speed Transceiver Logic (HSTL)

The HSTL standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO2 FPGA and SmartFusion2 SoC FPGA devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification (Applicable to DDRIO Bank Only)

Table 93 • **HSTL Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.425	1.5	1.575	V
Termination voltage	V_{TT}	0.698	0.750	0.803	V
Input reference voltage	V_{REF}	0.698	0.750	0.803	V

Table 94 • **HSTL DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high	V_{IH} (DC)	V_{REF} + 0.1	1.575	V
DC input logic low	V_{IL} (DC)	–0.3	V_{REF} – 0.1	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

1. See Table 24, page 22.

Table 118 • **DDR1/SSTL2 Class II Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
	–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	Unit
Single-ended	2.29	2.693	1.988	2.338	1.978	2.326	1.989	2.34	1.979	2.328	ns
Differential	2.418	2.846	2.304	2.711	2.297	2.702	2.131	2.506	2.124	2.499	ns

2.3.6.4 Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double date rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 119 • **SSTL18 DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.71	1.8	1.89	V
Termination voltage	V_{TT}	0.838	0.900	0.964	V
Input reference voltage	V_{REF}	0.838	0.900	0.964	V

Table 120 • **SSTL18 DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high	V_{IH} (DC)	V_{REF} + 0.125	1.89	V
DC input logic low	V_{IL} (DC)	–0.3	V_{REF} – 0.125	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

1. See Table 24, page 22.

Table 121 • **SSTL18 DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
SSTL18 Class I (DDR2 Reduced Drive)				
DC output logic high	V_{OH}	V_{TT} + 0.603		V
DC output logic low	V_{OL}		V_{TT}– 0.603	V
Output minimum source DC current (DDRIO I/O bank only)	I_{OH} at V_{OH}	6.5		mA
Output minimum sink current (DDRIO I/O bank only)	I_{OL} at V_{OL}	–6.5		mA
SSTL18 Class II (DDR2 Full Drive)[1]				
DC output logic high	V_{OH}	V_{TT} + 0.603		V
DC output logic low	V_{OL}		V_{TT}– 0.603	V
Output minimum source DC current (DDRIO I/O bank only)	I_{OH} at V_{OH}	13.4		mA
Output minimum sink current (DDRIO I/O bank only)	I_{OL} at V_{OL}	–13.4		mA

1. To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.

Table 168 • **LVDS25 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.554	3.004	ns
100	2.549	2.999	ns

Table 169 • **LVDS25 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
2.136	2.513	2.416	2.842	2.402	2.825	2.423	2.85	2.409	2.833	ns

Table 170 • **LVDS25 Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)**

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
	–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
No pre-emphasis	1.61	1.893	1.749	2.058	1.735	2.041	1.897	2.231	1.866	2.195	ns
Min pre-emphasis	1.527	1.796	1.757	2.067	1.744	2.052	1.905	2.241	1.876	2.207	ns
Med pre-emphasis	1.496	1.76	1.765	2.077	1.751	2.06	1.914	2.252	1.884	2.216	ns

LVDS33 AC Switching Characteristics

Table 171 • **LVDS33 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

	T_{PY}		
On Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.572	3.025	ns
100	2.569	3.023	ns

Table 172 • **LVDS33 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
1.942	2.284	1.98	2.33	1.97	2.318	1.953	2.298	1.96	2.307	ns

Table 191 • **M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.495	2.934	ns
100	2.495	2.935	ns

Table 192 • **M-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
2.258	2.656	2.348	2.762	2.334	2.746	2.123	2.497	2.125	2.5	ns

2.3.7.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

Mini-LVDS Minimum and Maximum Input and Output Levels

Table 193 • **Mini-LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V

Table 194 • **Mini-LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC Input voltage	V_I	0	2.925	V

Table 195 • **Mini-LVDS DC Output Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 196 • **Mini-LVDS DC Differential Voltage Specification**

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing	V_{OD}	300	600	mV
Output common mode voltage	V_{OCM}	1	1.4	V
Input common mode voltage	V_{ICM}	0.3	1.2	V
Input differential voltage	V_{ID}	100	600	mV

Table 197 • **Mini-LVDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	520	Mbps	AC loading: 2 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	700	Mbps	AC loading: 2 pF / 100 Ω differential load

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V.

Table 210 • **RSDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.855	3.359	ns
100	2.85	3.353	ns

Table 211 • **RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.602	3.061	ns
100	2.597	3.055	ns

Table 212 • **RSDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
2.097	2.467	2.303	2.709	2.291	2.695	1.961	2.307	1.947	2.29	ns

Table 213 • **RSDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
	–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
No pre-emphasis	1.614	1.899	1.559	1.834	1.55	1.823	1.59	1.87	1.575	1.852	ns
Min pre-emphasis	1.604	1.887	1.742	2.05	1.728	2.032	1.889	2.222	1.858	2.185	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

2.3.7.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

Minimum and Maximum Input and Output Levels (Applicable to MSIO I/O Bank Only)

Table 214 • **LVPECL Recommended DC Operating Conditions**

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

The following table lists the input data register propagation delays in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 219 • **Input Data Register Propagation Delays**

Parameter	Symbol	Measuring Nodes (from, to)[1]	–1	–Std	Unit
Bypass delay of the input register	T_{IBYP}	F, G	0.353	0.415	ns
Clock-to-Q of the input register	T_{ICLKQ}	E, G	0.16	0.188	ns
Data setup time for the input register	T_{ISUD}	A, E	0.357	0.421	ns
Data hold time for the input register	T_{IHD}	A, E	0	0	ns
Enable setup time for the input register	T_{ISUE}	B, E	0.46	0.542	ns
Enable hold time for the input register	T_{IHE}	B, E	0	0	ns
Synchronous load setup time for the input register	T_{ISUSL}	D, E	0.46	0.542	ns
Synchronous load hold time for the input register	T_{IHSL}	D, E	0	0	ns
Asynchronous clear-to-Q of the input register (ADn=1)	T_{IALN2Q}	C, G	0.625	0.735	ns
Asynchronous preset-to-Q of the input register (ADn=0)		C, G	0.587	0.69	ns
Asynchronous load removal time for the input register	$T_{IREMALN}$	C, E	0	0	ns
Asynchronous load recovery time for the input register	$T_{IRECALN}$	C, E	0.074	0.087	ns
Asynchronous load minimum pulse width for the input register	T_{IWALN}	C, C	0.304	0.357	ns
Clock minimum pulse width high for the input register	$T_{ICKMPWH}$	E, E	0.075	0.088	ns
Clock minimum pulse width low for the input register	$T_{ICKMPWL}$	E, E	0.159	0.187	ns

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

Table 221 • Input DDR Propagation Delays (continued)

Symbol	Description	Measuring Nodes (from, to)	–1	–Std	Unit
$T_{DDRIWAL}$	Asynchronous load minimum pulse width for input DDR	F, F	0.304	0.357	ns
$T_{DDRICKMPWH}$	Clock minimum pulse width high for input DDR	B, B	0.075	0.088	ns
$T_{DDRICKMPWL}$	Clock minimum pulse width low for input DDR	B, B	0.159	0.187	ns

2.3.9.4 Output DDR Module

Figure 12 • **Output DDR Module**

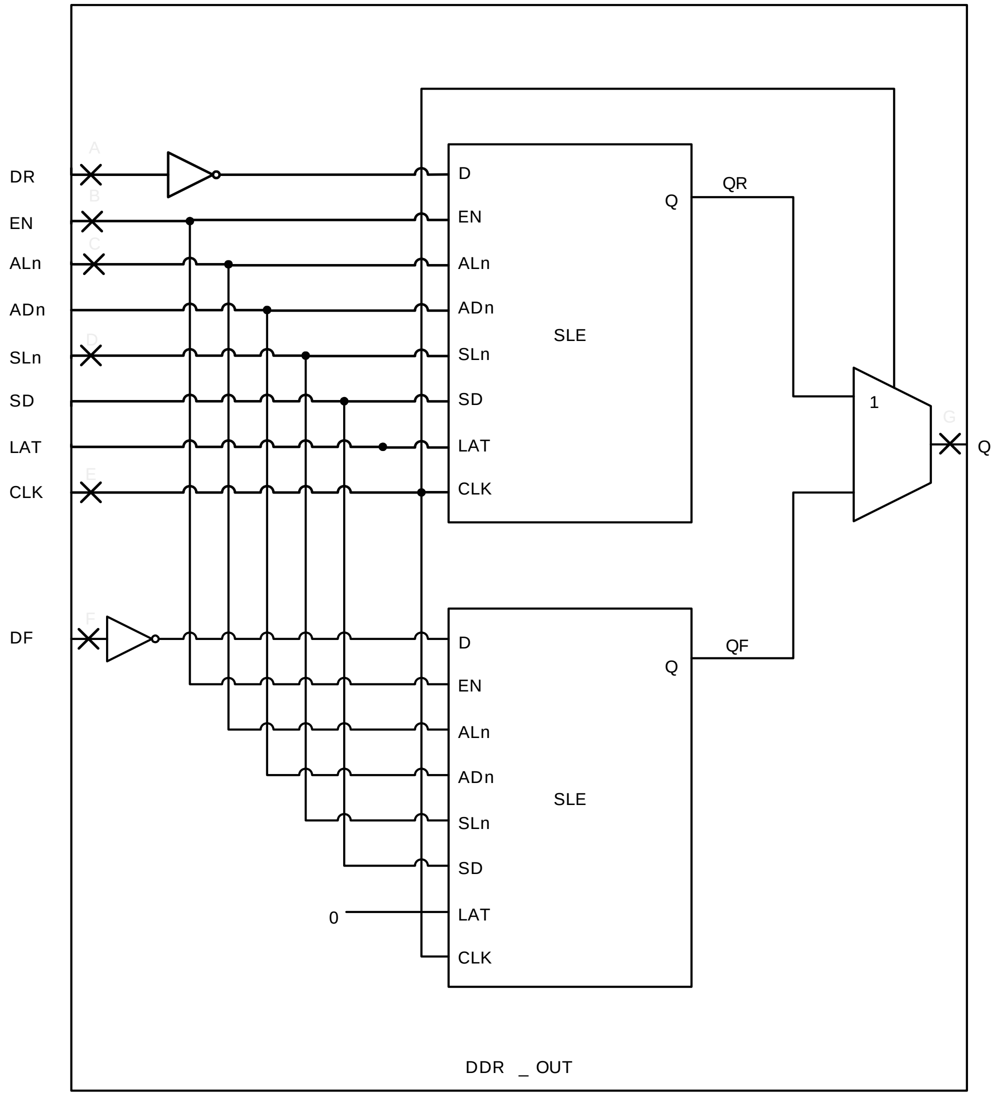


Table 239 • **µSRAM (RAM128x9) in 128 × 9 Mode *(continued)***

Parameter	Symbol	–1 Min	–1 Max	–Std Min	–Std Max	Unit
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.982	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the µSRAM in 128 × 8 mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 240 • **µSRAM (RAM128x8) in 128 × 8 Mode**

Parameter	Symbol	–1 Min	–1 Max	–Std Min	–Std Max	Unit
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns

The following table lists the µSRAM in 256 × 4 mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 241 • **µSRAM (RAM256x4) in 256 × 4 Mode**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.27		0.31	ns
Read access time without pipeline register			1.75		2.06	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.931		2.272		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.121		0.142		ns
Read address hold time in asynchronous mode		–0.65		–0.76		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.77		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.09		2.46	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.02		–0.03		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.83		0.98	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.101		0.118		ns
Write input data hold time	T_{DINCHD}	0.137		0.161		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns

Table 245 • **JTAG Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	137536	39	4	Sec
010	274816	78	9	Sec
025	274816	78	9	Sec
050	278528	84	8	Sec
060	268480	76	8	Sec
090	544496	154	15	Sec
150	544496	155	15	Sec

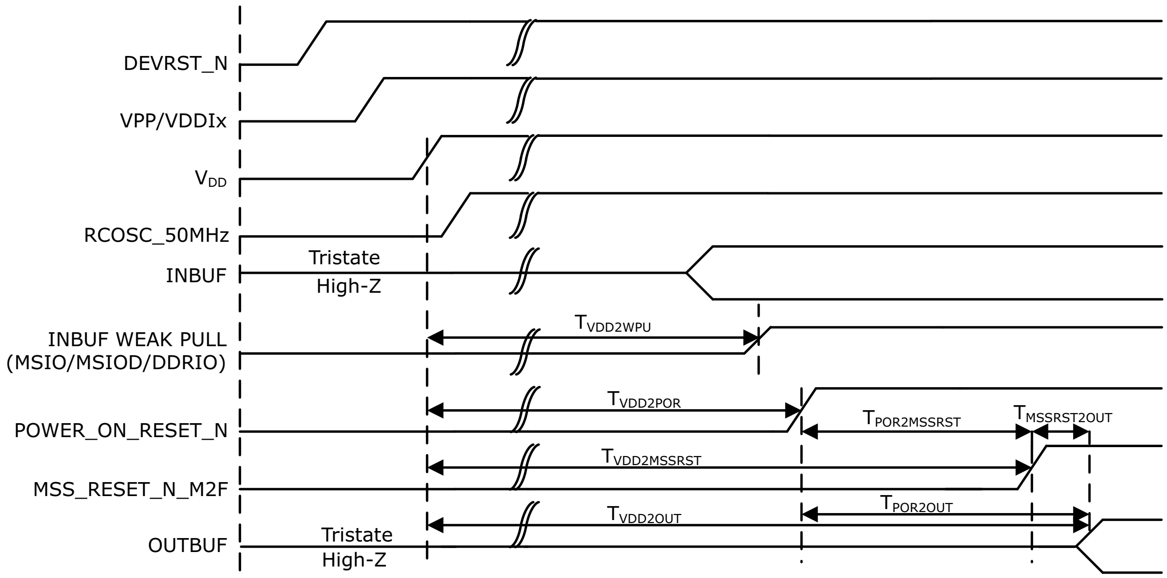
Table 246 • **JTAG Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	439296	59	11	Sec
010	842688	107	20	Sec
025	1497408	120	35	Sec
050	2695168	162	59	Sec
060	2686464	158	70	Sec
090	4190208	266	147	Sec
150	6682768	316	231	Sec

Table 247 • **2 Step IAP Programming (Fabric Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	302672	4	17	6	Sec
010	568784	7	23	12	Sec
025	1223504	14	33	23	Sec
050	2424832	29	52	40	Sec
060	2418896	39	61	50	Sec
090	3645968	60	84	73	Sec
150	6139184	100	132	120	Sec

Figure 17 • **Power-up to Functional Timing Diagram for SmartFusion2**



The following table lists the IGLOO2 power-up to functional times in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 289 • **Power-up to Functional Times for IGLOO2**

				Maximum Power-up to Functional Time for IGLOO2 (uS)						
Symbol	**From**	**To**	**Description**	**005**	**010**	**025**	**050**	**060**	**090**	**150**
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	114	114	113	114	114	114
$T_{VDD2OUT}$	V_{DD}	Output available at I/O	V_{DD} at its minimum threshold level to output	2587	2600	2607	2558	2591	2600	2699
$T_{VDD2POR}$	V_{DD}	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	2474	2486	2493	2445	2477	2486	2585
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide*.

2.3.30 SerDes Electrical and Timing AC and DC Characteristics

PCIe is a high-speed, packet-based, point-to-point, low-pin-count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block.

The following table lists the transmitter parameters in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 296 • **Transmitter Parameters**

Symbol	Description	Min	Max	Unit
VTX-DIFF-PP	Differential swing (2.5 Gbps, 5.0 Gbps)	0.8	1.2	V
VTX-CM-AC-P	Output common mode voltage (2.5 Gbps)		20	mV
VTX-CM-AC-PP	Output common mode voltage (5.0 Gbps)		100	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%, 2.5 Gbps)	0.125		UI
	Rise and fall time (20% to 80%, 5.0 Gbps)	0.15		UI
ZTX-DIFF-DC	Output impedance–differential	80	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SerDes block (2.5 Gbps)		500 ps + 2 UI	ps
	Lane-to-lane TX skew within a SerDes block (5.0 Gbps)		500 ps + 4 UI	ps
RLTX-DIFF	Return loss differential mode (2.5 Gbps)	–10		dB
	Return loss differential mode (5.0 Gbps) 0.05 GHz to 1.25 GHz	–10		dB
	1.25 GHz to 2.5 GHz	–8		dB
RLTX-CM	Return loss common mode (2.5 Gbps, 5.0 Gbps)	–6		dB
TX-LOCK-RST	Transmit PLL lock time from reset		10	µs
VTX-AMP	100 mV setting	90	150	mV
	400 mV setting	320	480	mV
	800 mV setting	660	940	mV
	1200 mV setting	950	1400	mV

The following table lists the receiver pa in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 297 • **Receiver Parameters**

Symbol	Description	Min	Typ	Max	Unit
VRX-IN-PP-CC	Differential input peak-to-peak sensitivity (2.5 Gbps)	0.238		1.2	V
	Differential input peak-to-peak sensitivity (2.5 Gbps, de-emphasized)	0.219		1.2	V
	Differential input peak-to-peak sensitivity (5.0 Gbps)	0.300		1.2	V
	Differential input peak-to-peak sensitivity (5.0 Gbps, de-emphasized)	0.300		1.2	V
VRX-CM-AC-P	Input common mode range (AC coupled)			150	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset			15	µs
RLRX-DIFF	Return loss differential mode (2.5 Gbps)	–10			dB
	Return loss differential mode (5.0 Gbps) 0.05 GHz to 1.25 GHz	–10			dB
	1.25 GHz to 2.5 GHz	–8			dB
RLRX-CM	Return loss common mode (2.5 Gbps, 5.0 Gbps)	–6			dB
RX-CID[1]	CID limit PCIe Gen1/2			200	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65		175	mV

1. AC-coupled, BER = e^{-12}, using synchronous clock.

Table 298 • **SerDes Protocol Compliance**

Protocol	Maximum Data Rate (Gbps)	–1	–Std
PCIe Gen 1	2.5	Yes	Yes
PCIe Gen 2	5.0	Yes	
XAUI	3.125	Yes	
Generic EPCS	3.2	Yes	
Generic EPCS	2.5	Yes	Yes

2.3.31.2 SmartFusion2 Inter-Integrated Circuit (I^2C) Characteristics

This section describes the DC and switching of the I^2C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, see Figure 21, page 125.

The following table lists the I^2C characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V

Table 303 • **I2C Characteristics**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input low voltage	V_{IL}	–0.3		0.8	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive.
Input high voltage	V_{IH}	2		3.45	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive.
Hysteresis of schmitt triggered inputs for V_{DDI} > 2 V	V_{HYS}	0.05 × V_{DDI}			V	See Table 28, page 23 for more information.
Input current high	I_{IL}			10	µA	See Single-Ended I/O Standards, page 24 for more information.
Input current low	I_{IH}			10	µA	See Single-Ended I/O Standards, page 24 for more information.
Input rise time	T_{ir}			1000	ns	Standard mode
				300	ns	Fast mode
Input fall time	T_{if}			300	ns	Standard mode
				300	ns	Fast mode
Maximum output voltage low (open drain) at 3 mA sink current for V_{DDI} > 2 V	V_{OL}			0.4	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive.
Pin capacitance	Cin			10	pF	V_{IN} = 0, f = 1.0 MHz
Output fall time from VIHMin to VILMax[1]	t_{OF}[1]		21.04		ns	V_{IHmin} to V_{ILMax}, CLOAD = 400 pF
			5.556		ns	V_{IHmin} to V_{ILMax}, CLOAD = 100 pF
Output rise time from VILMax to VIHMin[1]	t_{OR}[1]		19.887		ns	V_{ILMax} to V_{IHmin}, CLOAD = 400 pF
			5.218		ns	V_{ILMax} to V_{IHmin}, CLOAD = 100 pF
Output buffer maximum pull-down resistance[2, 3]	$R_{pull-up}$[2,3]			50	Ω	
Output buffer maximum pull-up resistance[2, 4]	$R_{pull-down}$[2,4]			131.25	Ω	

Table 310 • **SPI Characteristics for All Devices *(continued)***

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp2	SPI_[0|1]_CLK minimum pulse width high					
	SPI_[0|1]_CLK = PCLK/2	6			ns	
	SPI_[0|1]_CLK = PCLK/4	12.05			ns	
	SPI_[0|1]_CLK = PCLK/8	24.1			ns	
	SPI_[0|1]_CLK = PCLK/16	0.05			µs	
	SPI_[0|1]_CLK = PCLK/32	0.095			µs	
	SPI_[0|1]_CLK = PCLK/64	0.195			µs	
	SPI_[0|1]_CLK = PCLK/128	0.385			µs	
sp3	SPI_[0|1]_CLK minimum pulse width low					
	SPI_[0|1]_CLK = PCLK/2	6			ns	
	SPI_[0|1]_CLK = PCLK/4	12.05			ns	
	SPI_[0|1]_CLK = PCLK/8	24.1			ns	
	SPI_[0|1]_CLK = PCLK/16	0.05			µs	
	SPI_[0|1]_CLK = PCLK/32	0.095			µs	
	SPI_[0|1]_CLK = PCLK/64	0.195			µs	
	SPI_[0|1]_CLK = PCLK/128	0.385			µs	
sp4	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS rise time (10%–90%)[1]		2.77		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
sp5	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS fall time (10%–90%)[1]		2.906		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0|1]_DI setup time[2]	12			ns	
sp9m	SPI_[0|1]_DI hold time[2]	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0|1]_DI setup time[2]	2			ns	
sp9s	SPI_[0|1]_DI hold time[2]	7			ns	