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### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	27696
Total RAM Bits	1130496
Number of I/O	180
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	325-TFBGA, FCBGA
Supplier Device Package	325-FCBGA (11x11)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2gl025ts-fcs325i">https://www.e-xfl.com/product-detail/microchip-technology/m2gl025ts-fcs325i</a>

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## 2.2 References

The following documents are recommended references:

- *PB0121: IGLOO2 Product Brief*
- *DS0124: IGLOO2 Pin Descriptions*
- *PB0115: SmartFusion2 SoC FPGA Product Brief*
- *DS0115: SmartFusion2 Pin Descriptions*

All product documentation for IGLOO2 and SmartFusion2 is available at:

<http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga>

<http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#overview>

## 2.3 Electrical Specifications

### 2.3.1 Operating Conditions

The following table lists the stress limits. Stress applied above the specified limit may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table are not implied.

**Table 3 • Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Unit
DC core supply voltage. Must always power this pin.	$V_{DD}$	-0.3	1.32	V
Power supply for charge pumps (for normal operation and programming). Must always power this pin.	$V_{PP}$	-0.3	3.63	V
Analog power pad for MDDR PLL	MSS_MDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	HPMS_MDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for FDDR PLL	FDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_MSS_MDDR_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_HPMS_MDDR_VDDA	-0.3	3.63	V
Analog power pad for PLL0-5	CCC_XX[01]_PLL_VDDA	-0.3	3.63	V
High supply voltage for PLL SerDes[01]	SERDES_[01]_PLL_VDDA	-0.3	3.63	V
Analog power for SerDes[01] PLL lane0 to lane3. This is a 2.5 V SerDes internal PLL supply.	SERDES_[01]_L[0123]_VDDAPLL	-0.3	2.75	V
TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply.	SERDES_[01]_L[0123]_VDDAIO	-0.3	1.32	V
PCIe/PCS power supply	SERDES_[01]_VDD	-0.3	1.32	V
DC FPGA I/O buffer supply voltage for MSIO I/O bank	$V_{DDIx}$	-0.3	3.63	V
DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks	$V_{DDIx}$	-0.3	2.75	V
I/O Input voltage for MSIO I/O bank	$V_I$	-0.3	3.63	V
I/O Input voltage for MSIOD/DDRIO I/O bank	$V_I$	-0.3	2.75	V
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to $V_{PP}$ .	$V_{PPNVM}$	-0.3	3.63	V
Storage temperature <sup>1</sup>	$T_{STG}$	-65	150	°C
Junction temperature	$T_J$	-55	135	°C

**Figure 1 • High Temperature Data Retention (HTR)****2.3.1.1 Overshoot/Undershoot Limits**

For AC signals, the input signal may undershoot during transitions to  $-1.0$  V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to  $V_{CC1} + 1.0$  V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

**Note:** The above specifications do not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant with the PCI standard including the PCI overshoot/undershoot specifications.

**2.3.1.2 Thermal Characteristics**

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ1 through EQ3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

**Table 9 • Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices (continued)**

Device	Still Air	1.0 m/s	2.5 m/s	$\theta_{JB}$	$\theta_{JC}$	Unit
	$\theta_{JA}$					
<b>150</b>						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W
FCS536	15.01	12.06	10.76	3.69	1.55	°C/W
FCV484	16.21	13.11	11.84	6.73	0.10	°C/W

### 2.3.1.2.1 Theta-JA

Junction-to-ambient thermal resistance ( $\theta_{JA}$ ) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in the actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package with another.

The maximum power dissipation allowed is calculated using EQ4.

$$\text{Maximum power allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100 °C. EQ5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where:

$$\theta_{JA} = 14.7 \text{ °C/W (taken from Table 9, page 10).}$$

$$T_A = 85 \text{ °C}$$

$$\text{Maximum power allowed} = \frac{100 \text{ °C} - 85 \text{ °C}}{14.7 \text{ °C/W}} = 1.088 \text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink may be attached to the top of the case, or the airflow inside the system must be increased.

### 2.3.1.2.2 Theta-JB

Junction-to-board thermal resistance ( $\theta_{JB}$ ) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from the junction to the board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

### 2.3.1.2.3 Theta-JC

Junction-to-case thermal resistance ( $\theta_{JC}$ ) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable to packages used with external heat sinks. Constant temperature is applied to the surface, which acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

### 2.3.1.3 ESD Performance

See *RT0001: Microsemi Corporation - SoC Products Reliability Report* for information about ESD.

**Table 34 • LVTTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	1.4	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**Table 35 • LVTTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank**

Output Drive Selection	$V_{OH}$ (V)	$V_{OL}$ (V)	IOH (at $V_{OH}$ ) mA	IOL (at $V_{OL}$ ) mA
2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	$V_{DDI} - 0.4$	0.4	4	4
8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA	$V_{DDI} - 0.4$	0.4	16	16
20 mA	$V_{DDI} - 0.4$	0.4	20	20

**Note:** For a detailed I/V curve, use the corresponding IBIS models: [www.microsemi.com/soc/download/ibis/default.aspx](http://www.microsemi.com/soc/download/ibis/default.aspx).

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 3.0\text{ V}$

**Table 36 • LVTTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
	-1	-Std	-1	-Std	
None	2.262	2.663	2.289	2.695	ns

**Table 37 • LVTTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.192	3.755	3.47	4.083	2.969	3.494	1.856	2.183	3.337	3.926	ns
4 mA	Slow	2.331	2.742	2.673	3.145	2.526	2.973	3.034	3.569	4.451	5.236	ns
8 mA	Slow	2.135	2.511	2.33	2.741	2.297	2.703	4.532	5.331	4.825	5.676	ns
12 mA	Slow	2.052	2.414	2.107	2.479	2.162	2.544	5.75	6.764	5.445	6.406	ns
16 mA	Slow	2.062	2.425	2.072	2.438	2.145	2.525	5.993	7.05	5.625	6.618	ns
20 mA	Slow	2.148	2.527	1.999	2.353	2.088	2.458	6.262	7.367	5.876	6.913	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 53 • LVCMOS 1.8 V AC Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	Rodt_cal	75, 60, 50, 33, 25, 20	$\Omega$

**Table 54 • LVCMOS 1.8 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V <sub>TRIP</sub>	0.9	V
Resistance for enable path (T <sub>ZH</sub> , T <sub>ZL</sub> , T <sub>HZ</sub> , T <sub>LZ</sub> )	R <sub>ENT</sub>	2k	$\Omega$
Capacitive loading for enable path (T <sub>ZH</sub> , T <sub>ZL</sub> , T <sub>HZ</sub> , T <sub>LZ</sub> )	C <sub>ENT</sub>	5	pF
Capacitive loading for data path (T <sub>DP</sub> )	C <sub>LOAD</sub>	5	pF

**Table 55 • LVCMOS 1.8 V Transmitter Drive Strength Specifications**

Output Drive Selection			V <sub>OH</sub> (V)	V <sub>OL</sub> (V)	IOH (at V <sub>OH</sub> )	IOL (at V <sub>OL</sub> )
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max	mA	mA
2 mA	2 mA	2 mA	V <sub>DDI</sub> - 0.45	0.45	2	2
4 mA	4 mA	4 mA	V <sub>DDI</sub> - 0.45	0.45	4	4
6 mA	6 mA	6 mA	V <sub>DDI</sub> - 0.45	0.45	6	6
8 mA	8 mA	8 mA	V <sub>DDI</sub> - 0.45	0.45	8	8
10 mA	10 mA	10 mA	V <sub>DDI</sub> - 0.45	0.45	10	10
12 mA		12 mA	V <sub>DDI</sub> - 0.45	0.45	12	12
		16 mA <sup>1</sup>	V <sub>DDI</sub> - 0.45	0.45	16	16

1. 16 mA drive strengths, all slews, meets LPDDR JEDEC electrical compliance.

### AC Switching Characteristics

Worst commercial-case conditions: T<sub>J</sub> = 85 °C, V<sub>DD</sub> = 1.14 V, V<sub>DDI</sub> = 1.71 V

**Table 56 • LVCMOS 1.8 V Receiver Characteristics (Input Buffers)**

	On-Die Termination (ODT)	T <sub>py</sub>		T <sub>pys</sub>		Unit
		-1	-Std	-1	-Std	
<b>LVCMOS 1.8 V (for DDRIO I/O bank with Fixed Codes)</b>	None	1.968	2.315	2.099	2.47	ns
	None	2.898	3.411	2.883	3.393	ns
	50	3.05	3.59	3.044	3.583	ns
	75	2.999	3.53	2.987	3.516	ns
<b>LVCMOS 1.8 V (for MSIO I/O bank)</b>	150	2.947	3.469	2.933	3.452	ns
	None	2.611	3.071	2.598	3.057	ns
	50	2.775	3.264	2.775	3.265	ns
	75	2.72	3.2	2.712	3.19	ns
<b>LVCMOS 1.8 V (for MSIOD I/O bank)</b>	150	2.666	3.137	2.655	3.123	ns

**Table 57 • LVCMOS 1.8 V Transmitter Characteristics for DDRIO I/O Bank with Fixed Code (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub> <sup>1</sup>		T <sub>LZ</sub> <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	Medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	Medium fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	Fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4 mA	Slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	Medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	Medium fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	Fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6 mA	Slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	Medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	Medium fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	Fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns
8 mA	Slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns
	Medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	Medium fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	Fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10 mA	Slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	Medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	Medium fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	Fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12 mA	Slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	Medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	Medium fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	Fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16 mA	Slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	Medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	Medium fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	Fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.



### 2.3.6.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 139 • LPDDR DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max
Supply voltage	$V_{DDI}$	1.71	1.8	1.89
Termination voltage	$V_{TT}$	0.838	0.900	0.964
Input reference voltage	$V_{REF}$	0.838	0.900	0.964

**Table 140 • LPDDR DC Input Voltage Specification**

Parameter	Symbol	Min	Max
DC input logic high	$V_{IH}$ (DC)	$0.7 \times V_{DDI}$	1.89
DC input logic low	$V_{IL}$ (DC)	-0.3	$0.3 \times V_{DDI}$
Input current high <sup>1</sup>	$I_{IH}$ (DC)		
Input current low <sup>1</sup>	$I_{IL}$ (DC)		

1. See Table 24, page 22.

**Table 141 • LPDDR DC Output Voltage Specification Reduced Drive**

Parameter	Symbol	Min	Max
DC output logic high	$V_{OH}$	$0.9 \times V_{DDI}$	
DC output logic low	$V_{OL}$		$0.1 \times V_{DDI}$
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	0.1	
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-0.1	

**Table 142 • LPDDR DC Output Voltage Specification Full Drive<sup>1</sup>**

Parameter	Symbol	Min	Max
DC output logic high	$V_{OH}$	$0.9 \times V_{DDI}$	
DC output logic low	$V_{OL}$		$0.1 \times V_{DDI}$
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	0.1	
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-0.1	

1. To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.

**Table 143 • LPDDR DC Differential Voltage Specification**

Parameter	Symbol	Min
DC input differential voltage	$V_{ID}$ (DC)	$0.4 \times V_{DDI}$

**Table 168 • LVDS25 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.554	3.004	ns
100	2.549	2.999	ns

**Table 169 • LVDS25 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.136	2.513	2.416	2.842	2.402	2.825	2.423	2.85	2.409	2.833	ns

**Table 170 • LVDS25 Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
No pre-emphasis	1.61	1.893	1.749	2.058	1.735	2.041	1.897	2.231	1.866	2.195	ns
Min pre-emphasis	1.527	1.796	1.757	2.067	1.744	2.052	1.905	2.241	1.876	2.207	ns
Med pre-emphasis	1.496	1.76	1.765	2.077	1.751	2.06	1.914	2.252	1.884	2.216	ns

**LVDS33 AC Switching Characteristics**
**Table 171 • LVDS33 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

On Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.572	3.025	ns
100	2.569	3.023	ns

**Table 172 • LVDS33 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
1.942	2.284	1.98	2.33	1.97	2.318	1.953	2.298	1.96	2.307	ns

**Table 191 • M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

On-Die Termination (ODT)	T <sub>PY</sub>		Unit
	-1	-Std	
None	2.495	2.934	ns
100	2.495	2.935	ns

**Table 192 • M-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub>		T <sub>LZ</sub>		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.258	2.656	2.348	2.762	2.334	2.746	2.123	2.497	2.125	2.5	ns

### 2.3.7.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

#### Mini-LVDS Minimum and Maximum Input and Output Levels

**Table 193 • Mini-LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>DDI</sub>	2.375	2.5	2.625	V

**Table 194 • Mini-LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	V <sub>I</sub>	0	2.925	V

**Table 195 • Mini-LVDS DC Output Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V <sub>OH</sub>	1.25	1.425	1.6	V
DC output logic low	V <sub>OL</sub>	0.9	1.075	1.25	V

**Table 196 • Mini-LVDS DC Differential Voltage Specification**

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing	V <sub>OD</sub>	300	600	mV
Output common mode voltage	V <sub>OCM</sub>	1	1.4	V
Input common mode voltage	V <sub>ICM</sub>	0.3	1.2	V
Input differential voltage	V <sub>ID</sub>	100	600	mV

**Table 197 • Mini-LVDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D <sub>MAX</sub>	520	Mbps	AC loading: 2 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank)	D <sub>MAX</sub>	700	Mbps	AC loading: 2 pF / 100 Ω differential load

### 2.3.7.5 RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

#### Minimum and Maximum Input and Output Levels

**Table 203 • RSDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V

**Table 204 • RSDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	$V_I$	0	2.925	V

**Table 205 • RSDS DC Output Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	$V_{OH}$	1.25	1.425	1.6	V
DC output logic low	$V_{OL}$	0.9	1.075	1.25	V

**Table 206 • RSDS Differential Voltage Specification**

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing	$V_{OD}$	100	600	mV
Output common mode voltage	$V_{OCM}$	0.5	1.5	V
Input common mode voltage	$V_{ICM}$	0.3	1.5	V
Input differential voltage	$V_{ID}$	100	600	mV

**Table 207 • RSDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	520	Mbps	AC loading: 2 pF / 100 $\Omega$ differential load
Maximum data rate (for MSIOD I/O bank)	$D_{MAX}$	700	Mbps	AC loading: 2 pF / 100 $\Omega$ differential load

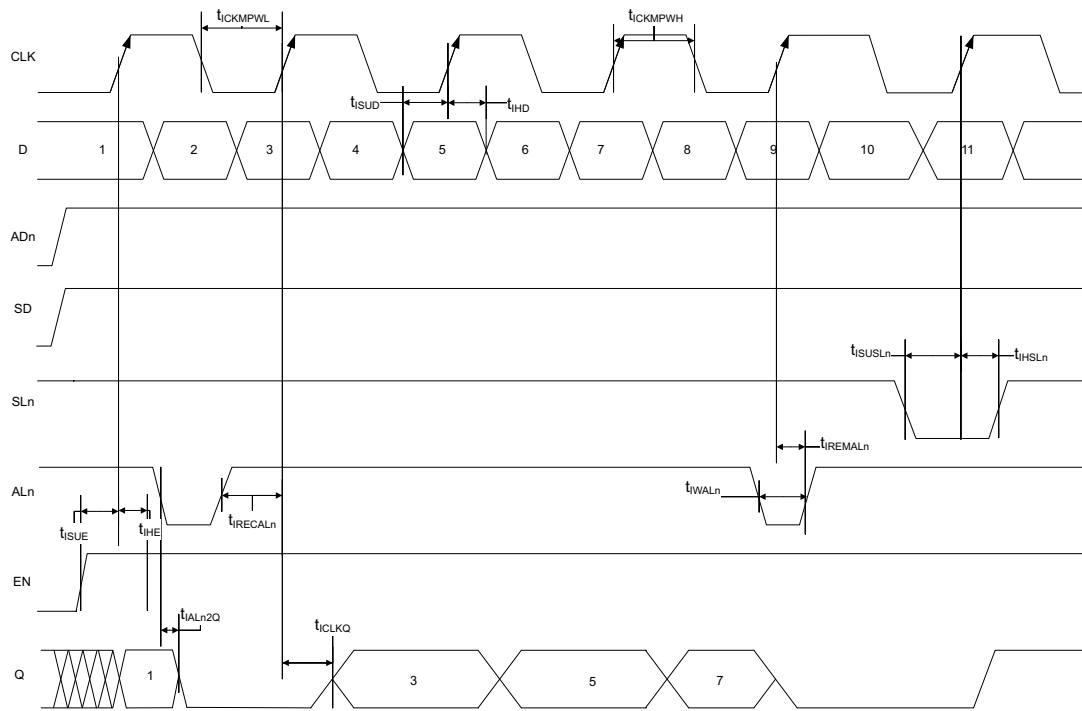
**Table 208 • RSDS AC Impedance Specifications**

Parameter	Symbol	Typ	Unit
Termination resistance	$R_T$	100	$\Omega$

**Table 209 • RSDS AC Test Parameter Specifications**

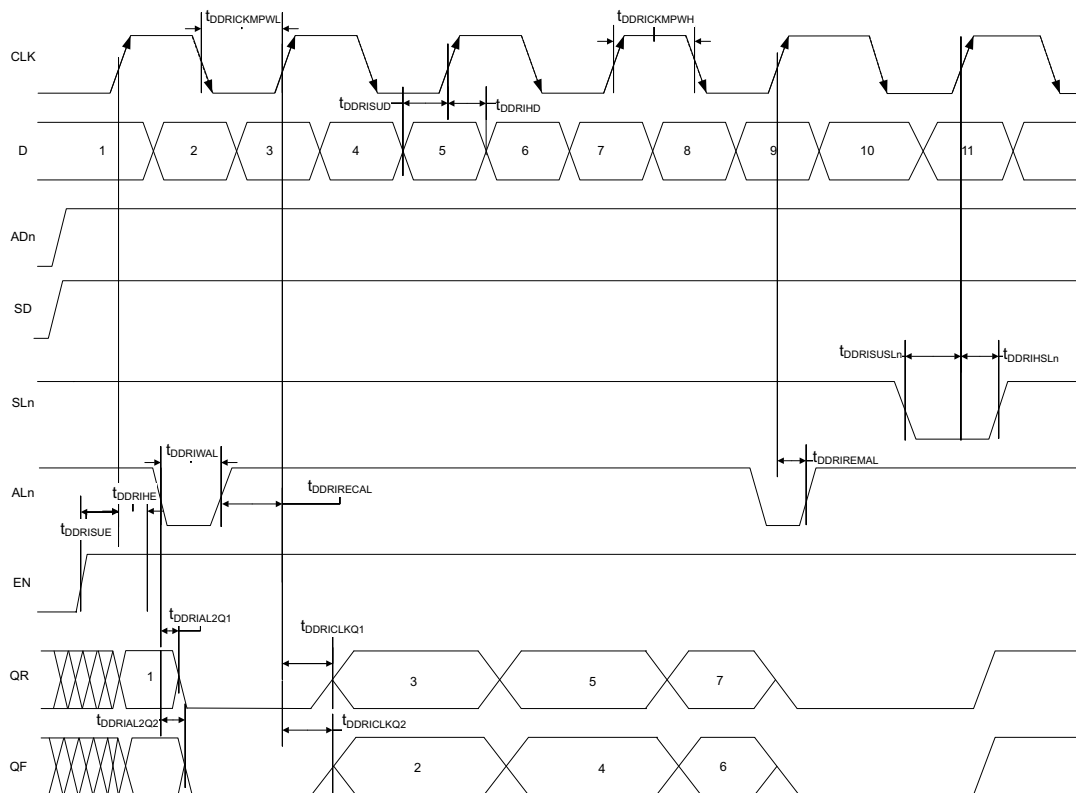
Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	Cross point	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF

**Figure 7 • I/O Register Input Timing Diagram**



### 2.3.9.2 Input DDR Timing Diagram

Figure 11 • Input DDR Timing Diagram



### 2.3.9.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 221 • Input DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDRICKLQ1}$	Clock-to-Out Out_QR for input DDR	B, C	0.16	0.188	ns
$T_{DDRICKLQ2}$	Clock-to-Out Out_QF for input DDR	B, D	0.166	0.195	ns
$T_{DDRISUD}$	Data setup for input DDR	A, B	0.357	0.421	ns
$T_{DDRIHD}$	Data hold for input DDR	A, B	0	0	ns
$T_{DDRISUE}$	Enable setup for input DDR	E, B	0.46	0.542	ns
$T_{DDRIHE}$	Enable hold for input DDR	E, B	0	0	ns
$T_{DDRISUSL}$	Synchronous load setup for input DDR	G, B	0.46	0.542	ns
$T_{DDRIHSL}$	Synchronous load hold for input DDR	G, B	0	0	ns
$T_{DDRIR2Q1}$	Asynchronous load-to-out QR for input DDR	F, C	0.587	0.69	ns
$T_{DDRIR2Q2}$	Asynchronous load-to-out QF for input DDR	F, D	0.541	0.636	ns
$T_{DDRIREMAL}$	Asynchronous load removal time for input DDR	F, B	0	0	ns
$T_{DDRIRECAL}$	Asynchronous load recovery time for input DDR	F, B	0.074	0.087	ns

### 2.3.10.2 Timing Characteristics

The following table lists the combinatorial cell propagation delays in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

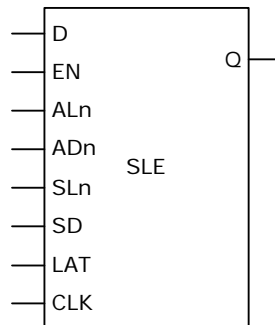
**Table 223 • Combinatorial Cell Propagation Delays**

Combinatorial Cell	Equation	Symbol	-1	-Std	Unit
INV	$Y = !A$	$T_{PD}$	0.1	0.118	ns
AND2	$Y = A \cdot B$	$T_{PD}$	0.164	0.193	ns
NAND2	$Y = !(A \cdot B)$	$T_{PD}$	0.147	0.173	ns
OR2	$Y = A + B$	$T_{PD}$	0.164	0.193	ns
NOR2	$Y = !(A + B)$	$T_{PD}$	0.147	0.173	ns
XOR2	$Y = A \oplus B$	$T_{PD}$	0.164	0.193	ns
XOR3	$Y = A \oplus B \oplus C$	$T_{PD}$	0.225	0.265	ns
AND3	$Y = A \cdot B \cdot C$	$T_{PD}$	0.209	0.246	ns
AND4	$Y = A \cdot B \cdot C \cdot D$	$T_{PD}$	0.287	0.338	ns

### 2.3.10.3 Sequential Module

IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

**Figure 15 • Sequential Module**



The following table lists the 010 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 229 • 010 Device Global Resource**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	$T_{RCKL}$	0.626	0.669	0.627	0.668	ns
Input high delay for global clock	$T_{RCKH}$	1.112	1.182	1.308	1.393	ns
Maximum skew for global clock	$T_{RCKSW}$		0.07		0.085	ns

The following table lists the 005 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 230 • 005 Device Global Resource**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	$T_{RCKL}$	0.625	0.66	0.628	0.66	ns
Input high delay for global clock	$T_{RCKH}$	1.126	1.187	1.325	1.397	ns
Maximum skew for global clock	$T_{RCKSW}$		0.061		0.072	ns

## 2.3.12 FPGA Fabric SRAM

See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for more information.

### 2.3.12.1 FPGA Fabric Large SRAM (LSRAM)

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 1K × 18 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 231 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Clock period	$T_{CY}$	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	$T_{PLCY}$	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register				0.334	0.393	ns
Read access time without pipeline register	$T_{CLK2Q}$			2.273	2.674	ns
Access time with feed-through write timing				1.529	1.799	ns
Address setup time	$T_{ADDRSU}$	0.441		0.519		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.341		0.401		ns
Data hold time	$T_{DHD}$	0.107		0.126		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns



**Table 237 •  $\mu$ SRAM (RAM64x18) in 64 × 18 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.026		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

The following table lists the  $\mu$ SRAM in 64 × 16 mode in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 238 •  $\mu$ SRAM (RAM64x16) in 64 × 16 Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	$T_{CY}$	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	$T_{PLCY}$	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	$T_{CLK2Q}$		0.266		0.313	ns
Read access time without pipeline register				1.677		1.973
Read address setup time in synchronous mode	$T_{ADDRSU}$	0.301		0.354		ns
Read address setup time in asynchronous mode			1.856		2.184	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.091		0.107		ns
Read address hold time in asynchronous mode			-0.778		-0.915	
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHD}$	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	$T_{RSTREM}$	-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)			0.046		0.054	
Read asynchronous reset recovery time (pipelined clock)	$T_{RSTREC}$	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)			0.236		0.278	
Read asynchronous reset to output propagation delay (with pipelined register enabled)	$T_{R2Q}$		0.835		0.983	ns
Read synchronous reset setup time	$T_{SRSTSU}$	0.271		0.319		ns

**Table 251 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only) (continued)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
150	544496	10	158	15	Sec

**Table 252 • SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	9	61	11	Sec
010	842688	15	107	21	Sec
025	1497408	26	121	35	Sec
050	2695168	43	141	55	Sec
060	2686464	48	143	60	Sec
090	4190208	75	244	91	Sec
150	6682768	117	296	141	Sec

**Table 253 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	Unit
	100 kHz	25 MHz	12.5 MHz	
005	47	27	28	Sec
010	77	35	35	Sec
025	150	42	41	Sec
050	33 <sup>1</sup>	Not Supported	Not Supported	Sec
060	291	83	82	Sec
090	427	109	108	Sec
150	708	157	160	Sec

1. Auto Programming in 050 device is done through SC\_SPI, and SPI CLK is set to 6.25 MHz.

**Table 254 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	Unit
	100 kHz	25 MHz	12.5 MHz	
005	41	48	49	Sec
010	86	87	87	Sec
025	87	85	86	Sec
050	85	Not Supported	Not Supported	Sec
060	78	86	86	Sec
090	154	162	162	Sec

## 2.3.24 Power-up to Functional Times

The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 288 • Power-up to Functional Times for SmartFusion2**

Symbol	From	To	Description	Maximum Power-up to Functional Time for SmartFusion2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	647	500	531	483	474	524	647
$T_{POR2MSSRST}$	POWER_ON_RESET_N	MSS_RESE T_N_M2F	Fabric to MSS	644	497	528	480	468	518	641
$T_{MSSRST2OUT}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.6	3.6	3.6	3.4	4.9	4.8	4.8
$T_{VDD2OUT}$	$V_{DD}$	Output available at I/O	$V_{DD}$ at its minimum threshold level to output	3096	2975	3012	2959	2869	2992	3225
$T_{VDD2POR}$	$V_{DD}$	POWER_ON_RESET_N	$V_{DD}$ at its minimum threshold level to fabric	2476	2487	2496	2486	2406	2563	2602
$T_{VDD2MSSRST}$	$V_{DD}$	MSS_RESE T_N_M2F	$V_{DD}$ at its minimum threshold level to MSS	3093	2972	3008	2956	2864	2987	3220
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

**Note:** For more information about power-up times, see *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

**Table 293 • Flash\*Freeze Entry and Exit Times (continued)**

Parameter	Symbol	Entry/Exit Timing			Unit	Conditions
		FCLK = 100MHz		FCLK = 3 MHz		
		005, 010, 025, 060, 090, and 150	050	All Devices		
Exit time with respect to the fabric PLL lock <sup>1</sup>	TFF_EXIT	1.5	1.5	1.5	ms	eNVM and MSS/HPMS PLL = ON during F*F
		1.5	1.5	1.5	ms	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit
Exit time with respect to the fabric buffer output	TFF_EXIT	21	15	21	µs	eNVM and MSS/HPMS PLL = ON during F*F
		65	55	65	µs	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit

1. PLL Lock Delay set to 1024 cycles (default).

### 2.3.28 DDR Memory Interface Characteristics

The following table lists the DDR memory interface characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 294 • DDR Memory Interface Characteristics**

Standard	Supported Data Rate		Unit
	Min	Max	
DDR3	667	667	Mbps
DDR2	667	667	Mbps
LPDDR	50	400	Mbps

### 2.3.29 SFP Transceiver Characteristics

IGLOO2 and SmartFusion2 SerDes complies with small form-factor pluggable (SFP) requirements as specified in SFP INF-80741. The following table provides the electrical characteristics.

The following table lists the SFP transceiver electrical characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 295 • SFP Transceiver Electrical Characteristics**

Pin	Direction	Differential Peak-Peak Voltage		Unit
		Min	Max	
RD+/- <sup>1</sup>	Output	1600	2400	mV
TD+/- <sup>2</sup>	Input	350	2400	mV

1. Based on default SerDes transmitter settings for PCIe Gen1. Lower amplitudes are available through programming changes to TX\_AMP setting.
2. Based on Input Voltage Common-Mode (VICM) = 0 V. Requires AC Coupling.

**Table 310 • SPI Characteristics for All Devices (continued)**

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp2	SPI_[0 1]_CLK minimum pulse width high					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			µs	
	SPI_[0 1]_CLK = PCLK/32	0.095			µs	
	SPI_[0 1]_CLK = PCLK/64	0.195			µs	
	SPI_[0 1]_CLK = PCLK/128	0.385			µs	
sp3	SPI_[0 1]_CLK minimum pulse width low					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			µs	
	SPI_[0 1]_CLK = PCLK/32	0.095			µs	
	SPI_[0 1]_CLK = PCLK/64	0.195			µs	
	SPI_[0 1]_CLK = PCLK/128	0.385			µs	
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) <sup>1</sup>		2.77		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%–90%) <sup>1</sup>		2.906		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0 1]_DI setup time <sup>2</sup>	12			ns	
sp9m	SPI_[0 1]_DI hold time <sup>2</sup>	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0 1]_DI setup time <sup>2</sup>	2			ns	
sp9s	SPI_[0 1]_DI hold time <sup>2</sup>	7			ns	