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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	27696
Total RAM Bits	1130496
Number of I/O	207
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-LFBGA
Supplier Device Package	400-VFBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2gl025ts-vf400">https://www.e-xfl.com/product-detail/microchip-technology/m2gl025ts-vf400</a>

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The following table lists the embedded operating flash limits.

**Table 6 • Embedded Operating Flash Limits**

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Commercial	Embedded flash	Min $T_J = 0\text{ }^\circ\text{C}$ Max $T_J = 85\text{ }^\circ\text{C}$	Min $T_J = 0\text{ }^\circ\text{C}$ Max $T_J = 85\text{ }^\circ\text{C}$	< 1000 cycles per page, up to two million cycles per eNVM array	20 years
				< 10000 cycles per page, up to 20 million cycles per eNVM array	10 years
Industrial	Embedded flash	Min $T_J = -40\text{ }^\circ\text{C}$ Max $T_J = 100\text{ }^\circ\text{C}$	Min $T_J = -40\text{ }^\circ\text{C}$ Max $T_J = 100\text{ }^\circ\text{C}$	< 1000 cycles per page, up to two million cycles per eNVM array	20 years
				< 10000 cycles per page, up to 20 million cycles per eNVM array	10 years

**Note:** If your product qualification requires accelerated programming cycles, see [Microsemi SoC Products Quality and Reliability Report](#) about recommended methodologies.

**Table 7 • Device Storage Temperature and Retention**

Product Grade	Storage Temperature (Tstg)	Retention
Commercial	Min $T_J = 0\text{ }^\circ\text{C}$ Max $T_J = 85\text{ }^\circ\text{C}$	20 years
Industrial	Min $T_J = -40\text{ }^\circ\text{C}$ Max $T_J = 100\text{ }^\circ\text{C}$	20 years

**Table 8 • High Temperature Data Retention (HTR) Lifetime**

$T_J$ (C)	HTR Lifetime <sup>1</sup> (yrs)
90	20.5
95	20.5
100	20.5
105	17.0
110	15.0
115	13.0
120	11.5
125	10.0
130	8.0
135	6.0
140	4.5
145	3.0
150	1.5

1. HTR Lifetime is the period during which a verify failure is not expected due to flash leakage.

## 2.3.2 Power Consumption

The following sections describe the power consumptions of the devices.

### 2.3.2.1 Quiescent Supply Current

**Table 10 • Quiescent Supply Current Characteristics**

Power Supplies/Blocks	Modes and Configurations	
	Non-Flash*Freeze	Flash*Freeze
FPGA Core	On	Off
V <sub>DD</sub> /SERDES_[01]_VDD <sup>1</sup>	On	On
V <sub>PP</sub> /V <sub>PPNVM</sub>	On	On
HPMS_MDDR_PLL_VDDA/FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA/PLL0_PLL1_HPMS_MDDR_VDD A	0 V	0 V
SERDES_[01]_PLL_VDDA <sup>2</sup>	0 V	0 V
SERDES_[01]_L[0123]_VDDAPLL/VDD_2V5 <sup>2</sup>	On	On
SERDES_[01]_L[0123]_VDDAIIO <sup>2</sup>	On	On
V <sub>DDIx</sub> <sup>3, 4</sup>	On	On
V <sub>REFx</sub>	On	On
MSSDDR CLK	32 kHz	32 kHz
RAM	On	Sleep state
System controller	50 MHz	50 MHz
50 MHz oscillator (enable/disable)	Enable	Disabled
1 MHz oscillator (enable/disable)	Disabled	Disabled
Crystal oscillator (enable/disable)	Disabled	Disabled

1. SERDES\_[01]\_VDD Power Supply is shorted to V<sub>DD</sub>.
2. SerDes and DDR blocks to be unused.
3. V<sub>DDIx</sub> has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate V<sub>DDI</sub> bank supplies. For details on bank power supplies, see "Recommendation for Unused Bank Supplies" table in the *AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.
4. No Differential (that is to say, LVDS) I/Os or ODT attributes to be used.

**Table 11 • SmartFusion2 and IGLOO2 Quiescent Supply Current (V<sub>DD</sub> = 1.2 V) – Typical Process**

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC1	Non-Flash*Freeze	6.2	6.9	8.9	13.1	15.3	15.4	27.5	mA	Typical (T <sub>J</sub> = 25 °C)
		24.0	28.4	40.6	67.8	80.6	81.4	144.7	mA	Commercial (T <sub>J</sub> = 85 °C)
		35.2	41.9	60.5	102.1	121.4	122.6	219.1	mA	Industrial (T <sub>J</sub> = 100 °C)

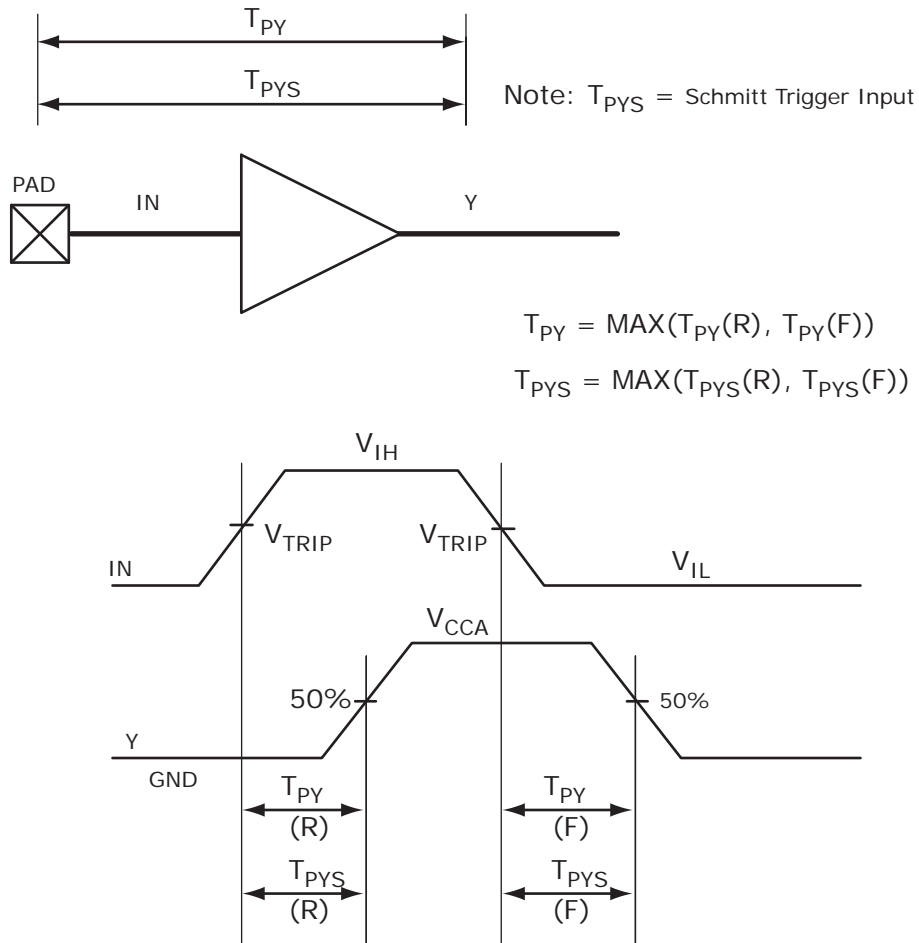
## 2.3.5 User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the I/Os section of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

### 2.3.5.1 Input Buffer and AC Loading

The following figure shows the input buffer and AC loading.

**Figure 3 • Input Buffer AC Loading**



## 2.3.5.6 Single-Ended I/O Standards

### 2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

### 2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 29 • LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	3.15	3.3	3.45	V

**Table 30 • LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}$ (DC)	2.0	3.45	V
DC input logic low	$V_{IL}$ (DC)	-0.3	0.8	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 31 • LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC output logic high <sup>1</sup>	$V_{OH}$	$V_{DDI} - 0.4$		V
DC output logic low <sup>1</sup>	$V_{OL}$		0.4	V

1. The  $V_{OH}/V_{OL}$  test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

**Table 32 • LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC output logic high	$V_{OH}$	2.4		V
DC output logic low	$V_{OL}$		0.4	V

**Table 33 • LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	600	Mbps	AC loading: 17 pF load, maximum drive/slew

**Table 34 • LVTTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	1.4	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**Table 35 • LVTTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank**

Output Drive Selection	$V_{OH}$ (V)	$V_{OL}$ (V)	IOH (at $V_{OH}$ ) mA	IOL (at $V_{OL}$ ) mA
2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	$V_{DDI} - 0.4$	0.4	4	4
8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA	$V_{DDI} - 0.4$	0.4	16	16
20 mA	$V_{DDI} - 0.4$	0.4	20	20

**Note:** For a detailed I/V curve, use the corresponding IBIS models:  
[www.microsemi.com/soc/download/ibis/default.aspx](http://www.microsemi.com/soc/download/ibis/default.aspx).

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 3.0\text{ V}$

**Table 36 • LVTTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
	-1	-Std	-1	-Std	
None	2.262	2.663	2.289	2.695	ns

**Table 37 • LVTTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.192	3.755	3.47	4.083	2.969	3.494	1.856	2.183	3.337	3.926	ns
4 mA	Slow	2.331	2.742	2.673	3.145	2.526	2.973	3.034	3.569	4.451	5.236	ns
8 mA	Slow	2.135	2.511	2.33	2.741	2.297	2.703	4.532	5.331	4.825	5.676	ns
12 mA	Slow	2.052	2.414	2.107	2.479	2.162	2.544	5.75	6.764	5.445	6.406	ns
16 mA	Slow	2.062	2.425	2.072	2.438	2.145	2.525	5.993	7.05	5.625	6.618	ns
20 mA	Slow	2.148	2.527	1.999	2.353	2.088	2.458	6.262	7.367	5.876	6.913	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.



### 2.3.5.7 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs that are in compliance with the JEDEC specification JESD8-5A.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 38 • LVCMOS 2.5 V DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V

**Table 39 • LVCMOS 2.5 V DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	$V_{IH}$ (DC)	1.7	2.625	V
DC input logic high (for MSIO I/O bank)	$V_{IH}$ (DC)	1.7	3.45	V
DC input logic low	$V_{IL}$ (DC)	-0.3	0.7	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See [Table 24](#), page 22.

**Table 40 • LVCMOS 2.5 V DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	$V_{OH}$ <sup>1</sup>	$V_{DDI} - 0.4$	-	V
DC output logic low	$V_{OL}$ <sup>2</sup>		0.4	V

1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

**Table 41 • LVCMOS 2.5 V AC Minimum and Maximum Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	$D_{MAX}$	400	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	410	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	$D_{MAX}$	420	Mbps	AC loading: 17 pF load, maximum drive/slew

**Table 42 • LVCMOS 2.5 V AC Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	Rodt_cal	75, 60, 50, 33, 25, 20	$\Omega$

**Table 82 • LVCMOS 1.2 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
	-1	-Std	-1	-Std	
None	4.154	4.887	4.114	4.84	ns
50	6.918	8.139	6.806	8.008	ns
75	5.613	6.603	5.533	6.509	ns
150	4.716	5.549	4.657	5.479	ns

**Table 83 • LVCMOS 1.2 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	6.713	7.897	5.362	6.308	6.723	7.909	7.233	8.51	6.375	7.499	ns
	Medium	5.912	6.955	4.616	5.43	5.915	6.959	6.887	8.102	6.009	7.069	ns
	Medium fast	5.5	6.469	4.231	4.978	5.5	6.471	6.672	7.849	5.835	6.865	ns
	Fast	5.462	6.426	4.194	4.935	5.463	6.427	6.646	7.819	5.828	6.857	ns
4 mA	Slow	6.109	7.186	4.708	5.539	6.098	7.174	8.005	9.418	7.033	8.274	ns
	Medium	5.355	6.299	4.034	4.746	5.338	6.28	7.637	8.985	6.672	7.849	ns
	Medium fast	4.953	5.826	3.685	4.336	4.932	5.802	7.44	8.752	6.499	7.646	ns
	Fast	4.911	5.777	3.658	4.303	4.89	5.754	7.427	8.737	6.488	7.632	ns
6 mA	Slow	5.89	6.929	4.506	5.301	5.874	6.911	8.337	9.808	7.315	8.605	ns
	Medium	5.176	6.089	3.862	4.543	5.155	6.065	7.986	9.394	6.943	8.168	ns
	Medium fast	4.792	5.637	3.523	4.145	4.765	5.606	7.808	9.186	6.775	7.97	ns
	Fast	4.754	5.593	3.486	4.101	4.728	5.563	7.777	9.149	6.769	7.963	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 84 • LVCMOS 1.2 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	6.746	7.937	7.458	8.774	8.172	9.614	9.867	11.608	8.393	9.874	ns
4 mA	Slow	7.068	8.315	6.678	7.857	7.474	8.793	10.986	12.924	9.043	10.638	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.7.5 RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

#### Minimum and Maximum Input and Output Levels

**Table 203 • RSDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V

**Table 204 • RSDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	$V_I$	0	2.925	V

**Table 205 • RSDS DC Output Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	$V_{OH}$	1.25	1.425	1.6	V
DC output logic low	$V_{OL}$	0.9	1.075	1.25	V

**Table 206 • RSDS Differential Voltage Specification**

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing	$V_{OD}$	100	600	mV
Output common mode voltage	$V_{OCM}$	0.5	1.5	V
Input common mode voltage	$V_{ICM}$	0.3	1.5	V
Input differential voltage	$V_{ID}$	100	600	mV

**Table 207 • RSDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	520	Mbps	AC loading: 2 pF / 100 $\Omega$ differential load
Maximum data rate (for MSIOD I/O bank)	$D_{MAX}$	700	Mbps	AC loading: 2 pF / 100 $\Omega$ differential load

**Table 208 • RSDS AC Impedance Specifications**

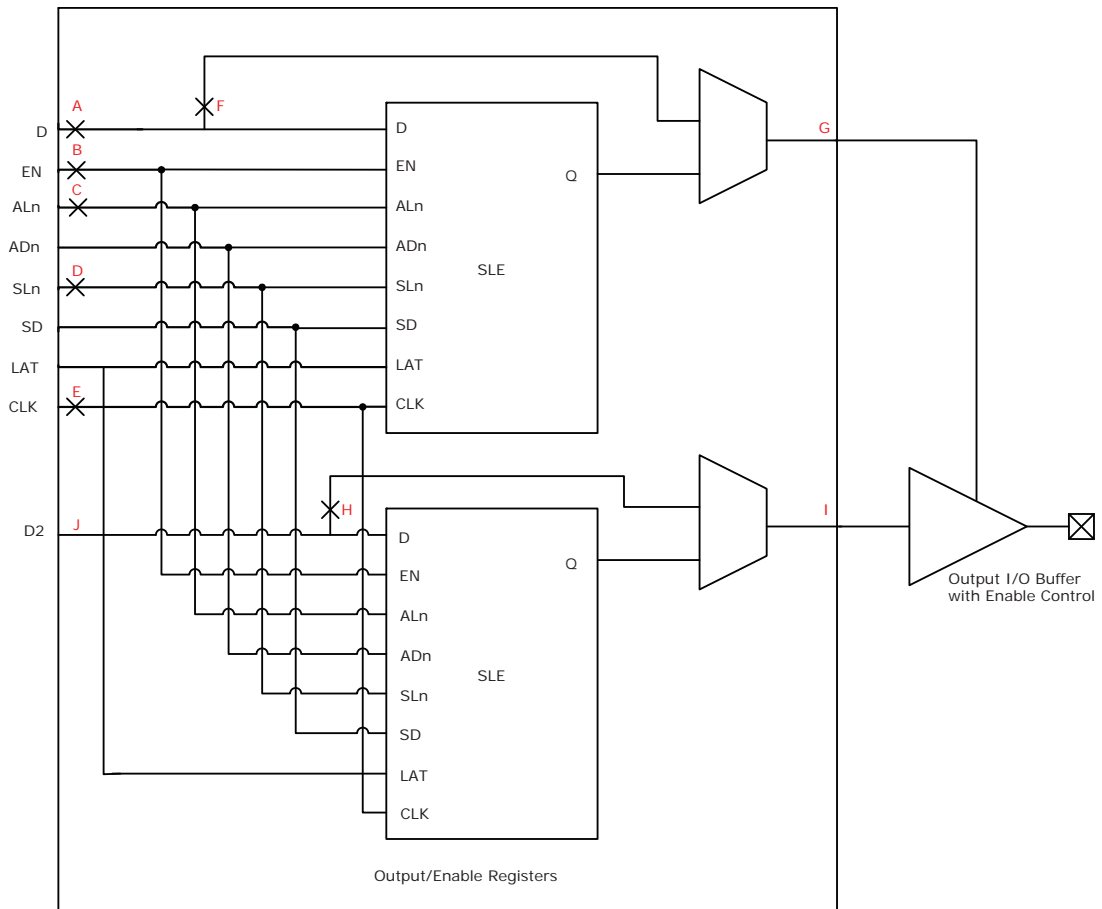
Parameter	Symbol	Typ	Unit
Termination resistance	RT	100	$\Omega$

**Table 209 • RSDS AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	Cross point	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF

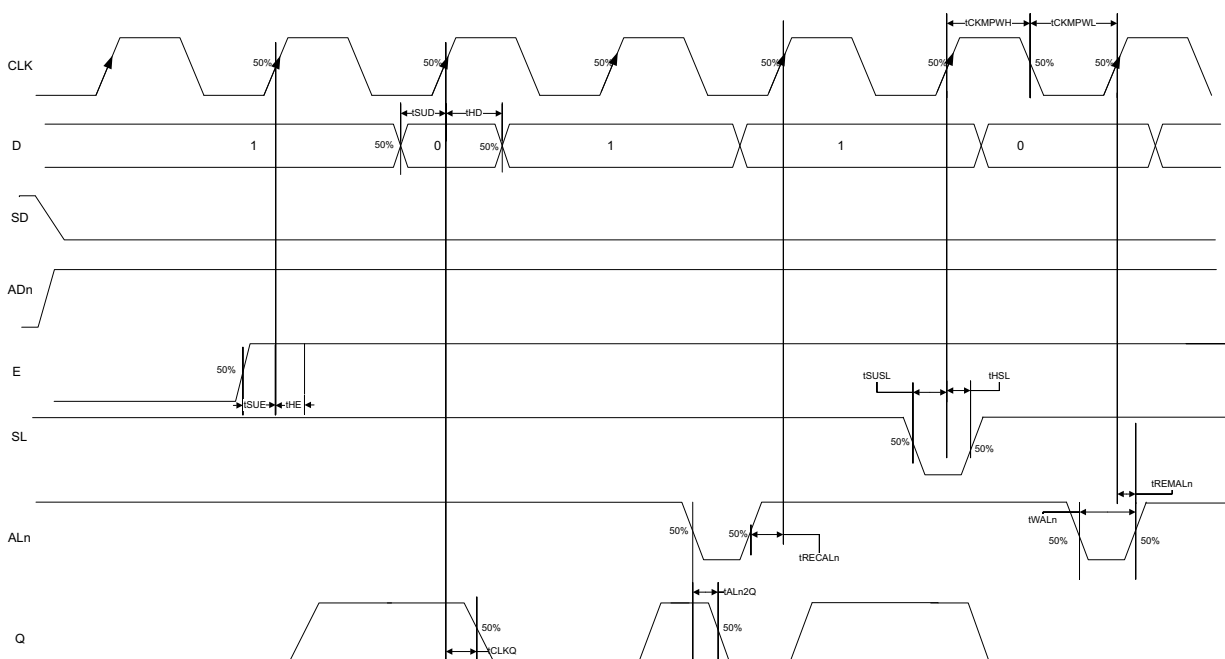
### 2.3.8.2 Output/Enable Register

Figure 8 • Timing Model for Output/Enable Register



The following figure shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

**Figure 16 • Sequential Module Timing Diagram**



### 2.3.10.3.1 Timing Characteristics

The following table lists the register delays in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 224 • Register Delays**

Parameter	Symbol	-1	-Std	Unit
Clock-to-Q of the core register	$T_{CLKQ}$	0.108	0.127	ns
Data setup time for the core register	$T_{SUD}$	0.254	0.298	ns
Data hold time for the core register	$T_{HD}$	0	0	ns
Enable setup time for the core register	$T_{SUE}$	0.335	0.394	ns
Enable hold time for the core register	$T_{HE}$	0	0	ns
Synchronous load setup time for the core register	$T_{SUSL}$	0.335	0.394	ns
Synchronous load hold time for the core register	$T_{HSL}$	0	0	ns
Asynchronous Clear-to-Q of the core register (ADn = 1)	$T_{ALn2Q}$	0.473	0.556	ns
Asynchronous preset-to-Q of the core register (ADn = 0)		0.451	0.531	ns
Asynchronous load removal time for the core register	$T_{REMAln}$	0	0	ns
Asynchronous load recovery time for the core register	$T_{RECALn}$	0.353	0.415	ns
Asynchronous load minimum pulse width for the core register	$T_{WALn}$	0.266	0.313	ns
Clock minimum pulse width high for the core register	$T_{CKMPWH}$	0.065	0.077	ns
Clock minimum pulse width low for the core register	$T_{CKMPWL}$	0.139	0.164	ns

**Table 240 •  $\mu$ SRAM (RAM128x8) in 128 x 8 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.091		0.107		ns
Read address hold time in asynchronous mode		-0.778		-0.915		ns
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHD}$	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	$T_{RSTREM}$	-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	$T_{RSTREC}$	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	$T_{R2Q}$		0.835		0.982	ns
Read synchronous reset setup time	$T_{SRSTSU}$	0.271		0.319		ns
Read synchronous reset hold time	$T_{SRSTHD}$	0.061		0.071		ns
Write clock period	$T_{CCY}$	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	$T_{BLKCSU}$	0.404		0.476		ns
Write block hold time	$T_{BLKCHD}$	0.007		0.008		ns
Write input data setup time	$T_{DINCSU}$	0.115		0.135		ns
Write input data hold time	$T_{DINCHD}$	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.026		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

**Table 248 • 2 Step IAP Programming (eNVM Only)**

<b>M2S/M2GL</b>					
<b>Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	137536	2	37	5	Sec
010	274816	4	76	11	Sec
025	274816	4	78	10	Sec
050	278528	3	85	9	Sec
060	268480	5	76	22	Sec
090	544496	10	152	43	Sec
150	544496	10	153	44	Sec

**Table 249 • 2 Step IAP Programming (Fabric and eNVM)**

<b>M2S/M2GL</b>					
<b>Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	439296	6	56	11	Sec
010	842688	11	100	21	Sec
025	1497408	19	113	32	Sec
050	2695168	32	136	48	Sec
060	2686464	43	137	70	Sec
090	4190208	68	236	115	Sec
150	6682768	109	286	162	Sec

**Table 250 • SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

<b>M2S/M2GL</b>					
<b>Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	302672	6	19	8	Sec
010	568784	10	26	14	Sec
025	1223504	21	39	29	Sec
050	2424832	39	60	50	Sec
060	2418896	44	65	54	Sec
090	3645968	66	90	79	Sec
150	6139184	108	140	128	Sec

**Table 251 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

<b>M2S/M2GL</b>					
<b>Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	137536	3	42	4	Sec
010	274816	4	82	7	Sec
025	274816	4	82	8	Sec
050	278528	4	80	8	Sec
060	268480	6	80	8	Sec
090	544496	10	157	15	Sec

**Table 265 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	69	49	50	Sec
010	99	57	57	Sec
025	150	64	63	Sec
050	55 <sup>1</sup>	Not Supported	Not Supported	Sec
060	313	105	104	Sec
090	449	131	130	Sec
150	730	179	183	Sec

1. Auto programming in 050 device is done through SC\_SPI, and SPI CLK is set to 6.25 MHz.

**Table 266 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	63	70	71	Sec
010	108	109	109	Sec
025	109	107	108	Sec
050	107	Not Supported	Not Supported	Sec
060	100	108	108	Sec
090	176	184	184	Sec
150	183	183	183	Sec

**Table 267 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	109	89	88	Sec
010	183	135	135	Sec
025	251	142	143	Sec
050	134	Not Supported	Not Supported	Sec
060	390	183	180	Sec
090	604	283	282	Sec
150	889	331	332	Sec



## 2.3.21 Clock Conditioning Circuits (CCC)

The following table lists the CCC/PLL specifications in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 282 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**

Parameter	Min	Typ	Max	Unit	Conditions
Clock conditioning circuitry input frequency $F_{IN\_CCC}$	1		200	MHz	All CCC
	0.032		200	MHz	32 kHz capable CCC
Clock conditioning circuitry output frequency $F_{OUT\_CCC}^1$	0.078		400	MHz	
PLL VCO frequency <sup>2</sup>	500		1000	MHz	
Delay increments in programmable delay blocks		75	100	ps	
Number of programmable values in each programmable delay block			64		
Acquisition time		70	100	$\mu\text{s}$	$F_{IN} \geq 1\text{ MHz}$
		1	16	ms	$F_{IN} = 32\text{ kHz}$
Input duty cycle (reference clock)	Internal Feedback				
	10		90	%	$1\text{ MHz} \leq F_{IN\_CCC} \leq 25\text{ MHz}$
	25		75	%	$25\text{ MHz} \leq F_{IN\_CCC} \leq 100\text{ MHz}$
	35		65	%	$100\text{ MHz} \leq F_{IN\_CCC} \leq 150\text{ MHz}$
	45		55	%	$150\text{ MHz} \leq F_{IN\_CCC} \leq 200\text{ MHz}$
	External Feedback (CCC, FPGA, Off-chip)				
	25		75	%	$1\text{ MHz} \leq F_{IN\_CCC} \leq 25\text{ MHz}$
	35		65	%	$25\text{ MHz} \leq F_{IN\_CCC} \leq 35\text{ MHz}$
	45		55	%	$35\text{ MHz} \leq F_{IN\_CCC} \leq 50\text{ MHz}$
	Output duty cycle	48		52	%
48			52	%	005, 010, and 025 devices $F_{OUT} < 350\text{ MHz}$
46			54	%	005, 010, and 025 devices $350\text{ MHz} \leq F_{out} \leq 400\text{ MHz}$
48			52	%	060 and 090 devices $F_{OUT} \leq 100\text{ MHz}$
44			52	%	060 and 090 devices $100\text{ MHz} \leq F_{OUT} \leq 400\text{ MHz}$
48			52	%	150 devices $F_{OUT} \leq 120\text{ MHz}$
45			52	%	150 devices $120\text{ MHz} \leq F_{OUT} \leq 400\text{ MHz}$
<b>Spread Spectrum Characteristics</b>					
Modulation frequency range	25	35	50	k	
Modulation depth range	0		1.5	%	
Modulation depth control		0.5		%	

## 2.3.24 Power-up to Functional Times

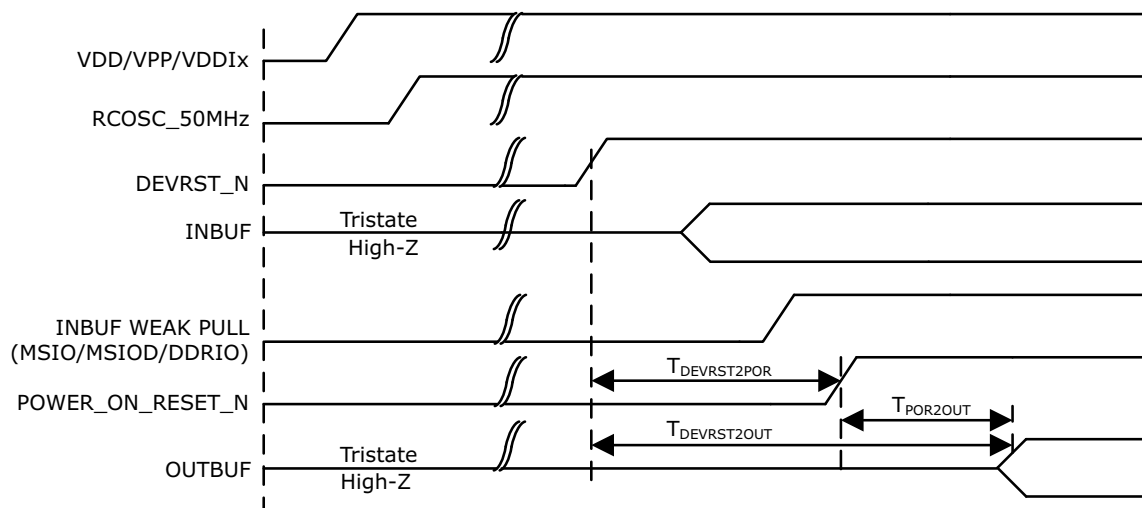
The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 288 • Power-up to Functional Times for SmartFusion2**

Symbol	From	To	Description	Maximum Power-up to Functional Time for SmartFusion2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	647	500	531	483	474	524	647
$T_{POR2MSSRST}$	POWER_ON_RESET_N	MSS_RESE T_N_M2F	Fabric to MSS	644	497	528	480	468	518	641
$T_{MSSRST2OUT}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.6	3.6	3.6	3.4	4.9	4.8	4.8
$T_{VDD2OUT}$	$V_{DD}$	Output available at I/O	$V_{DD}$ at its minimum threshold level to output	3096	2975	3012	2959	2869	2992	3225
$T_{VDD2POR}$	$V_{DD}$	POWER_ON_RESET_N	$V_{DD}$ at its minimum threshold level to fabric	2476	2487	2496	2486	2406	2563	2602
$T_{VDD2MSSRST}$	$V_{DD}$	MSS_RESE T_N_M2F	$V_{DD}$ at its minimum threshold level to MSS	3093	2972	3008	2956	2864	2987	3220
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

**Note:** For more information about power-up times, see [UG0331: SmartFusion2 Microcontroller Subsystem User Guide](#).

Figure 20 • DEVRST\_N to Functional Timing Diagram for IGLOO2



### 2.3.27 Flash\*Freeze Timing Characteristics

The following table lists the Flash\*Freeze entry and exit times in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 293 • Flash\*Freeze Entry and Exit Times

Parameter	Symbol	Entry/Exit Timing			Unit	Conditions
		FCLK = 100MHz		FCLK = 3 MHz		
		005, 010, 025, 060, 090, and 150	050	All Devices		
Entry time	TFF_ENTRY	160	150	320	$\mu\text{s}$	eNVM and MSS/HPMS PLL = ON
		215	200	430	$\mu\text{s}$	eNVM and MSS/HPMS PLL= OFF
Exit time with respect to the MSS PLL Lock	TFF_EXIT	100	100	140	$\mu\text{s}$	eNVM and MSS/HPMS PLL = ON during F*F
		136	120	190	$\mu\text{s}$	eNVM = ON and MSS/HPMS PLL = OFF during F*F and MSS/HPMS PLL turned back on at exit
		200	200	285	$\mu\text{s}$	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit
		200	200	285	$\mu\text{s}$	eNVM = OFF and MSS/HPMS PLL = ON during F*F and eNVM turned back on at exit

**Table 303 • I2C Characteristics (continued)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Maximum data rate	$D_{MAX}$			400	Kbps	Fast mode
				100	Kbps	Standard mode
Pulse width of spikes which must be suppressed by the input filter	$T_{FILT}$		50		ns	Fast mode

1. These values are provided for MSIO Bank–LVTTTL 8 mA Low Drive at 25 °C, typical conditions. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on  $V_{DDIX}$ , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
3.  $R(PULL-DOWN-MAX) = (VOLspec)/IOLspec$ .
4.  $R(PULL-UP-MAX) = (VDDImax-VOHspec)/IOHspec$ .

The following table lists the I<sup>2</sup>C switching characteristics in worst-case industrial conditions when  $T_J = 100\text{ °C}$ ,  $V_{DD} = 1.14\text{ V}$

**Table 304 • I2C Switching Characteristics**

Parameter	Symbol	-1		Unit
		Min	Min	
Low period of I2C_x_SCL	$T_{LOW}$	1	1	PCLK cycles
High period of I2C_x_SCL	$T_{HIGH}$	1	1	PCLK cycles
START hold time	$T_{HD;STA}$	1	1	PCLK cycles
START setup time	$T_{SU;STA}$	1	1	PCLK cycles
DATA hold time	$T_{HD;DAT}$	1	1	PCLK cycles
DATA setup time	$T_{SU;DAT}$	1	1	PCLK cycles
STOP setup time	$T_{SU;STO}$	1	1	PCLK cycles

**Figure 21 • I<sup>2</sup>C Timing Parameter Definition**

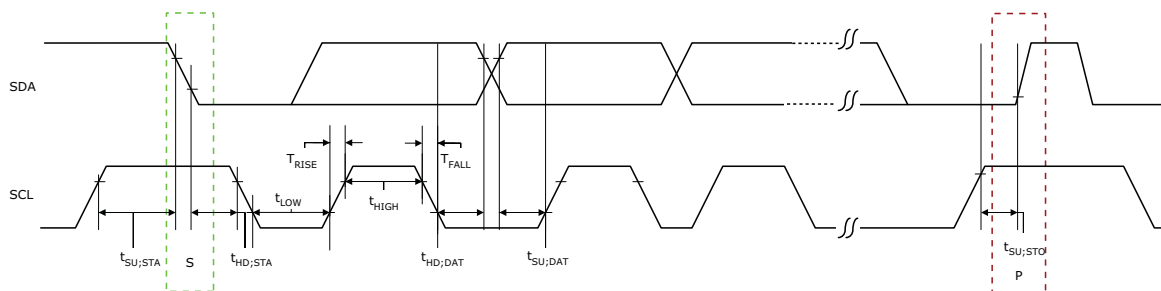
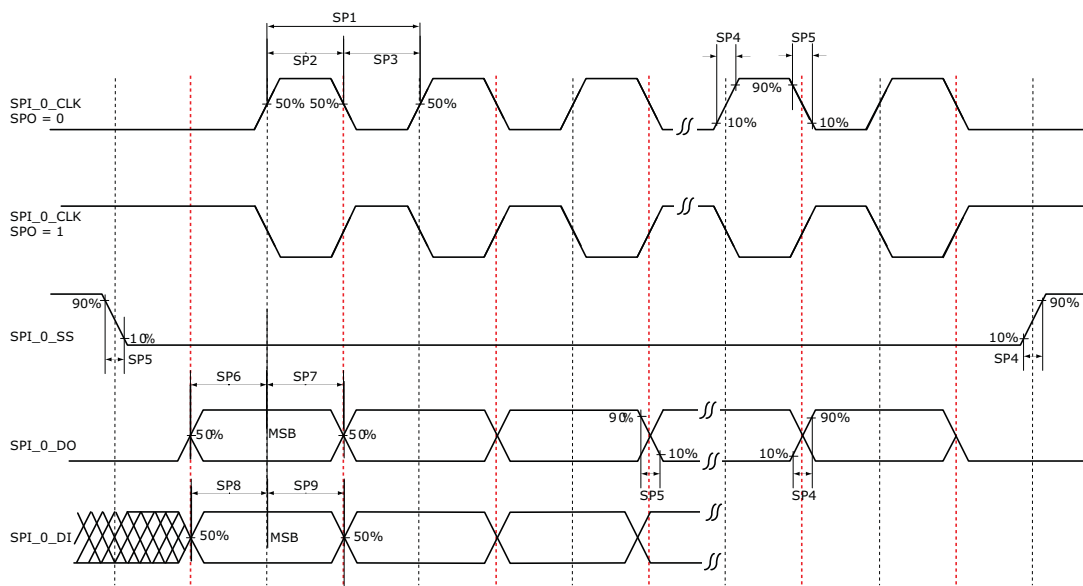


Figure 22 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)



### 2.3.32 CAN Controller Characteristics

The following table lists the CAN controller characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 306 • CAN Controller Characteristics

Parameter	Description	-1	-Std	Unit
FCANREFCLK <sup>1</sup>	Internally sourced CAN reference clock frequency	160	136	MHz
BAUDCANMAX	Maximum CAN performance baud rate	1	1	Mbps
BAUDCANMIN	Minimum CAN performance baud rate	0.05	0.05	Mbps

1. PCLK to CAN controller must be a multiple of 8 MHz.

### 2.3.33 USB Characteristics

The following table lists the USB characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 307 • USB Characteristics

Parameter	Description	-1	-Std	Unit
FUSBREFCLK	Internally sourced USB reference clock frequency	166	142	MHz
TUSBCLK	USB clock period	16.66	16.66	ns
TUSBPD	Clock to USB data propagation delay	9.0	9.0	ns
TUSBSU	Setup time for USB data	6.0	6.0	ns
TUSBHD	Hold time for USB data	0	0	ns