



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	56340
Total RAM Bits	1869824
Number of I/O	200
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	325-TFBGA, FCBGA
Supplier Device Package	325-FCBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl050ts-1fcs325i

2.3.5.2 Output Buffer and AC Loading

The following figure shows the output buffer and AC loading.

Figure 4 • Output Buffer AC Loading

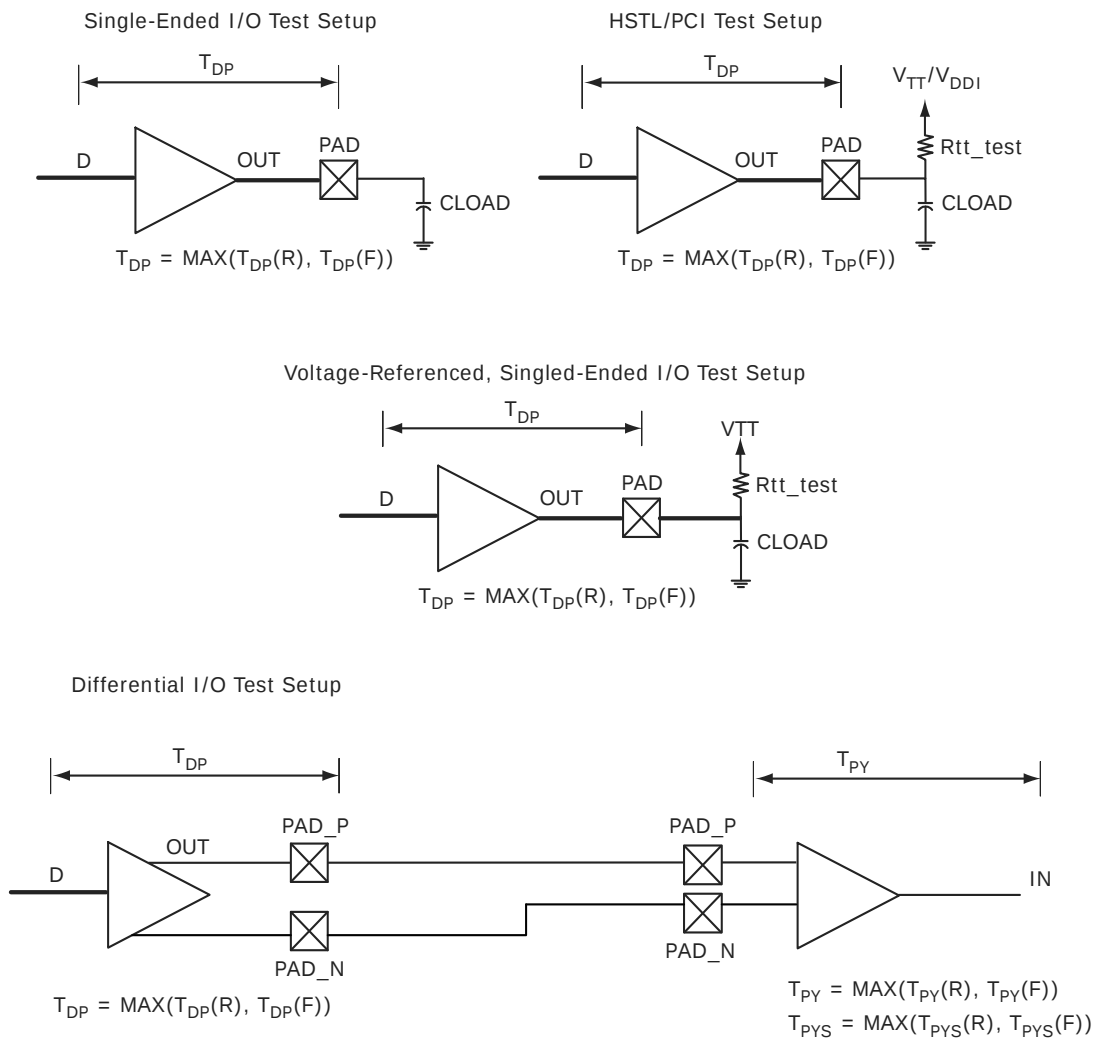


Table 34 • LVTTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.4	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 35 • LVTTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank

Output Drive Selection	V_{OH} (V)	V_{OL} (V)	IOH (at V_{OH}) mA	IOL (at V_{OL}) mA
2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	$V_{DDI} - 0.4$	0.4	4	4
8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA	$V_{DDI} - 0.4$	0.4	16	16
20 mA	$V_{DDI} - 0.4$	0.4	20	20

Note: For a detailed I/V curve, use the corresponding IBIS models:
www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.0\text{ V}$

Table 36 • LVTTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	2.262	2.663	2.289	2.695	ns

Table 37 • LVTTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.192	3.755	3.47	4.083	2.969	3.494	1.856	2.183	3.337	3.926	ns
4 mA	Slow	2.331	2.742	2.673	3.145	2.526	2.973	3.034	3.569	4.451	5.236	ns
8 mA	Slow	2.135	2.511	2.33	2.741	2.297	2.703	4.532	5.331	4.825	5.676	ns
12 mA	Slow	2.052	2.414	2.107	2.479	2.162	2.544	5.75	6.764	5.445	6.406	ns
16 mA	Slow	2.062	2.425	2.072	2.438	2.145	2.525	5.993	7.05	5.625	6.618	ns
20 mA	Slow	2.148	2.527	1.999	2.353	2.088	2.458	6.262	7.367	5.876	6.913	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 62 • LVCMOS 1.5 V DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC output logic high	VOH	$V_{DDI} \times 0.75$		V
DC output logic low	VOL		$V_{DDI} \times 0.25$	V

Table 63 • LVCMOS 1.5 V AC Minimum and Maximum Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D _{MAX}	235	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D _{MAX}	160	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	D _{MAX}	220	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 64 • LVCMOS 1.5 V AC Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CA L	75, 60, 50, 40	Ω

Table 65 • LVCMOS 1.5 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point	V _{TRIP}	0.75	V
Resistance for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	R _{ENT}	2K	Ω
Capacitive loading for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	C _{ENT}	5	pF
Capacitive loading for data path (T _{DP})	C _{LOAD}	5	pF

Table 66 • LVCMOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			V _{OH} (V)	V _{OL} (V)	IOH (at V _{OH}) mA	IOL (at V _{OL}) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	2	2
4 mA	4 mA	4 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	4	4
6 mA	6 mA	6 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	6	6
8 mA		8 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	8	8
		10 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	10	10
		12 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	12	12

Note: For a detailed I/V curve, use the corresponding IBIS models:
www.microsemi.com/soc/download/ibis/default.aspx.

Table 136 • SSTL15 AC Test Parameter Specifications (for DDRIO I/O Bank Only)

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.75	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for SSTL15 Class I (T_{DP})	RTT_TEST	50	Ω
Reference resistance for data test path for SSTL15 Class II (T_{DP})	RTT_TEST	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.425\text{ V}$

Table 137 • DDR3/SSTL15 Receiver Characteristics for DDRIO I/O Bank – with Calibration Only

		T_{PY}		Unit
On-Die Termination (ODT)		-1	-Std	
Pseudo differential	None	1.605	1.888	ns
	20	1.616	1.901	ns
	30	1.613	1.897	ns
	40	1.611	1.895	ns
	60	1.609	1.893	ns
	120	1.607	1.89	ns
True differential	None	1.623	1.91	ns
	20	1.637	1.926	ns
	30	1.63	1.918	ns
	40	1.626	1.914	ns
	60	1.622	1.91	ns
	120	1.619	1.905	ns

Table 138 • DDR3/SSTL15 Transmitter Characteristics (Output and Tristate Buffers)

	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ}		T _{LZ}		Unit
	−1	−Std	−1	−Std	−1	−Std	−1	−Std	−1	−Std	
DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)											
Single-ended	2.533	2.98	2.522	2.967	2.523	2.968	2.427	2.855	2.428	2.856	ns
Differential	2.555	3.005	3.073	3.615	3.073	3.615	2.416	2.843	2.416	2.843	ns
DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)											
Single-ended	2.53	2.977	2.514	2.958	2.516	2.96	2.422	2.849	2.425	2.852	ns
Differential	2.552	3.002	2.591	3.048	2.59	3.047	2.882	3.391	2.881	3.39	ns

2.3.6.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 139 • LPDDR DC Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max
Supply voltage	V_{DDI}	1.71	1.8	1.89
Termination voltage	V_{TT}	0.838	0.900	0.964
Input reference voltage	V_{REF}	0.838	0.900	0.964

Table 140 • LPDDR DC Input Voltage Specification

Parameter	Symbol	Min	Max
DC input logic high	V_{IH} (DC)	$0.7 \times V_{DDI}$	1.89
DC input logic low	V_{IL} (DC)	-0.3	$0.3 \times V_{DDI}$
Input current high ¹	I_{IH} (DC)		
Input current low ¹	I_{IL} (DC)		

1. See Table 24, page 22.

Table 141 • LPDDR DC Output Voltage Specification Reduced Drive

Parameter	Symbol	Min	Max
DC output logic high	V_{OH}	$0.9 \times V_{DDI}$	
DC output logic low	V_{OL}		$0.1 \times V_{DDI}$
Output minimum source DC current	I_{OH} at V_{OH}	0.1	
Output minimum sink current	I_{OL} at V_{OL}	-0.1	

Table 142 • LPDDR DC Output Voltage Specification Full Drive¹

Parameter	Symbol	Min	Max
DC output logic high	V_{OH}	$0.9 \times V_{DDI}$	
DC output logic low	V_{OL}		$0.1 \times V_{DDI}$
Output minimum source DC current	I_{OH} at V_{OH}	0.1	
Output minimum sink current	I_{OL} at V_{OL}	-0.1	

1. To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.

Table 143 • LPDDR DC Differential Voltage Specification

Parameter	Symbol	Min
DC input differential voltage	V_{ID} (DC)	$0.4 \times V_{DDI}$

Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers) (continued)

10 mA	medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	medium_fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
	slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
12 mA	medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	medium_fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
	slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
16 mA	medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	medium_fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
	slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	medium_fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management).

2.3.7 Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

2.3.7.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

Minimum and Maximum Input and Output Levels

Table 160 • LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{DDI}	2.375	2.5	2.625	V	2.5 V range
Supply voltage	V_{DDI}	3.15	3.3	3.45	V	3.3 V range

Table 161 • LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit	Conditions
DC Input voltage	V_I	0	2.925	V	2.5 V range
DC input voltage	V_I	0	3.45	V	3.3 V range
Input current high ¹	I_{IH} (DC)				
Input current low ¹	I_{IL} (DC)				

1. See Table 24, page 22.

Table 215 • LVPECL DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	3.45	V

Table 216 • LVPECL DC Differential Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
Input common mode voltage	V_{ICM}	0.3		2.8	V
Input differential voltage	V_{IDIFF}	100	300	1,000	mV

Table 217 • LVPECL Minimum and Maximum AC Switching Speeds

Parameter	Symbol	Max	Unit
Maximum data rate	D_{MAX}	900	Mbps

AC Switching Characteristics

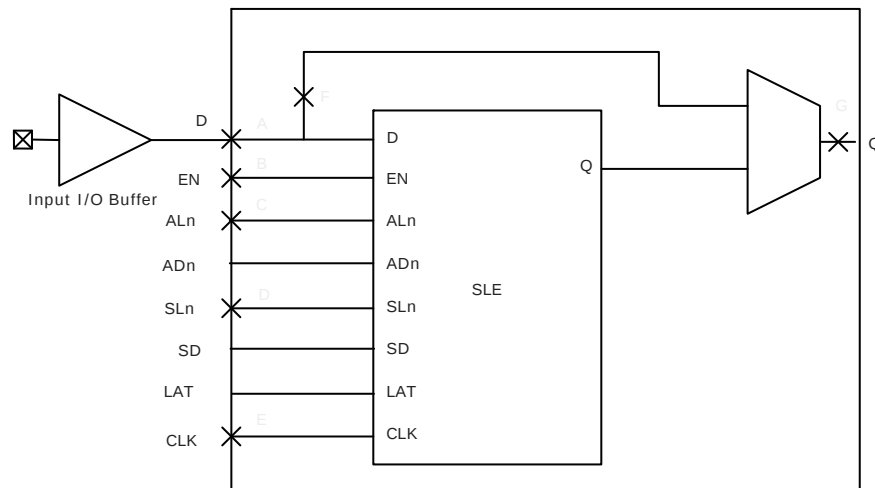
Worst commercial-case conditions: $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$.

Table 218 • LVPECL Receiver Characteristics for MSIO I/O Bank

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.572	3.025	ns
100	2.569	3.023	ns

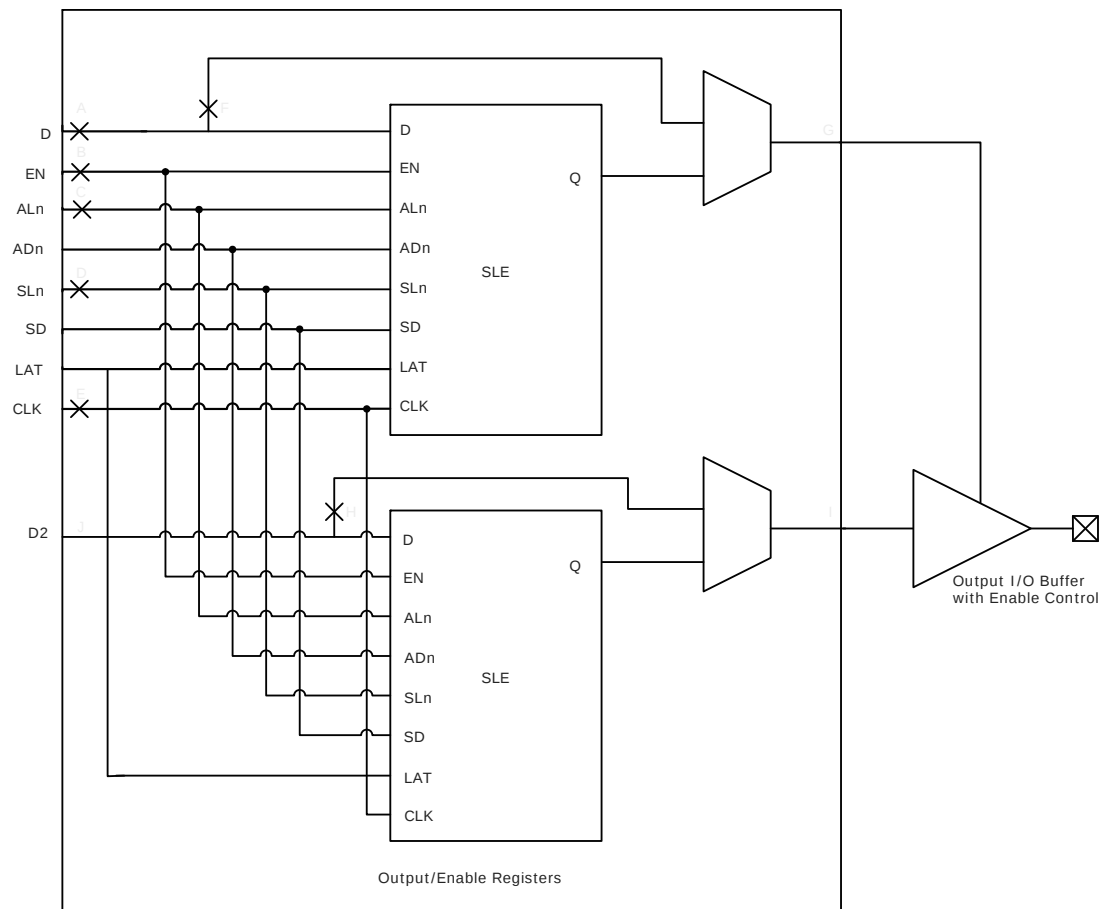
2.3.8 I/O Register Specifications

This section describes input and output register specifications.

2.3.8.1 Input Register**Figure 6 • Timing Model for Input Register**

2.3.8.2 Output/Enable Register

Figure 8 • Timing Model for Output/Enable Register

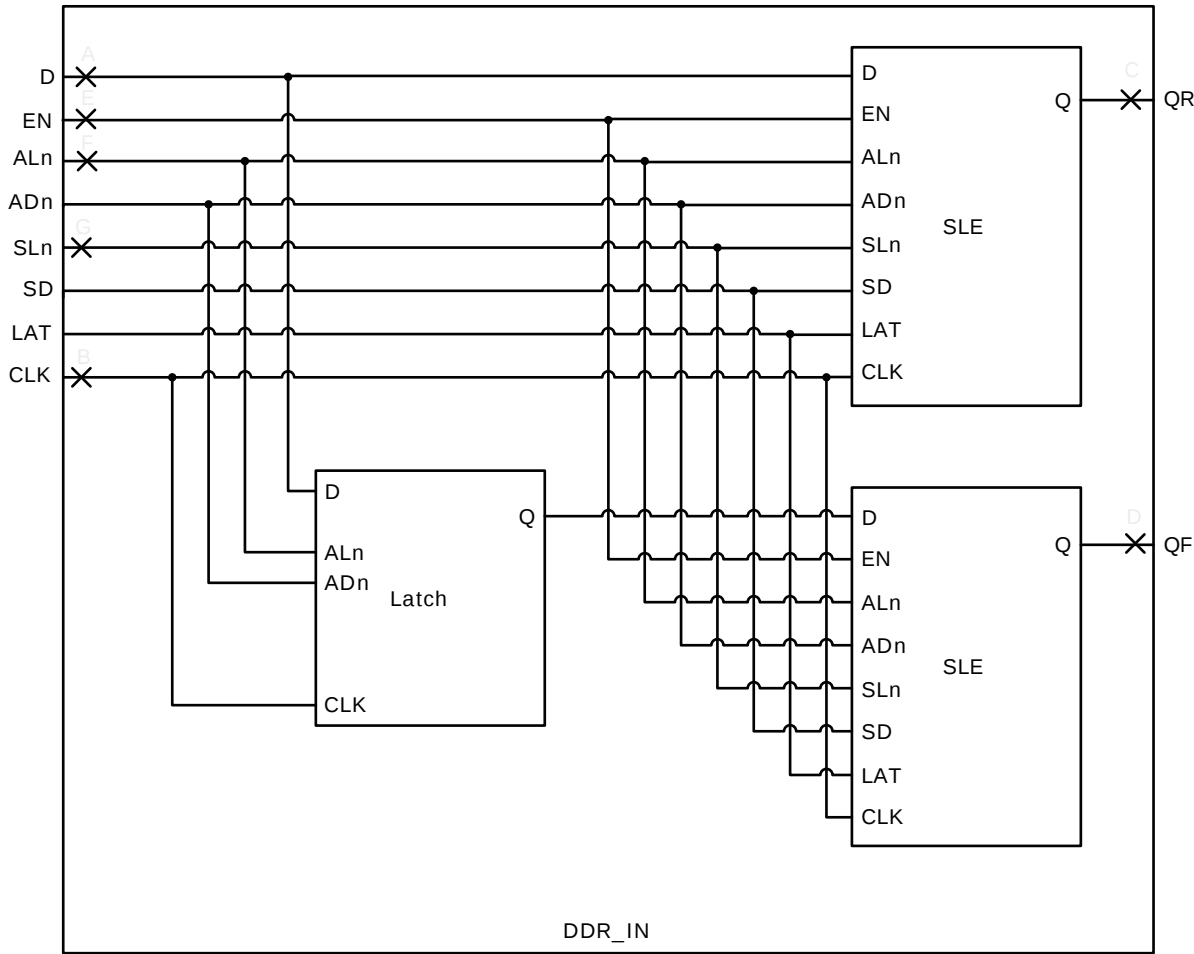


2.3.9 DDR Module Specification

This section describes input and output DDR module and timing specifications.

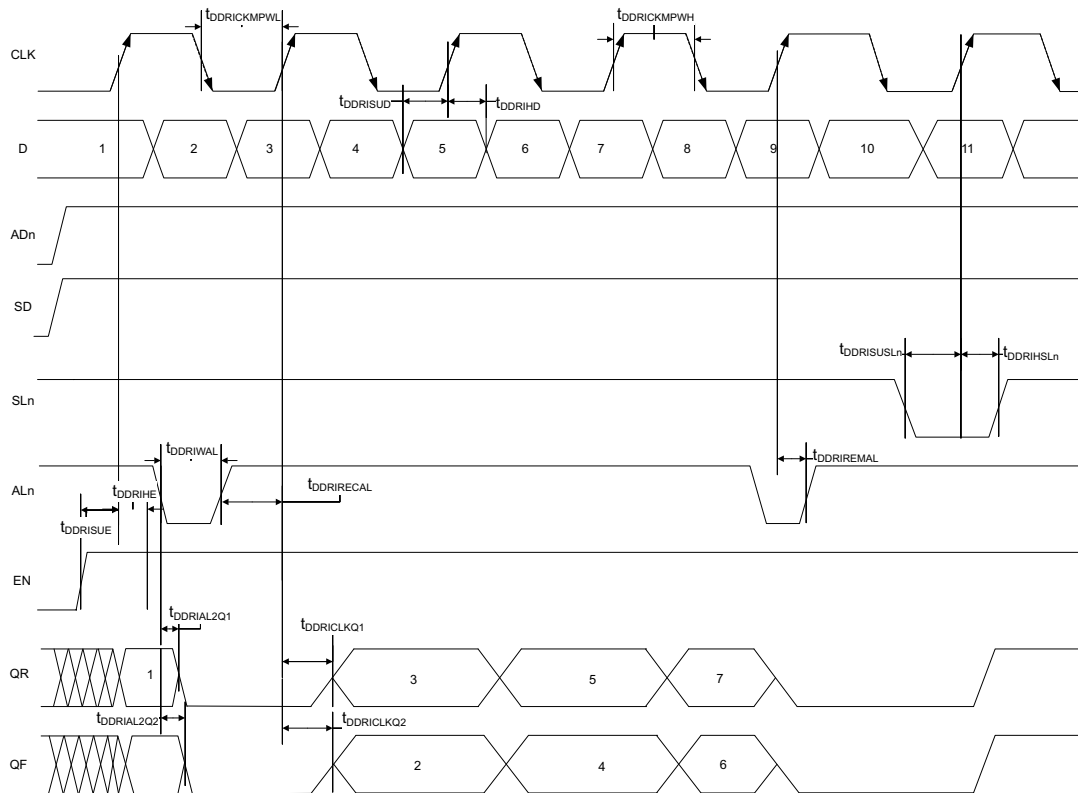
2.3.9.1 Input DDR Module

Figure 10 • Input DDR Module



2.3.9.2 Input DDR Timing Diagram

Figure 11 • Input DDR Timing Diagram



2.3.9.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 221 • Input DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDRICKQ1}$	Clock-to-Out Out_QR for input DDR	B, C	0.16	0.188	ns
$T_{DDRICKQ2}$	Clock-to-Out Out_QF for input DDR	B, D	0.166	0.195	ns
$T_{DDRISUD}$	Data setup for input DDR	A, B	0.357	0.421	ns
T_{DDRIHD}	Data hold for input DDR	A, B	0	0	ns
$T_{DDRISUE}$	Enable setup for input DDR	E, B	0.46	0.542	ns
T_{DDRIHE}	Enable hold for input DDR	E, B	0	0	ns
$T_{DDRISUSLn}$	Synchronous load setup for input DDR	G, B	0.46	0.542	ns
$T_{DDRIHSLn}$	Synchronous load hold for input DDR	G, B	0	0	ns
$T_{DDRIAL2Q1}$	Asynchronous load-to-out QR for input DDR	F, C	0.587	0.69	ns
$T_{DDRIAL2Q2}$	Asynchronous load-to-out QF for input DDR	F, D	0.541	0.636	ns
$T_{DDRIREMAL}$	Asynchronous load removal time for input DDR	F, B	0	0	ns
$T_{DDRIRECAL}$	Asynchronous load recovery time for input DDR	F, B	0.074	0.087	ns

Table 222 • Output DDR Propagation Delays (continued)

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDROWAL}$	Asynchronous load minimum pulse width for output DDR	C, C	0.304	0.357	ns
$T_{DDROCKMPWH}$	Clock minimum pulse width high for the output DDR	E, E	0.075	0.088	ns
$T_{DDROCKMPWL}$	Clock minimum pulse width low for the output DDR	E, E	0.159	0.187	ns

2.3.10 Logic Element Specifications

2.3.10.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, see *SmartFusion2 and IGLOO2 Macro Library Guide*.

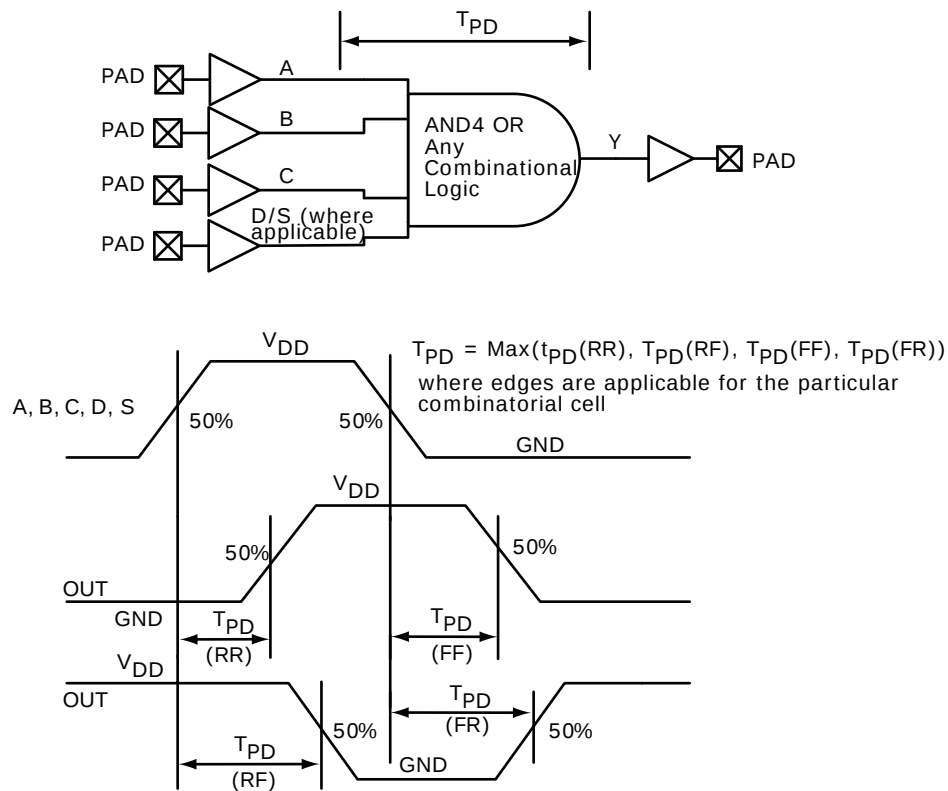
Figure 14 • LUT-4

Table 231 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18 (continued)

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Block select hold time	T _{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T _{BLK2Q}		1.529		1.799	ns
Block select minimum pulse width	T _{BLKMPW}	0.186		0.219		ns
Read enable setup time	T _{RDESU}	0.449		0.528		ns
Read enable hold time	T _{RDEHD}	0.167		0.197		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	T _{RDPLESU}	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	T _{RDPLEHD}	0.102		0.12		ns
Asynchronous reset to output propagation delay	T _{R2Q}	–	1.506	–	1.772	ns
Asynchronous reset removal time	T _{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T _{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T _{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	T _{PLRSTREM}	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	T _{PLRSTREC}	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	T _{PLRSTMPW}	0.282		0.332		ns
Synchronous reset setup time	T _{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T _{SRSTHD}	0.036		0.043		ns
Write enable setup time	T _{WESU}	0.39		0.458		ns
Write enable hold time	T _{WEHD}	0.242		0.285		ns
Maximum frequency	F _{MAX}		400		340	MHz

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 2K × 9 in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 232 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	T _{CY}	2.5		2.941		ns
Clock minimum pulse width high	T _{CLKMPWH}	1.125		1.323		ns
Clock minimum pulse width low	T _{CLKMPWL}	1.125		1.323		ns
Pipelined clock period	T _{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	T _{PLCLKMPWH}	1.125		1.323		ns
Pipelined clock minimum pulse width low	T _{PLCLKMPWL}	1.125		1.323		ns
Read access time with pipeline register			0.334		0.393	ns
Read access time without pipeline register	T _{CLK2Q}		2.273		2.674	ns
Access time with feed-through write timing			1.529		1.799	ns

Table 237 • μ SRAM (RAM64x18) in 64 × 18 Mode (continued)

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 64 × 16 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 238 • μ SRAM (RAM64x16) in 64 × 16 Mode

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		–0.778		–0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.983	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns

Table 262 • SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	302672	6	41	8	Sec
010	568784	10	48	14	Sec
025	1223504	21	61	29	Sec
050	2424832	39	82	50	Sec
060	2418896	44	87	54	Sec
090	3645968	66	112	79	Sec
150	6139184	108	162	128	Sec

Table 263 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	137536	3	64	4	Sec
010	274816	4	104	7	Sec
025	274816	4	104	8	Sec
050	2,78,528	4	102	8	Sec
060	268480	6	102	8	Sec
090	544496	10	179	15	Sec
150	544496	10	180	15	Sec

Table 264 • SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)

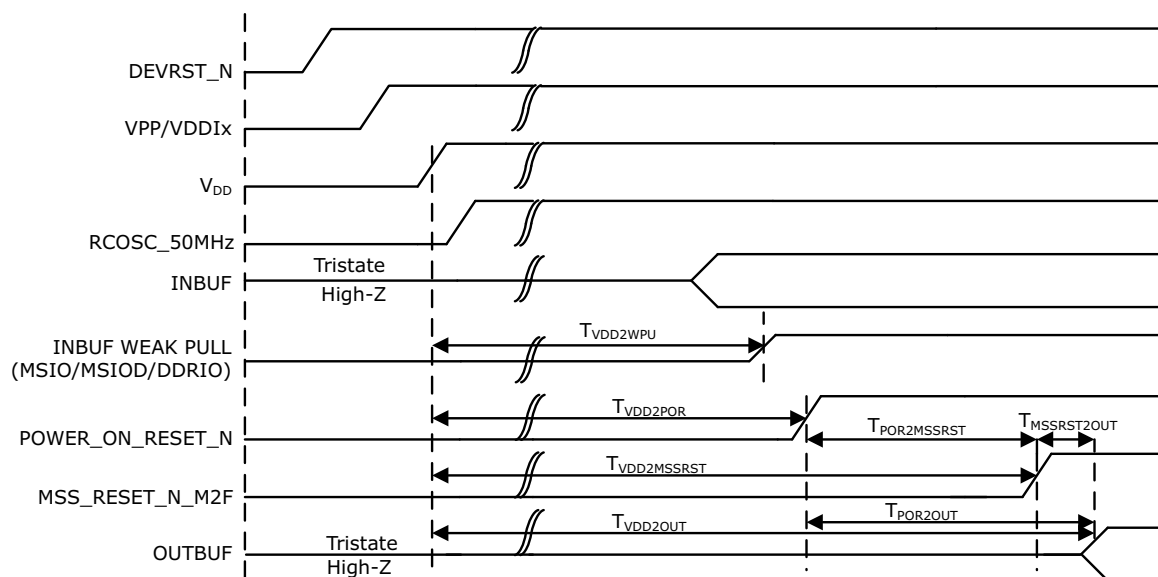
M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	9	83	11	Sec
010	842688	15	129	21	Sec
025	1497408	26	143	35	Sec
050	2695168	43	163	55	Sec
060	2686464	48	165	60	Sec
090	4190208	75	266	91	Sec
150	6682768	117	318	141	Sec

2.3.21 Clock Conditioning Circuits (CCC)

The following table lists the CCC/PLL specifications in worst-case industrial conditions when $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 282 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification

Parameter	Min	Typ	Max	Unit	Conditions
Clock conditioning circuitry input frequency F_{IN_CCC}	1		200	MHz	All CCC
	0.032		200	MHz	32 kHz capable CCC
Clock conditioning circuitry output frequency $F_{OUT_CCC}^1$	0.078		400	MHz	
PLL VCO frequency ²	500		1000	MHz	
Delay increments in programmable delay blocks		75	100	ps	
Number of programmable values in each programmable delay block			64		
Acquisition time		70	100	μs	$F_{IN} \geq 1\text{ MHz}$
		1	16	ms	$F_{IN} = 32\text{ kHz}$
Input duty cycle (reference clock)					Internal Feedback
	10		90	%	$1\text{ MHz} \leq F_{IN_CCC} \leq 25\text{ MHz}$
	25		75	%	$25\text{ MHz} \leq F_{IN_CCC} \leq 100\text{ MHz}$
	35		65	%	$100\text{ MHz} \leq F_{IN_CCC} \leq 150\text{ MHz}$
	45		55	%	$150\text{ MHz} \leq F_{IN_CCC} \leq 200\text{ MHz}$
					External Feedback (CCC, FPGA, Off-chip)
	25		75	%	$1\text{ MHz} \leq F_{IN_CCC} \leq 25\text{ MHz}$
	35		65	%	$25\text{ MHz} \leq F_{IN_CCC} \leq 35\text{ MHz}$
	45		55	%	$35\text{ MHz} \leq F_{IN_CCC} \leq 50\text{ MHz}$
	48		52	%	050 devices $F_{OUT} \leq 400\text{ MHz}$
	48		52	%	005, 010, and 025 devices $F_{OUT} < 350\text{ MHz}$
	46		54	%	005, 010, and 025 devices $350\text{ MHz} \leq F_{out} \leq 400\text{ MHz}$
Output duty cycle	48		52	%	060 and 090 devices $F_{OUT} \leq 100\text{ MHz}$
	44		52	%	060 and 090 devices $100\text{ MHz} \leq F_{OUT} \leq 400\text{ MHz}$
	48		52	%	150 devices $F_{OUT} \leq 120\text{ MHz}$
	45		52	%	150 devices $120\text{ MHz} \leq F_{OUT} \leq 400\text{ MHz}$
Spread Spectrum Characteristics					
Modulation frequency range	25	35	50	k	
Modulation depth range	0		1.5	%	
Modulation depth control		0.5		%	

Figure 17 • Power-up to Functional Timing Diagram for SmartFusion2

The following table lists the IGLOO2 power-up to functional times in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 289 • Power-up to Functional Times for IGLOO2

				Maximum Power-up to Functional Time for IGLOO2 (uS)						
Symbol	From	To	Description	005	010	025	050	060	090	150
T _{POR2OUT}	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	114	114	113	114	114	114
T _{VDD2OUT}	V _{DD}	Output available at I/O	V _{DD} at its minimum threshold level to output	2587	2600	2607	2558	2591	2600	2699
T _{VDD2POR}	V _{DD}	POWER_ON_RESET_N	V _{DD} at its minimum threshold level to fabric	2474	2486	2493	2445	2477	2486	2585
T _{VDD2WPU}	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide*.

The following table lists the IGLOO2 DEVRST_N to functional times in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 292 • DEVRST_N to Functional Times for IGLOO2

Symbol	From	To	Description	Maximum Power-up to Functional Time for IGLOO2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	116	113	113	115	115	114
$T_{DEVRST2OUT}$	DEVRST_N	Output available at I/O	V_{DD} at its minimum threshold level to output	314	353	314	307	343	341	341
$T_{DEVRST2POR}$	DEVRST_N	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	200	238	201	195	230	229	227
$T_{DEVRST2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215

The following table lists the SerDes reference clock AC specifications in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 299 • SerDes Reference Clock AC Specifications

Parameter	Symbol	Min	Max	Unit
Reference clock frequency	F_{REFCLK}	100	160	MHz
Reference clock rise time	T_{RISE}	0.6	4	V/ns
Reference clock fall time	T_{FALL}	0.6	4	V/ns
Reference clock duty cycle	T_{CYC}	40	60	%
Reference clock mismatch	$M_{MREFCLK}$	-300	300	ppm
Reference spread spectrum clock	SSC_{ref}	0	5000	ppm

Table 300 • HCSL Minimum and Maximum DC Input Levels (Applicable to SerDes REFCLK Only)

Parameter	Symbol	Min	Typ	Max	Unit
Recommended DC Operating Conditions					
Supply voltage	V_{DDI}	2.375	2.5	2.625	V
HCSL DC Input Voltage Specification					
DC Input voltage	V_I	0		2.625	V
HCSL Differential Voltage Specification					
Input common mode voltage	V_{ICM}	0.05		2.4	V
Input differential voltage	V_{IDIFF}	100		1100	mV

Table 301 • HCSL Minimum and Maximum AC Switching Speeds (Applicable to SerDes REFCLK Only)

Parameter	Symbol	Min	Typ	Max	Unit
HCSL AC Specifications					
Maximum data rate (for MSIO I/O bank)	F_{MAX}			350	Mbps
HCSL Impedance Specifications					
Termination resistance	R_t		100		Ω

2.3.31 SmartFusion2 Specifications

2.3.31.1 MSS Clock Frequency

The following table lists the maximum frequency for MSS main clock in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 302 • Maximum Frequency for MSS Main Clock

Symbol	Description	-1	-Std	Unit
M3_CLK	Maximum frequency for the MSS main clock	166	142	MHz

Table 303 • I2C Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Maximum data rate	D_{MAX}			400	Kbps	Fast mode
				100	Kbps	Standard mode
Pulse width of spikes which must be suppressed by the input filter	T_{FILT}		50		ns	Fast mode

1. These values are provided for MSIO Bank–LVTTL 8 mA Low Drive at 25 °C, typical conditions. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on V_{DDIX} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
3. $R(PULL-DOWN-MAX) = (VOL_{spec})/IOL_{spec}$.
4. $R(PULL-UP-MAX) = (VDDImax - VOH_{spec})/IOH_{spec}$.

The following table lists the I²C switching characteristics in worst-case industrial conditions when $T_J = 100\text{ °C}$, $V_{DD} = 1.14\text{ V}$

Table 304 • I2C Switching Characteristics

Parameter	Symbol	–1	Std	Unit
		Min	Min	
Low period of I2C_x_SCL	T_{LOW}	1	1	PCLK cycles
High period of I2C_x_SCL	T_{HIGH}	1	1	PCLK cycles
START hold time	$T_{HD;STA}$	1	1	PCLK cycles
START setup time	$T_{SU;STA}$	1	1	PCLK cycles
DATA hold time	$T_{HD;DAT}$	1	1	PCLK cycles
DATA setup time	$T_{SU;DAT}$	1	1	PCLK cycles
STOP setup time	$T_{SU;STO}$	1	1	PCLK cycles

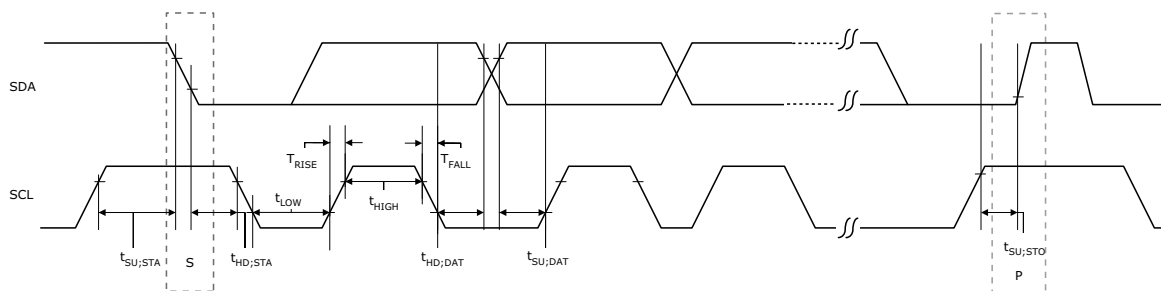
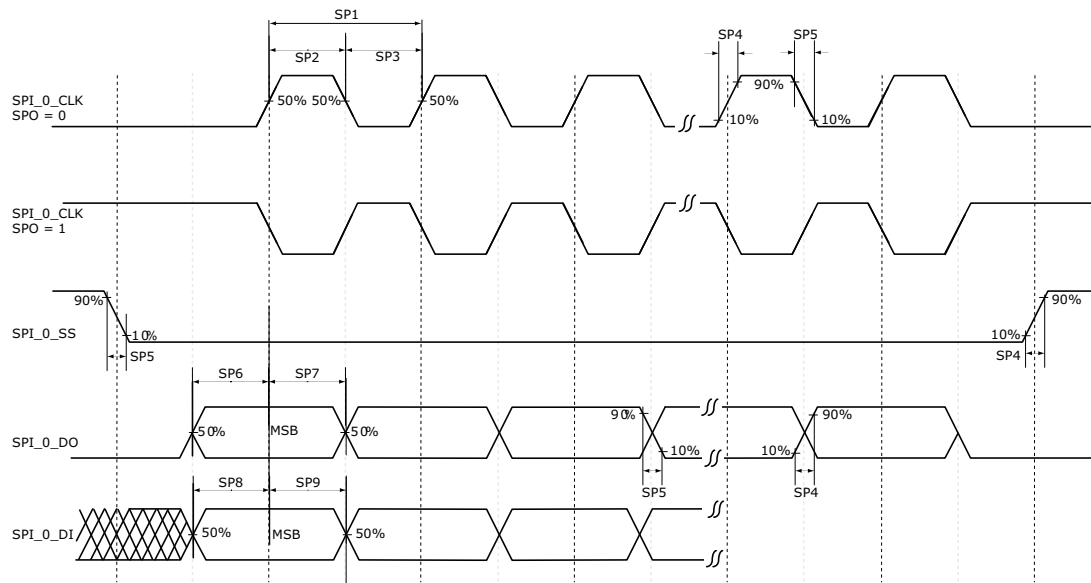
Figure 21 • I²C Timing Parameter Definition

Figure 22 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)

2.3.32 CAN Controller Characteristics

The following table lists the CAN controller characteristics in worst-case industrial conditions when $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 306 • CAN Controller Characteristics

Parameter	Description	–1	–Std	Unit
FCANREFCLK ¹	Internally sourced CAN reference clock frequency	160	136	MHz
BAUDCANMAX	Maximum CAN performance baud rate	1	1	Mbps
BAUDCANMIN	Minimum CAN performance baud rate	0.05	0.05	Mbps

1. PCLK to CAN controller must be a multiple of 8 MHz.

2.3.33 USB Characteristics

The following table lists the USB characteristics in worst-case industrial conditions when $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 307 • USB Characteristics

Parameter	Description	–1	–Std	Unit
FUSBREFCLK	Internally sourced USB reference clock frequency	166	142	MHz
TUSBCLK	USB clock period	16.66	16.66	ns
TUSBPD	Clock to USB data propagation delay	9.0	9.0	ns
TUSBSU	Setup time for USB data	6.0	6.0	ns
TUSBHD	Hold time for USB data	0	0	ns