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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### **Details**

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	56340
Total RAM Bits	1869824
Number of I/O	200
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	325-TFBGA, FCBGA
Supplier Device Package	325-FCBGA (11x11)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2gl050ts-fcs325">https://www.e-xfl.com/product-detail/microchip-technology/m2gl050ts-fcs325</a>

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## 2.3.2 Power Consumption

The following sections describe the power consumptions of the devices.

### 2.3.2.1 Quiescent Supply Current

**Table 10 • Quiescent Supply Current Characteristics**

Power Supplies/Blocks	Modes and Configurations	
	Non-Flash*Freeze	Flash*Freeze
FPGA Core	On	Off
$V_{DD}/SERDES_{[01]}_VDD^1$	On	On
$V_{PP}/V_{PPNVM}$	On	On
HPMS_MDDR_PLL_VDDA/FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA/PLL0_PLL1_HPMS_MDDR_VDD A	0 V	0 V
$SERDES_{[01]}_PLL_VDDA^2$	0 V	0 V
$SERDES_{[01]}_L[0123]_VDDAPLL/VDD_{2V5}^2$	On	On
$SERDES_{[01]}_L[0123]_VDDAIO^2$	On	On
$V_{DDIx}^{3,4}$	On	On
$V_{REFx}$	On	On
MSSDDR CLK	32 kHz	32 kHz
RAM	On	Sleep state
System controller	50 MHz	50 MHz
50 MHz oscillator (enable/disable)	Enable	Disabled
1 MHz oscillator (enable/disable)	Disabled	Disabled
Crystal oscillator (enable/disable)	Disabled	Disabled

- SERDES\_[01]\_VDD Power Supply is shorted to  $V_{DD}$ .
- SerDes and DDR blocks to be unused.
- $V_{DDIx}$  has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate  $V_{DDI}$  bank supplies. For details on bank power supplies, see "Recommendation for Unused Bank Supplies" table in the AC393: *SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.
- No Differential (that is to say, LVDS) I/Os or ODT attributes to be used.

**Table 11 • SmartFusion2 and IGLOO2 Quiescent Supply Current ( $V_{DD} = 1.2 V$ ) – Typical Process**

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC1	Non-Flash*Freeze	6.2	6.9	8.9	13.1	15.3	15.4	27.5	mA	Typical ( $T_J = 25\text{ }^\circ\text{C}$ )
		24.0	28.4	40.6	67.8	80.6	81.4	144.7	mA	Commercial ( $T_J = 85\text{ }^\circ\text{C}$ )
		35.2	41.9	60.5	102.1	121.4	122.6	219.1	mA	Industrial ( $T_J = 100\text{ }^\circ\text{C}$ )

**Table 15 • Inrush Currents at Power up,  $-40\text{ }^{\circ}\text{C} \leq T_J \leq 100\text{ }^{\circ}\text{C}$  – Typical Process**

Power Supplies	Voltage (V)	005	010	025	050	060	090	150	Unit
$V_{DD}$	1.26	25	32	38	48	45	77	109	mA
$V_{PP}$	3.46	33	49	36	180	13	36	51	mA
$V_{DDI}$	2.62	134	141	161	187	93	272	388	mA
Number of banks		7	8	8	10	10	9	19	

### 2.3.3 Average Fabric Temperature and Voltage Derating Factors

The following table lists the average temperature and voltage derating factors for fabric timing delays normalized to  $T_J = 85\text{ }^{\circ}\text{C}$ , in worst-case  $V_{DD} = 1.14\text{ V}$ .

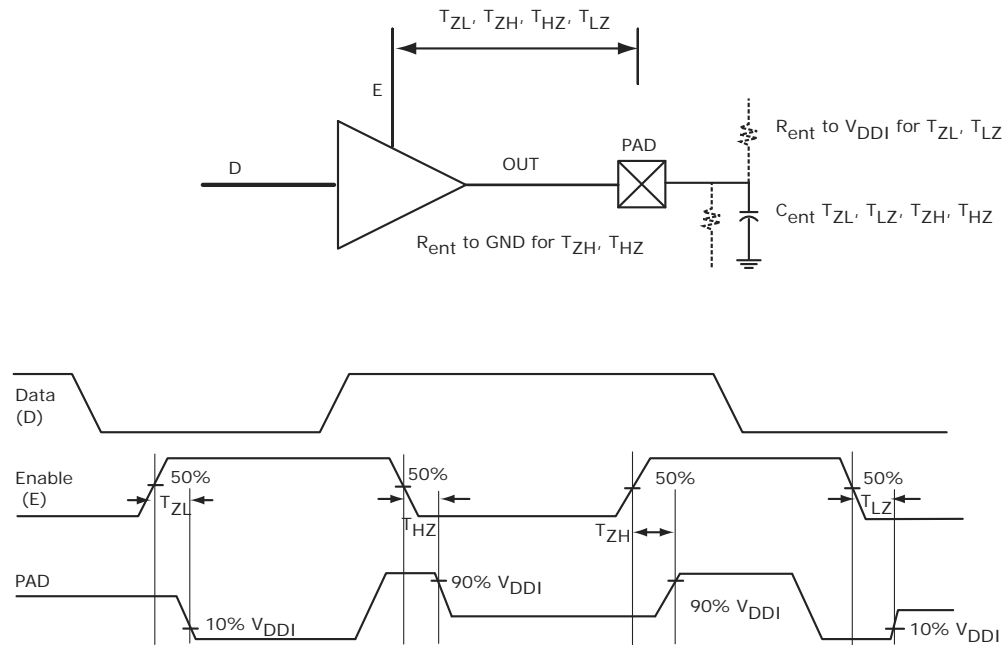
**Table 16 • Average Junction Temperature and Voltage Derating Factors for Fabric Timing Delays**

Array Voltage $V_{DD}$ (V)	$-40\text{ }^{\circ}\text{C}$	$0\text{ }^{\circ}\text{C}$	$25\text{ }^{\circ}\text{C}$	$70\text{ }^{\circ}\text{C}$	$85\text{ }^{\circ}\text{C}$	$100\text{ }^{\circ}\text{C}$
1.14	0.83	0.89	0.92	0.98	<b>1.00</b>	1.02
1.2	0.75	0.80	0.83	0.89	0.91	0.93
1.26	0.69	0.73	0.76	0.81	0.83	0.85

### 2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

**Figure 5 • Tristate Buffer for Enable Path Test Point**



### 2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

**Table 18 • Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	630			Mbps
LVTTL 3.3 V	600			Mbps
LVC MOS 3.3 V	600			Mbps
LVC MOS 2.5 V	410	420	400	Mbps
LVC MOS 1.8 V	295	400	400	Mbps
LVC MOS 1.5 V	160	220	235	Mbps
LVC MOS 1.2 V	120	160	200	Mbps
LPDDR-LVC MOS 1.8 V mode			400	Mbps

**Table 22 • Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
LPDDR			200	MHz
HSTL1.5 V			200	MHz
SSTL 2.5 V	255	350	200	MHz
SSTL 1.8 V			334	MHz
SSTL 1.5 V			334	MHz

**Table 23 • Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	Unit
LVPECL (input only)	450		MHz
LVDS 3.3 V	267.5		MHz
LVDS 2.5 V	267.5	350	MHz
RSDS	260	350	MHz
BLVDS	250		MHz
MLVDS	250		MHz
Mini-LVDS	260	350	MHz

## 2.3.5.6 Single-Ended I/O Standards

### 2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

#### 2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 29 • LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	3.15	3.3	3.45	V

**Table 30 • LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}$ (DC)	2.0	3.45	V
DC input logic low	$V_{IL}$ (DC)	-0.3	0.8	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 31 • LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC output logic high <sup>1</sup>	$V_{OH}$	$V_{DDI} - 0.4$		V
DC output logic low <sup>1</sup>	$V_{OL}$		0.4	V

1. The  $V_{OH}/V_{OL}$  test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

**Table 32 • LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC output logic high	$V_{OH}$	2.4		V
DC output logic low	$V_{OL}$		0.4	V

**Table 33 • LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	600	Mbps	AC loading: 17 pF load, maximum drive/slew

**Table 70 • LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**  
(continued)

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
6 mA	Slow	4.244	4.993	3.465	4.076	4.233	4.979	6.39	7.518	5.736	6.748	ns
	Medium	3.774	4.44	3.05	3.587	3.762	4.426	6.114	7.193	5.397	6.35	ns
	Medium fast	3.544	4.17	2.839	3.339	3.529	4.152	5.978	7.033	5.27	6.2	ns
	Fast	3.519	4.14	2.82	3.317	3.504	4.122	5.965	7.017	5.259	6.187	ns
8 mA	Slow	4.099	4.823	3.311	3.894	4.087	4.807	6.584	7.746	5.854	6.888	ns
	Medium	3.656	4.301	2.927	3.443	3.642	4.284	6.311	7.425	5.553	6.533	ns
	Medium fast	3.437	4.044	2.731	3.213	3.42	4.023	6.182	7.273	5.435	6.394	ns
	Fast	3.41	4.012	2.715	3.193	3.393	3.991	6.178	7.269	5.425	6.383	ns
10 mA	Slow	4.029	4.74	3.238	3.809	4.015	4.723	6.732	7.921	5.965	7.018	ns
	Medium	3.601	4.237	2.867	3.372	3.586	4.218	6.473	7.615	5.669	6.669	ns
	Medium fast	3.384	3.981	2.672	3.143	3.365	3.958	6.351	7.471	5.55	6.529	ns
	Fast	3.357	3.949	2.655	3.123	3.338	3.927	6.345	7.464	5.54	6.518	ns
12 mA	Slow	3.974	4.675	3.196	3.759	3.958	4.656	6.842	8.049	6.068	7.139	ns
	Medium	3.55	4.176	2.827	3.326	3.534	4.157	6.584	7.746	5.751	6.766	ns
	Medium fast	3.345	3.935	2.638	3.103	3.325	3.911	6.488	7.633	5.641	6.637	ns
	Fast	3.316	3.902	2.621	3.083	3.297	3.878	6.486	7.63	5.626	6.619	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 71 • LVCMOS 1.5 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	4.423	5.203	5.397	6.35	5.686	6.69	5.609	6.599	5.561	6.542	ns
4 mA	Slow	4.05	4.765	4.503	5.298	4.92	5.788	7.358	8.657	6.525	7.677	ns
6 mA	Slow	4.081	4.801	4.259	5.012	4.699	5.528	7.659	9.011	6.709	7.893	ns
8 mA	Slow	4.234	4.98	4.068	4.786	4.521	5.319	8.218	9.668	7.05	8.294	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.



**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 3.0\text{ V}$

**Table 91 • PCI/PCIX AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
	-1	-Std	-1	-Std	
None	2.229	2.623	2.238	2.633	ns

**Table 92 • PCI/PCIX AC switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)**

$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.146	2.525	2.043	2.404	2.084	2.452	6.095	7.171	5.558	6.539	ns

**2.3.6 Memory Interface and Voltage Referenced I/O Standards**

This section describes High-Speed Transceiver Logic (HSTL) memory interface and voltage reference I/O standards.

**2.3.6.1 High-Speed Transceiver Logic (HSTL)**

The HSTL standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO2 FPGA and SmartFusion2 SoC FPGA devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification (Applicable to DDRIO Bank Only)**

**Table 93 • HSTL Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	1.425	1.5	1.575	V
Termination voltage	$V_{TT}$	0.698	0.750	0.803	V
Input reference voltage	$V_{REF}$	0.698	0.750	0.803	V

**Table 94 • HSTL DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}$ (DC)	$V_{REF} + 0.1$	1.575	V
DC input logic low	$V_{IL}$ (DC)	-0.3	$V_{REF} - 0.1$	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 112 • SSTL2 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

	On-Die Termination (ODT)	T <sub>PY</sub>		Unit
		-1	-Std	
Pseudo differential	None	2.798	3.293	ns
True differential	None	2.733	3.215	ns

**Table 113 • DDR1/SSTL2 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

	On-Die Termination (ODT)	T <sub>PY</sub>		Unit
		-1	-Std	
Pseudo differential	None	2.476	2.913	ns
True differential	None	2.475	2.911	ns

**Table 114 • SSTL2 Class I Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub>		T <sub>LZ</sub>		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.26	2.66	1.99	2.341	1.985	2.335	2.135	2.512	2.13	2.505	ns
Differential	2.26	2.658	2.202	2.591	2.201	2.589	2.393	2.815	2.392	2.814	ns

**Table 115 • DDR1/SSTL2 Class I Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub>		T <sub>LZ</sub>		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.055	2.417	2.037	2.396	2.03	2.388	2.068	2.433	2.061	2.425	ns
Differential	2.192	2.58	2.434	2.864	2.425	2.852	2.164	2.545	2.156	2.536	ns

**Table 116 • DDR1/SSTL2 Class I Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)**

	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub>		T <sub>LZ</sub>		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	1.512	1.779	1.462	1.72	1.462	1.72	1.676	1.972	1.676	1.971	ns
Differential	1.676	1.971	1.774	2.087	1.766	2.077	1.854	2.181	1.845	2.171	ns

**Table 117 • DDR1/SSTL2 Class II Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub>		T <sub>LZ</sub>		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.122	2.497	1.906	2.243	1.902	2.237	2.061	2.424	2.056	2.418	ns
Differential	2.127	2.501	2.042	2.402	2.043	2.403	2.363	2.78	2.365	2.781	ns

### 2.3.6.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 139 • LPDDR DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max
Supply voltage	$V_{DDI}$	1.71	1.8	1.89
Termination voltage	$V_{TT}$	0.838	0.900	0.964
Input reference voltage	$V_{REF}$	0.838	0.900	0.964

**Table 140 • LPDDR DC Input Voltage Specification**

Parameter	Symbol	Min	Max
DC input logic high	$V_{IH}$ (DC)	$0.7 \times V_{DDI}$	1.89
DC input logic low	$V_{IL}$ (DC)	-0.3	$0.3 \times V_{DDI}$
Input current high <sup>1</sup>	$I_{IH}$ (DC)		
Input current low <sup>1</sup>	$I_{IL}$ (DC)		

1. See Table 24, page 22.

**Table 141 • LPDDR DC Output Voltage Specification Reduced Drive**

Parameter	Symbol	Min	Max
DC output logic high	$V_{OH}$	$0.9 \times V_{DDI}$	
DC output logic low	$V_{OL}$		$0.1 \times V_{DDI}$
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	0.1	
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-0.1	

**Table 142 • LPDDR DC Output Voltage Specification Full Drive<sup>1</sup>**

Parameter	Symbol	Min	Max
DC output logic high	$V_{OH}$	$0.9 \times V_{DDI}$	
DC output logic low	$V_{OL}$		$0.1 \times V_{DDI}$
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	0.1	
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-0.1	

1. To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.

**Table 143 • LPDDR DC Differential Voltage Specification**

Parameter	Symbol	Min
DC input differential voltage	$V_{ID}$ (DC)	$0.4 \times V_{DDI}$

### 2.3.7.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 173 • B-LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V

**Table 174 • B-LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	$V_I$	0	2.925	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 175 • B-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	$V_{OH}$	1.25	1.425	1.6	V
DC output logic low	$V_{OL}$	0.9	1.075	1.25	V

**Table 176 • B-LVDS DC Differential Voltage Specification**

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	$V_{OD}$	65	460	mV
Output common mode voltage (for MSIO I/O bank only)	$V_{OCM}$	1.1	1.5	V
Input common mode voltage	$V_{ICM}$	0.05	2.4	V
Input differential voltage	$V_{ID}$	0.1	$V_{DDI}$	V

**Table 177 • B-LVDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	500	Mbps	AC loading: 2 pF / 100 $\Omega$ differential load

**Table 178 • B-LVDS AC Impedance Specifications**

Parameter	Symbol	Typ	Unit
Termination resistance	$R_T$	27	$\Omega$

**Table 179 • B-LVDS AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	Cross point	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF

**Table 185 • M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	$V_{OH}$	1.25	1.425	1.6	V
DC output logic low	$V_{OL}$	0.9	1.075	1.25	V

**Table 186 • M-LVDS Differential Voltage Specification**

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	$V_{OD}$	300	650	mV
Output common mode voltage (for MSIO I/O bank only)	$V_{OCM}$	0.3	2.1	V
Input common mode voltage	$V_{ICM}$	0.3	1.2	V
Input differential voltage	$V_{ID}$	50	2400	mV

**Table 187 • M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	$D_{MAX}$	500	Mbps	AC loading: 2 pF / 100 $\Omega$ differential load

**Table 188 • M-LVDS AC Impedance Specifications**

Parameter	Symbol	Typ	Unit
Termination resistance	$R_T$	50	$\Omega$

**Table 189 • M-LVDS AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	Cross point	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF

**AC Switching Characteristics**

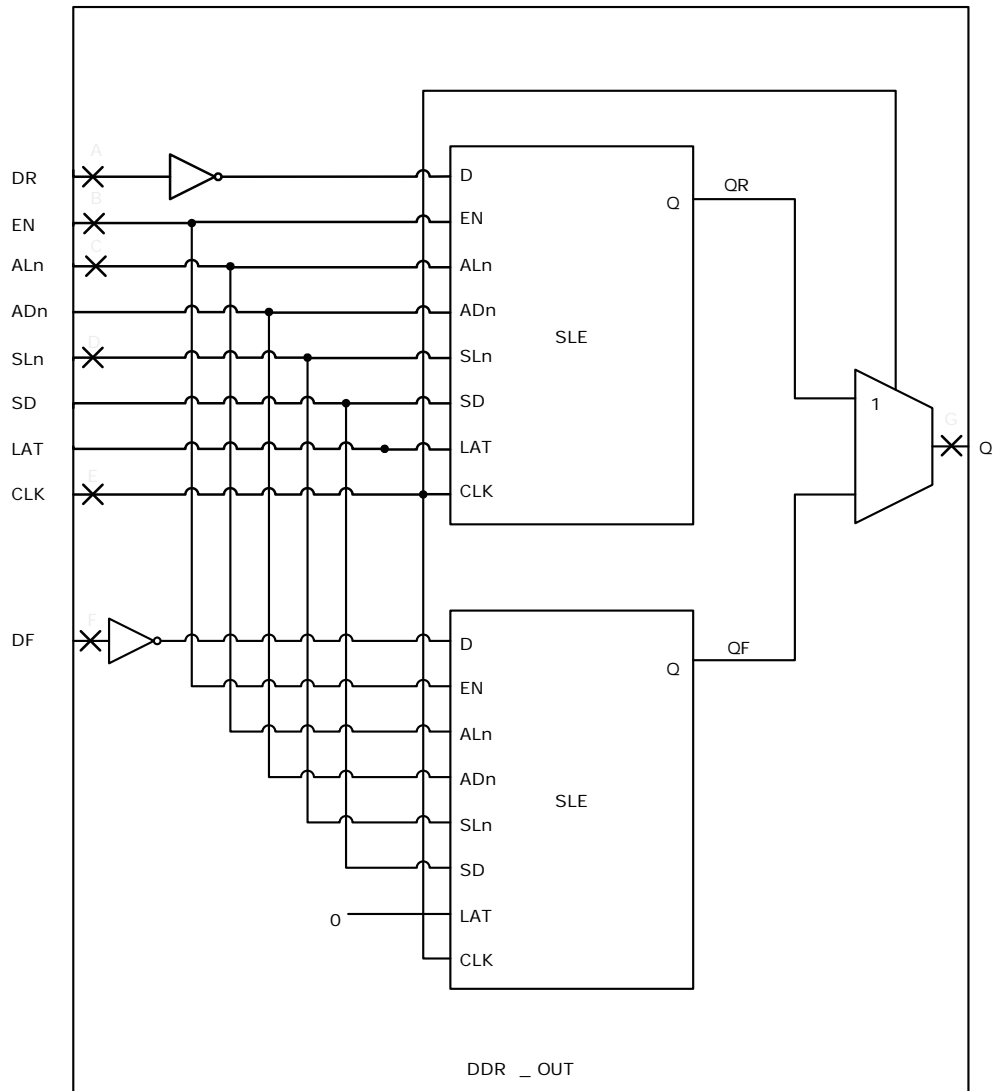
Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

**Table 190 • M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.738	3.221	ns
100	2.735	3.218	ns

**2.3.9.4 Output DDR Module**

**Figure 12 • Output DDR Module**



**Table 238 •  $\mu$ SRAM (RAM64x16) in 64 x 16 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read synchronous reset hold time	$T_{SRSTHD}$	0.061		0.071		ns
Write clock period	$T_{CCY}$	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	$T_{BLKCSU}$	0.404		0.476		ns
Write block hold time	$T_{BLKCHD}$	0.007		0.008		ns
Write input data setup time	$T_{DINCSU}$	0.115		0.135		ns
Write input data hold time	$T_{DINCHD}$	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.026		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

The following table lists the  $\mu$ SRAM in 128 x 9 mode in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 239 •  $\mu$ SRAM (RAM128x9) in 128 x 9 Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	$T_{CY}$	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	$T_{PLCY}$	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	$T_{CLK2Q}$		0.266		0.313	ns
Read access time without pipeline register				1.677		1.973
Read address setup time in synchronous mode	$T_{ADDRSU}$	0.301		0.354		ns
Read address setup time in asynchronous mode			1.856		2.184	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.091		0.107		ns
Read address hold time in asynchronous mode			-0.778		-0.915	
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHD}$	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.036		2.396	ns

**Table 241 •  $\mu$ SRAM (RAM256x4) in 256 x 4 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Write address hold time	$T_{ADDRCHD}$	0.245		0.288		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.03		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

The following table lists the  $\mu$ SRAM in 512 x 2 mode in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 242 •  $\mu$ SRAM (RAM512x2) in 512 x 2 Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	$T_{CY}$	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	$T_{PLCY}$	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	$T_{CLK2Q}$		0.27		0.31	ns
Read access time without pipeline register				1.76		2.08
Read address setup time in synchronous mode	$T_{ADDRSU}$	0.301		0.354		ns
Read address setup time in asynchronous mode			1.96		2.306	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.137		0.161		ns
Read address hold time in asynchronous mode			-0.58		-0.68	
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHD}$	-0.65		-0.77		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.14		2.52	ns
Read asynchronous reset removal time (pipelined clock)	$T_{RSTREM}$	-0.02		-0.03		ns
Read asynchronous reset removal time (non-pipelined clock)			0.046		0.054	
Read asynchronous reset recovery time (pipelined clock)	$T_{RSTREC}$	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)			0.236		0.278	
Read asynchronous reset to output propagation delay (with pipelined register enabled)	$T_{R2Q}$		0.83		0.98	ns
Read synchronous reset setup time	$T_{SRSTSU}$	0.271		0.319		ns
Read synchronous reset hold time	$T_{SRSTHD}$	0.061		0.071		ns



**Table 259 • 2 Step IAP Programming (Fabric Only)**

M2S/M2GL Device	Image size		Authenticate	Program	Verify	Unit
	Bytes					
005	302672	4	39	6	Sec	
010	568784	7	45	12	Sec	
025	1223504	14	55	23	Sec	
050	2424832	29	74	40	Sec	
060	2418896	39	83	50	Sec	
090	3645968	60	106	73	Sec	
150	6139184	100	154	120	Sec	

**Table 260 • 2 Step IAP Programming (eNVM Only)**

M2S/M2GL Device	Image size		Authenticate	Program	Verify	Unit
	Bytes					
005	137536	2	59	5	Sec	
010	274816	4	98	11	Sec	
025	274816	4	100	10	Sec	
050	2,78,528	3	107	9	Sec	
060	268480	5	98	22	Sec	
090	544496	10	174	43	Sec	
150	544496	10	175	44	Sec	

**Table 261 • 2 Step IAP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size		Authenticate	Program	Verify	Unit
	Bytes					
005	439296	6	78	11	Sec	
010	842688	11	122	21	Sec	
025	1497408	19	135	32	Sec	
050	2695168	32	158	48	Sec	
060	2686464	43	159	70	Sec	
090	4190208	68	258	115	Sec	
150	6682768	109	308	162	Sec	

## 2.3.16 SRAM PUF

For more details on static random-access memory (SRAM) physical unclonable functions (PUF) services, see *AC434: Using SRAM PUF System Service in SmartFusion2 Application Note*.

The following table lists the SRAM PUF in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 274 • SRAM PUF**

Service	PUF Off		PUF On		Unit
	Typ	Max	Typ	Max	
Create activation code	709.1	746.4	754.4	762.5	ms
Delete activation code	1329.3	1399.3	1414.1	1429.3	ms
Create intrinsic keycode	656.6	691.1	698.5	706.0	ms
Create extrinsic keycode	656.6	691.1	698.5	706.0	ms
Get number of keys	1.3	1.4	1.4	1.4	ms
Export (Kc0, Kc1)	998.0	1050.5	1061.7	1073.1	ms
Export 2 keycodes	2020.2	2126.5	2149.2	2172.3	ms
Export 4 keycodes	3065.7	3227.0	3261.3	3296.4	ms
Export 8 keycodes	5101.0	5369.5	5426.6	5485.0	ms
Export 16 keycodes	9212.1	9697.0	9800.1	9905.5	ms
Import (Kc0, Kc1)	39.7	41.8	42.2	42.7	ms
Import 2 keycodes	50.1	52.7	53.3	53.9	ms
Import 4 keycodes	60.6	63.8	64.5	65.2	ms
Import 8 keycodes	80.9	85.1	86.1	87.0	ms
Import 16 keycodes	123.8	130.4	131.7	133.2	ms
Delete keycode	552.5	581.6	587.8	594.1	ms
Fetch key	31.4	33.0	33.4	33.7	ms
Fetch ecc key	20.0	21.1	21.3	21.5	ms
Get seed	2.0	2.1	2.2	2.2	ms

**Table 277 • Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz) (continued)**

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Startup time (with regard to stable oscillator output)	SUXTAL			0.8	ms	005, 010, 025, and 050 devices
				1.0	ms	090 and 150 devices

**Table 278 • Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)**

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		2		MHz	
Accuracy	ACCXTAL			0.00105	%	050 devices
				0.003	%	005, 010, 025, 090, and 150 devices
				0.004	%	060 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		1	5	ns	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		1	5	ns	
Operating current	IDYNXTAL		0.3		mA	
Input logic level high	VIHXTAL	0.9 V <sub>PP</sub>			V	
Input logic level low	VILXTAL			0.1 V <sub>PP</sub>	V	
Startup time (with regard to stable oscillator output)	SUXTAL			4.5	ms	010 and 050 devices
				5	ms	005 and 025 devices
				7	ms	090 and 150 devices

**Table 279 • Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)**

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		32		kHz	
Accuracy	ACCXTAL			0.004	%	005, 010, 025, 050, 060, and 090 devices
				0.005	%	150 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		150	300	ns	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		150	300	ns	
Operating current	IDYNXTAL		0.044		mA	010 and 050 devices
			0.060		mA	005, 025, 060, 090, and 150 devices
Input logic level high	VIHXTAL	0.9 V <sub>PP</sub>			V	
Input logic level low	VILXTAL			0.1 V <sub>PP</sub>	V	
Startup time (with regard to stable oscillator output)	SUXTAL			115	ms	005, 025, 050, 090, and 150 devices
				126	ms	010 devices

### 2.3.31.2 SmartFusion2 Inter-Integrated Circuit (I<sup>2</sup>C) Characteristics

This section describes the DC and switching of the I<sup>2</sup>C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, see Figure 21, page 125.

The following table lists the I<sup>2</sup>C characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$

**Table 303 • I<sup>2</sup>C Characteristics**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input low voltage	$V_{IL}$	-0.3		0.8	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive.
Input high voltage	$V_{IH}$	2		3.45	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive.
Hysteresis of schmitt triggered inputs for $V_{DDI} > 2\text{ V}$	$V_{HYS}$	$0.05 \times V_{DDI}$			V	See Table 28, page 23 for more information.
Input current high	$I_{IL}$			10	$\mu\text{A}$	See Single-Ended I/O Standards, page 24 for more information.
Input current low	$I_{IH}$			10	$\mu\text{A}$	See Single-Ended I/O Standards, page 24 for more information.
Input rise time	$T_{ir}$			1000	ns	Standard mode
				300	ns	Fast mode
Input fall time	$T_{if}$			300	ns	Standard mode
				300	ns	Fast mode
Maximum output voltage low (open drain) at 3 mA sink current for $V_{DDI} > 2\text{ V}$	$V_{OL}$			0.4	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive.
Pin capacitance	$C_{in}$			10	pF	$V_{IN} = 0$ , $f = 1.0\text{ MHz}$
Output fall time from $V_{IHMin}$ to $V_{ILMax}^1$	$t_{OF}^1$		21.04		ns	$V_{IHmin}$ to $V_{ILMax}$ , $C_{LOAD} = 400\text{ pF}$
			5.556		ns	$V_{IHmin}$ to $V_{ILMax}$ , $C_{LOAD} = 100\text{ pF}$
Output rise time from $V_{ILMax}$ to $V_{IHMin}^1$	$t_{OR}^1$		19.887		ns	$V_{ILMax}$ to $V_{IHmin}$ , $C_{LOAD} = 400\text{ pF}$
			5.218		ns	$V_{ILMax}$ to $V_{IHmin}$ , $C_{LOAD} = 100\text{ pF}$
Output buffer maximum pull-down resistance <sup>2,3</sup>	$R_{pull-up}^{2,3}$			50	$\Omega$	
Output buffer maximum pull-up resistance <sup>2,4</sup>	$R_{pull-down}^{2,4}$			131.25	$\Omega$	

**Table 310 • SPI Characteristics for All Devices (continued)**

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPI master configuration (applicable for 060, 090, and 150 devices)						
sp6m	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 7.0			ns	
sp7m	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 9.5			ns	
sp8m	SPI_[0 1]_DI setup time <sup>2</sup>	15			ns	
sp9m	SPI_[0 1]_DI hold time <sup>2</sup>	–2.5			ns	
SPI slave configuration (applicable for 060, 090, and 150 devices)						
sp6s	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 16.0			ns	
sp7s	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 3.5			ns	
sp8s	SPI_[0 1]_DI setup time <sup>2</sup>	3			ns	
sp9s	SPI_[0 1]_DI hold time <sup>2</sup>	2.5			ns	

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. For allowable pclk configurations, see the Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

**Figure 23 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**

