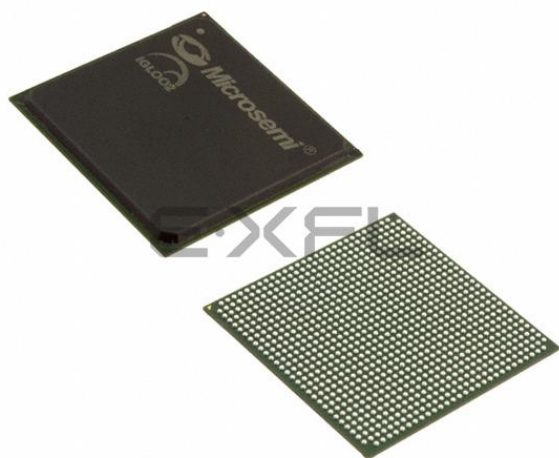




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Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	56340
Total RAM Bits	1869824
Number of I/O	377
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl050ts-fgg896i

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2.3.2 Power Consumption

The following sections describe the power consumptions of the devices.

2.3.2.1 Quiescent Supply Current

Table 10 • Quiescent Supply Current Characteristics

Power Supplies/Blocks	Modes and Configurations	
	Non-Flash*Freeze	Flash*Freeze
FPGA Core	On	Off
V _{DD} /SERDES_[01]_VDD ¹	On	On
V _{PP} /V _{PPNVM}	On	On
HPMS_MDDR_PLL_VDDA/FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA/PLL0_PLL1_HPMS_MDDR_VDD A	0 V	0 V
SERDES_[01]_PLL_VDDA ²	0 V	0 V
SERDES_[01]_L[0123]_VDDAPLL/VDD_2V5 ²	On	On
SERDES_[01]_L[0123]_VDDAIIO ²	On	On
V _{DDI_x} ^{3, 4}	On	On
V _{REFx}	On	On
MSSDDR CLK	32 kHz	32 kHz
RAM	On	Sleep state
System controller	50 MHz	50 MHz
50 MHz oscillator (enable/disable)	Enable	Disabled
1 MHz oscillator (enable/disable)	Disabled	Disabled
Crystal oscillator (enable/disable)	Disabled	Disabled

1. SERDES_[01]_VDD Power Supply is shorted to V_{DD}.
2. SerDes and DDR blocks to be unused.
3. V_{DDI_x} has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate V_{DDI} bank supplies. For details on bank power supplies, see "Recommendation for Unused Bank Supplies" table in the AC393: *SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.
4. No Differential (that is to say, LVDS) I/Os or ODT attributes to be used.

Table 11 • SmartFusion2 and IGLOO2 Quiescent Supply Current (V_{DD} = 1.2 V) – Typical Process

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC1	Non-Flash*Freeze	6.2	6.9	8.9	13.1	15.3	15.4	27.5	mA	Typical (T _J = 25 °C)
		24.0	28.4	40.6	67.8	80.6	81.4	144.7	mA	Commercial (T _J = 85 °C)
		35.2	41.9	60.5	102.1	121.4	122.6	219.1	mA	Industrial (T _J = 100 °C)

Table 11 • SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD} = 1.2$ V) – Typical Process

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC2	Flash*Freeze	1.4	2.6	3.7	5.1	5.0	5.1	8.9	mA	Typical ($T_J = 25$ °C)
		12.0	20.0	26.6	35.3	35.4	35.7	57.8	mA	Commercial ($T_J = 85$ °C)
		18.5	30.8	41.0	54.5	54.5	55.0	89.0	mA	Industrial ($T_J = 100$ °C)

Table 12 • SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD} = 1.26$ V) – Worst-Case Process

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC1	Non-Flash*Freeze	43.8	57.0	84.6	132.3	161.4	163.0	242.5	mA	Commercial ($T_J = 85$ °C)
		65.3	85.7	127.8	200.9	245.4	247.8	369.0	mA	Industrial ($T_J = 100$ °C)
IDC2	Flash*Freeze	29.1	45.6	51.7	62.7	69.3	70.0	84.8	mA	Commercial ($T_J = 85$ °C)
		44.9	70.3	79.7	96.5	106.8	107.8	130.6	mA	Industrial ($T_J = 100$ °C)

2.3.2.2 Programming Currents

The following tables represent programming, verify and Inrush currents for SmartFusion2 SoC and IGLOO2 FPGA devices.

Table 13 • Currents During Program Cycle, 0 °C $\leq T_J \leq 85$ °C – Typical Process

Power Supplies	Voltage (V)	005	010	025	050	060	090	150 ¹	Unit
V_{DD}	1.26	46	53	55	58	30	42	52	mA
V_{PP}	3.46	8	11	6	10	9	12	12	mA
V_{PPNVM}	3.46	1	2	2	3	3	3		mA
V_{DDI}	2.62	31	16	17	1	12	12	81	mA
	3.46	62	31	36	1	12	17	84	mA
Number of banks		7	8	8	10	10	9	19	

1. V_{PP} and V_{PPNVM} are internally shorted.

Table 14 • Currents During Verify Cycle, 0 °C $\leq T_J \leq 85$ °C – Typical Process

Power Supplies	Voltage (V)	005	010	025	050	060	090	150 ¹	Unit
V_{DD}	1.26	44	53	55	58	33	41	51	mA
V_{PP}	3.46	6	5	3	15	8	11	12	mA
V_{PPNVM}	3.46	1	0	0	1	1	1		mA
V_{DDI}	2.62	31	16	17	1	12	11	81	mA
	3.46	61	32	36	1	12	17	84	mA
Number of banks		7	8	8	10	10	9	19	

1. V_{PP} and V_{PPNVM} are internally shorted.

2.3.5.6 Single-Ended I/O Standards

2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 29 • LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

Table 30 • LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DC input logic high	V_{IH} (DC)	2.0	3.45	V
DC input logic low	V_{IL} (DC)	−0.3	0.8	V
Input current high ¹	I_{IH} (DC)			
Input current low ¹	I_{IL} (DC)			

1. See Table 24, page 22.

Table 31 • LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DC output logic high ¹	V_{OH}	$V_{DDI} - 0.4$		V
DC output logic low ¹	V_{OL}		0.4	V

1. The V_{OH}/V_{OL} test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

Table 32 • LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	2.4		V
DC output logic low	V_{OL}		0.4	V

Table 33 • LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	600	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 43 • LVCMOS 2.5 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.2	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	$\Omega\sigma$
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 44 • LVCMOS 2.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (With Software Default Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	4 mA	4 mA	$V_{DDI} - 0.4$	0.4	4	4
6 mA	6 mA	6 mA	$V_{DDI} - 0.4$	0.4	6	6
8 mA	8 mA	8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	12 mA	12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA		16 mA	$V_{DDI} - 0.4$	0.4	16	16

Note: For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at:
www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 45 • LVCMOS 2.5 V Receiver Characteristics (Input Buffers)

	On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
		-1	-Std	-1	-Std	
LVCMOS 2.5 V (for DDRIO I/O bank)	None	1.823	2.145	1.932	2.274	ns
LVCMOS 2.5 V (for MSIO I/O bank)	None	2.486	2.925	2.495	2.935	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	None	2.29	2.694	2.305	2.712	ns

Table 46 • LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.657	4.302	3.393	3.991	3.675	4.323	3.894	4.582	3.552	4.18	ns
	Medium	3.374	3.97	3.139	3.693	3.396	3.995	3.635	4.277	3.253	3.828	ns
	Medium fast	3.239	3.811	3.036	3.572	3.261	3.836	3.519	4.141	3.128	3.681	ns
	Fast	3.224	3.793	3.029	3.563	3.246	3.818	3.512	4.132	3.119	3.67	ns

Table 62 • LVCMOS 1.5 V DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC output logic high	VOH	$V_{DDI} \times 0.75$		V
DC output logic low	VOL		$V_{DDI} \times 0.25$	V

Table 63 • LVCMOS 1.5 V AC Minimum and Maximum Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D _{MAX}	235	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D _{MAX}	160	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	D _{MAX}	220	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 64 • LVCMOS 1.5 V AC Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CA L	75, 60, 50, 40	Ω

Table 65 • LVCMOS 1.5 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point	V _{TRIP}	0.75	V
Resistance for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	R _{ENT}	2K	Ω
Capacitive loading for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	C _{ENT}	5	pF
Capacitive loading for data path (T _{DP})	C _{LOAD}	5	pF

Table 66 • LVCMOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			V _{OH} (V)	V _{OL} (V)	IOH (at V _{OH}) mA	IOL (at V _{OL}) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	2	2
4 mA	4 mA	4 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	4	4
6 mA	6 mA	6 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	6	6
8 mA		8 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	8	8
		10 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	10	10
		12 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	12	12

Note: For a detailed I/V curve, use the corresponding IBIS models:
www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching CharacteristicsWorst commercial-case conditions: $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.425\text{ V}$ **Table 67 • LVCMOS 1.5 V Receiver Characteristics for DDRIO I/O Bank with Fixed Codes (Input Buffers)**

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	2.051	2.413	2.086	2.455	ns

Table 68 • LVCMOS 1.5 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	3.311	3.896	3.285	3.865	ns
50	3.654	4.299	3.623	4.263	ns
75	3.533	4.156	3.501	4.119	ns
150	3.415	4.018	3.388	3.986	ns

Table 69 • LVCMOS 1.5 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	2.959	3.481	2.93	3.447	ns
50	3.298	3.88	3.268	3.845	ns
75	3.162	3.719	3.128	3.68	ns
150	3.053	3.592	3.021	3.554	ns

Table 70 • LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	5.122	6.026	4.31	5.07	5.145	6.052	5.258	6.186	4.672	5.496	ns
	Medium	4.58	5.389	3.86	4.54	4.6	5.411	4.977	5.855	4.357	5.126	ns
	Medium fast	4.323	5.086	3.629	4.269	4.341	5.107	4.804	5.652	4.228	4.974	ns
	Fast	4.296	5.054	3.609	4.245	4.314	5.075	4.791	5.636	4.219	4.963	ns
4 mA	Slow	4.449	5.235	3.707	4.361	4.443	5.227	6.058	7.127	5.458	6.421	ns
	Medium	3.961	4.66	3.264	3.839	3.954	4.651	5.778	6.797	5.116	6.018	ns
	Medium fast	3.729	4.387	3.043	3.579	3.72	4.376	5.63	6.624	4.981	5.86	ns
	Fast	3.704	4.358	3.027	3.56	3.695	4.347	5.624	6.617	4.973	5.851	ns

2.3.6.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 103 • DDR1/SSTL2 DC Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V
Termination voltage	V_{TT}	1.164	1.250	1.339	V
Input reference voltage	V_{REF}	1.164	1.250	1.339	V

Table 104 • DDR1/SSTL2 DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input logic high	V_{IH} (DC)	$V_{REF} + 0.15$	2.625	V
DC input logic low	V_{IL} (DC)	-0.3	$V_{REF} - 0.15$	V
Input current high ¹	I_{IH} (DC)			
Input current low ¹	I_{IL} (DC)			

1. See Table 24, page 22.

Table 105 • DDR1/SSTL2 DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
SSTL2 Class I (DDR Reduced Drive)				
DC output logic high	V_{OH}	$V_{TT} + 0.608$		V
DC output logic low	V_{OL}		$V_{TT} - 0.608$	V
Output minimum source DC current	I_{OH} at V_{OH}	8.1		mA
Output minimum sink current	I_{OL} at V_{OL}	-8.1		mA
SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Bank Only				
DC output logic high	V_{OH}	$V_{TT} + 0.81$		V
DC output logic low	V_{OL}		$V_{TT} - 0.81$	V
Output minimum source DC current	I_{OH} at V_{OH}	16.2		mA
Output minimum sink current	I_{OL} at V_{OL}	-16.2		mA

Table 106 • DDR1/SSTL2 DC Differential Voltage Specification

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID} (DC)	0.3	V

Table 107 • SSTL2 AC Differential Voltage Specifications

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	$V_{DIFF} (AC)$	0.7		V
AC differential cross point voltage	$V_x (AC)$	$0.5 \times V_{DDI} - 0.2$	$0.5 \times V_{DDI} + 0.2$	V

Table 108 • SSTL2 Minimum and Maximum AC Switching Speeds

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	400	Mbps	AC loading: per JEDEC specifications
Maximum data rate (for MSIO I/O bank)	D_{MAX}	575	Mbps	AC loading: 17pF load
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	700	Mbps	AC loading: 3 pF / 50 Ω load
		510	Mbps	AC loading: 17pF load

Table 109 • SSTL2 AC Impedance Specifications

Parameter	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	20, 42	Ω	Reference resistor = 150 Ω

Table 110 • DDR1/SSTL2 AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.25	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for SSTL2 Class I (T_{DP})	RTT_TEST	50	Ω
Reference resistance for data test path for SSTL2 Class II (T_{DP})	RTT_TEST	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 111 • SSTL2 Receiver Characteristics for DDRIO I/O Bank (Input Buffers)

		T_{PY}		Unit
	On-Die Termination (ODT)	-1	-Std	
Pseudo differential	None	1.549	1.821	ns
True differential	None	1.589	1.87	ns

2.3.7.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 173 • B-LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V

Table 174 • B-LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	2.925	V
Input current high ¹	I_{IH} (DC)			
Input current low ¹	I_{IL} (DC)			

1. See Table 24, page 22.

Table 175 • B-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 176 • B-LVDS DC Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	V_{OD}	65	460	mV
Output common mode voltage (for MSIO I/O bank only)	V_{OCM}	1.1	1.5	V
Input common mode voltage	V_{ICM}	0.05	2.4	V
Input differential voltage	V_{ID}	0.1	V_{DDI}	V

Table 177 • B-LVDS Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	500	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 178 • B-LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	27	Ω

Table 179 • B-LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

2.3.7.5 RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

Minimum and Maximum Input and Output Levels

Table 203 • RSDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V

Table 204 • RSDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	2.925	V

Table 205 • RSDS DC Output Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 206 • RSDS Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing	V_{OD}	100	600	mV
Output common mode voltage	V_{OCM}	0.5	1.5	V
Input common mode voltage	V_{ICM}	0.3	1.5	V
Input differential voltage	V_{ID}	100	600	mV

Table 207 • RSDS Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	520	Mbps	AC loading: 2 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	700	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 208 • RSDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	100	Ω

Table 209 • RSDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

The following table lists the input data register propagation delays in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 219 • Input Data Register Propagation Delays

Parameter	Symbol	Measuring Nodes (from, to) ¹	-1	-Std	Unit
Bypass delay of the input register	T_{IBYP}	F, G	0.353	0.415	ns
Clock-to-Q of the input register	T_{ICLKQ}	E, G	0.16	0.188	ns
Data setup time for the input register	T_{ISUD}	A, E	0.357	0.421	ns
Data hold time for the input register	T_{IHD}	A, E	0	0	ns
Enable setup time for the input register	T_{ISUE}	B, E	0.46	0.542	ns
Enable hold time for the input register	T_{IHE}	B, E	0	0	ns
Synchronous load setup time for the input register	T_{ISUSL}	D, E	0.46	0.542	ns
Synchronous load hold time for the input register	T_{IHSL}	D, E	0	0	ns
Asynchronous clear-to-Q of the input register (ADn=1)	T_{IALN2Q}	C, G	0.625	0.735	ns
Asynchronous preset-to-Q of the input register (ADn=0)		C, G	0.587	0.69	ns
Asynchronous load removal time for the input register	$T_{IREMALN}$	C, E	0	0	ns
Asynchronous load recovery time for the input register	$T_{IRECALN}$	C, E	0.074	0.087	ns
Asynchronous load minimum pulse width for the input register	T_{IWALN}	C, C	0.304	0.357	ns
Clock minimum pulse width high for the input register	$T_{ICKMPWH}$	E, E	0.075	0.088	ns
Clock minimum pulse width low for the input register	$T_{ICKMPWL}$	E, E	0.159	0.187	ns

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

2.3.8.2 Output/Enable Register

Figure 8 • Timing Model for Output/Enable Register

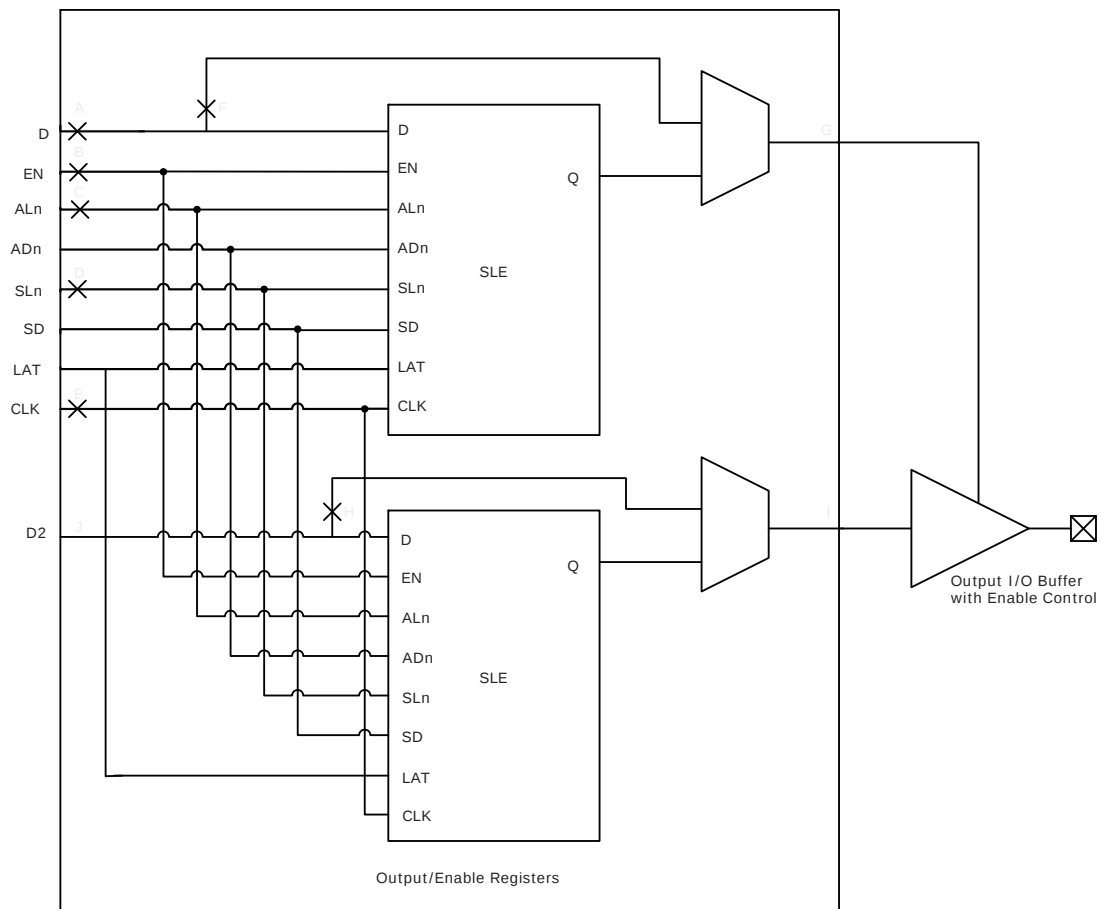
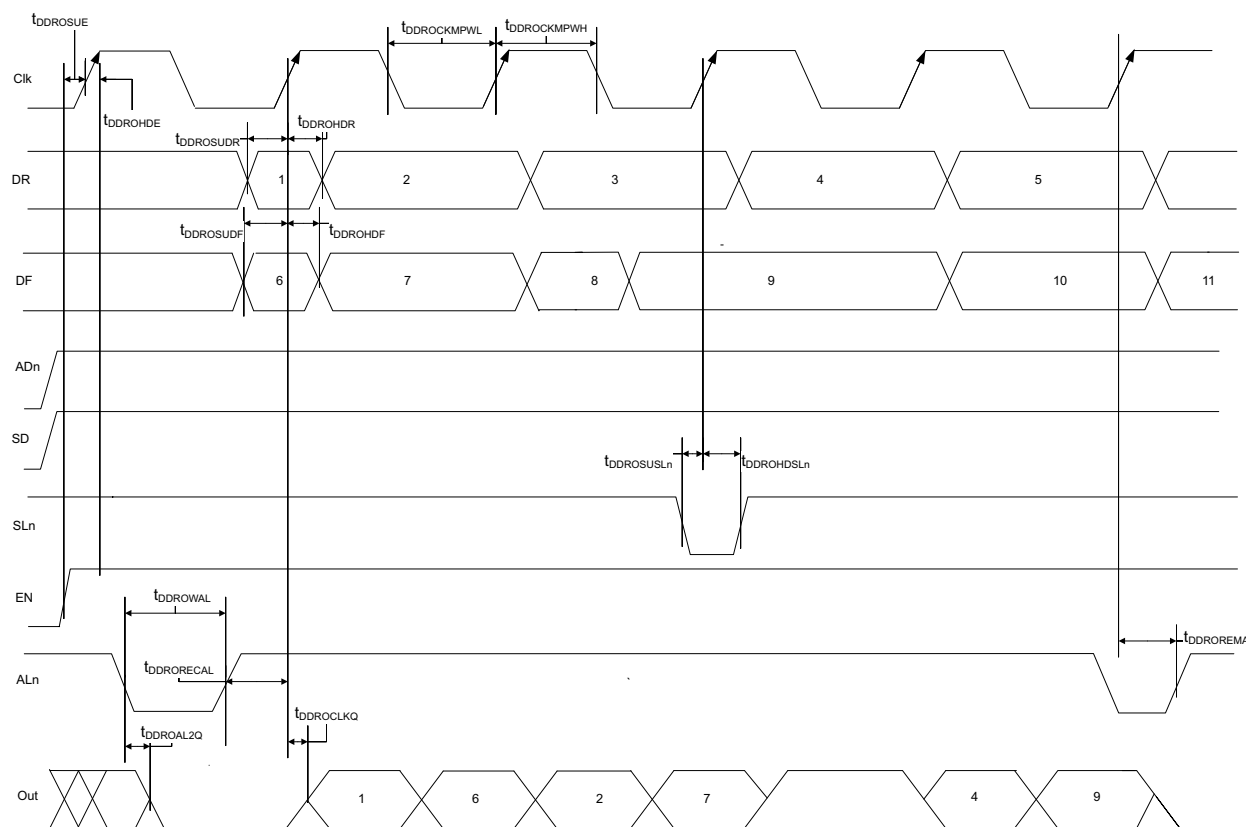


Table 221 • Input DDR Propagation Delays (continued)

Symbol	Description	Measuring Nodes (from, to)	–1	–Std	Unit
T _{DDRIWAL}	Asynchronous load minimum pulse width for input DDR	F, F	0.304	0.357	ns
T _{DDRICKMPWH}	Clock minimum pulse width high for input DDR	B, B	0.075	0.088	ns
T _{DDRICKMPWL}	Clock minimum pulse width low for input DDR	B, B	0.159	0.187	ns

Figure 13 • Output DDR Timing Diagram



2.3.9.5 Timing Characteristics

The following table lists the output DDR propagation delays in worst commercial-case conditions when $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 222 • Output DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	–1	–Std	Unit
T _{DDROCLKQ}	Clock-to-out of DDR for output DDR	E, G	0.263	0.309	ns
T _{DDROSUDF}	Data_F data setup for output DDR	F, E	0.143	0.168	ns
T _{DDROSUDR}	Data_R data setup for output DDR	A, E	0.19	0.223	ns
T _{DDROHDF}	Data_F data hold for output DDR	F, E	0	0	ns
T _{DDROHDR}	Data_R data hold for output DDR	A, E	0	0	ns
T _{DDROSUE}	Enable setup for input DDR	B, E	0.419	0.493	ns
T _{DDROHE}	Enable hold for input DDR	B, E	0	0	ns
T _{DDROSUSLN}	Synchronous load setup for input DDR	D, E	0.196	0.231	ns
T _{DDROHSLN}	Synchronous load hold for input DDR	D, E	0	0	ns
T _{DDROAL2Q}	Asynchronous load-to-out for output DDR	C, G	0.528	0.621	ns
T _{DDROREMA}	Asynchronous load removal time for output DDR	C, E	0	0	ns
T _{DDRORECA}	Asynchronous load recovery time for output DDR	C, E	0.034	0.04	ns

Table 238 • μ SRAM (RAM64x16) in 64 × 16 Mode (continued)

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	-0.026		-0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 128 × 9 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 239 • μ SRAM (RAM128x9) in 128 × 9 Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		-0.778		-0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns

The following table lists the programming times in worst-case conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 256 • JTAG Programming (Fabric Only)

M2S/M2GL Device	Image size		Program	Verify	Unit
	Bytes				
005	302672	44	10	Sec	
010	568784	50	18	Sec	
025	1223504	73	26	Sec	
050	2424832	88	54	Sec	
060	2418896	99	54	Sec	
090	3645968	135	126	Sec	
150	6139184	177	193	Sec	

Table 257 • JTAG Programming (eNVM Only)

M2S/M2GL Device	Image size		Program	Verify	Unit
	Bytes				
005	137536	61	4	Sec	
010	274816	100	9	Sec	
025	274816	100	9	Sec	
050	2,78,528	106	8	Sec	
060	268480	98	8	Sec	
090	544496	176	15	Sec	
150	544496	177	15	Sec	

Table 258 • JTAG Programming (Fabric and eNVM)

M2S/M2GL Device	Image size		Program	Verify	Unit
	Bytes				
005	439296	71	11	Sec	
010	842688	129	20	Sec	
025	1497408	142	35	Sec	
050	2695168	184	59	Sec	
060	2686464	180	70	Sec	
090	4190208	288	147	Sec	
150	6682768	338	231	Sec	

2.3.17 Non-Deterministic Random Bit Generator (NRBG) Characteristics

For more information about NRBG, see *AC407: Using NRBG Services in SmartFusion2 and IGLOO2 Devices Application Note*. The following table lists the NRBG in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 275 • Non-Deterministic Random Bit Generator (NRBG)

Service	Timing	Unit	Conditions	
			Prediction Resistance	Additional Input
Instantiate	85	ms	OFF	X
Generate (after Instantiate) ¹	4.5 ms + (6.25 us/byte x No. of Bytes)		OFF	0
	6.0 ms + (6.25 us/byte x No. of Bytes)		OFF	64
	7.0 ms + (6.25 us/byte x No. of Bytes)		OFF	128
Generate (after Instantiate)	47	ms	ON	X
Generate (subsequent) ¹	0.5 ms + (6.25 us/byte x No. of Bytes)		OFF	0
	2.0 ms + (6.25 us/byte x No. of Bytes)		OFF	64
	3.0 ms + (6.25 us/byte x No. of Bytes)		OFF	128
Generate (subsequent)	43	ms	ON	X
Reseed	40	ms		
Uninstantiate	0.16	ms		
Reset	0.10	ms		
Self test	20	ms	First time after power-up	
	6	ms	Subsequent	

1. If PUF_OFF, generate will incur additional PUF delay time for consecutive service calls.

2.3.18 Cryptographic Block Characteristics

For more information about cryptographic block and associated services, see *AC410: Using AES System Services in SmartFusion2 and IGLOO2 Devices Application Note* and *AC432: Using SHA-256 System Services in SmartFusion2 and IGLOO2 Devices Application Note*.

The following table lists the cryptographic block characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 276 • Cryptographic Block Characteristics

Service	Conditions	Timing	Unit
Any service	First certificate check penalty at boot	11.5	ms
AES128/256 (encoding / decoding) ¹	100 blocks up to 64k blocks	700	kbps

2.3.24 Power-up to Functional Times

The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 288 • Power-up to Functional Times for SmartFusion2

Symbol	From	To	Description	Maximum Power-up to Functional Time for SmartFusion2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	647	500	531	483	474	524	647
$T_{POR2MSSRST}$	POWER_ON_RESET_N	MSS_RESE T_N_M2F	Fabric to MSS	644	497	528	480	468	518	641
$T_{MSSRST2OUT}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.6	3.6	3.6	3.4	4.9	4.8	4.8
$T_{VDD2OUT}$	V_{DD}	Output available at I/O	V_{DD} at its minimum threshold level to output	3096	2975	3012	2959	2869	2992	3225
$T_{VDD2POR}$	V_{DD}	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	2476	2487	2496	2486	2406	2563	2602
$T_{VDD2MSSRST}$	V_{DD}	MSS_RESE T_N_M2F	V_{DD} at its minimum threshold level to MSS	3093	2972	3008	2956	2864	2987	3220
$T_{VDD2WPU}$	DEV_RST_N	DDRIO Inbuf weak pull	DEV_RST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEV_RST_N	MSIO Inbuf weak pull	DEV_RST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEV_RST_N	MSIOD Inbuf weak pull	DEV_RST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

Table 305 • SPI Characteristics for All Devices (continued)

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%– 90%) ¹		2.906		ns	IO Configuration: LVCMOS 2.5 V-8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0 1]_DI setup time ²	12			ns	
sp9m	SPI_[0 1]_DI hold time ²	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0 1]_DI setup time ²	2			ns	
sp9s	SPI_[0 1]_DI hold time ²	7			ns	
SPI master configuration (applicable for 060, 090, and 150 devices)						
sp6m	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 7.0			ns	
sp7m	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) – 9.5			ns	
sp8m	SPI_[0 1]_DI setup time ²	15			ns	
sp9m	SPI_[0 1]_DI hold time ²	–2.5			ns	
SPI slave configuration (applicable for 060, 090, and 150 devices)						
sp6s	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 16.0			ns	
sp7s	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) – 3.5			ns	
sp8s	SPI_[0 1]_DI setup time ²	3			ns	
sp9s	SPI_[0 1]_DI hold time ²	2.5			ns	

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. For allowable pclk configurations, see Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.