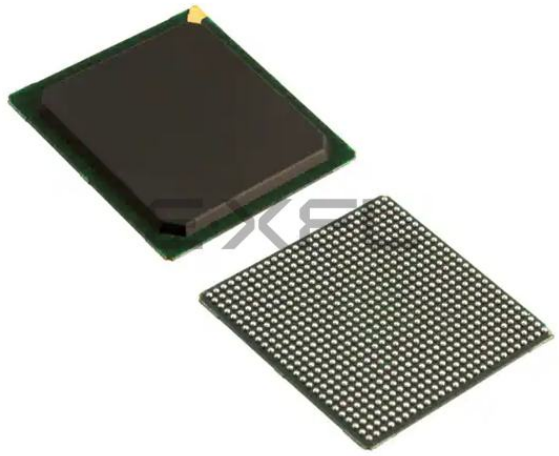

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	56520
Total RAM Bits	1869824
Number of I/O	387
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl060-1fg676i

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- Added Table 244, page 94 and Table 256, page 99 (SAR 73971).
- Updated the SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 71171).
- Added the DEVRST_N Characteristics, page 116 (SAR 64100, 72103).
- Added Table 298, page 122 (SAR 71897).
- Updated Table 25, page 22, Table 26, page 23, and Table 27, page 23 (SAR 74570).
- Added 060 devices in Table 277, page 107, Table 278, page 108, and Table 279, page 108 (SAR 57898).
- Updated duty cycle parameter of crystal in Table 280, page 109 and Table 281, page 109 (SAR 57898).
- Added 32 KHz mode PLL acquisition time in Table 282, page 110 (SAR 68281).
- Updated Table 293, page 119 for 060 devices (SAR 57828).
- Updated Table 297, page 122 for CID value (SAR 70878).

1.4 Revision 8.0

The following is a summary of the changes in revision 8.0 of this document.

- Updated Table 11, page 12 (SAR 69218).
- Updated Table 12, page 13 (SAR 69218).
- Updated Table 283, page 111 (SAR 69000).

1.5 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Updated Table 1, page 4(SAR 68620).

1.6 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- Updated Table 5, page 7 (SAR 65949).
- Updated Table 9, page 10 (SAR 62995).
- Updated Table 123, page 47 and Table 133, page 49 (SAR 67210).
- Added Embedded NVM (eNVM) Characteristics, page 104 (SAR 52509).
- Updated Table 277, page 107 (SAR 64855).
- Updated Table 282, page 110 (SAR 65958 and SAR 56666).
- Added DDR Memory Interface Characteristics, page 120 (SAR 66223).
- Added SFP Transceiver Characteristics, page 120 (SAR 63105).
- Updated Table 302, page 123 and Table 309, page 129 (SAR 66314).

1.7 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Updated Table 1, page 4.
- Updated Table 4, page 6 for T_J symbol information.
- Updated Table 5, page 7 (SAR 63109).
- Updated Table 9, page 10.
- Updated Table 282, page 110 (SAR 62012).
- Added Table 290, page 116 (SAR 64100).
- Added Table 306, page 128, Table 307, page 128 (SAR 50424).

1.8 Revision 4.0

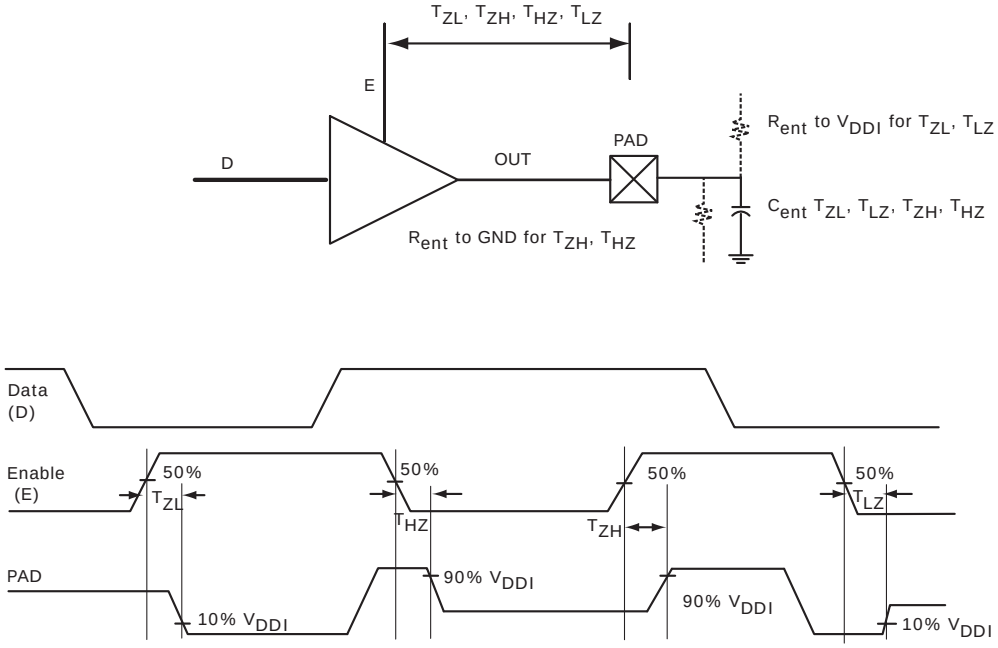
The following is a summary of the changes in revision 4.0 of this document.

- Updated Table 1, page 4. Changed the Status of 090 devices to "Production" (SAR 62750).
- Updated Figure 10, page 70. Removed inverter bubble from DDR_IN latch (SAR 61418).
- Updated SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 62836).

2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

Figure 5 • **Tristate Buffer for Enable Path Test Point**



2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

Table 18 • **Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	630			Mbps
LVTTL 3.3 V	600			Mbps
LVCMOS 3.3 V	600			Mbps
LVCMOS 2.5 V	410	420	400	Mbps
LVCMOS 1.8 V	295	400	400	Mbps
LVCMOS 1.5 V	160	220	235	Mbps
LVCMOS 1.2 V	120	160	200	Mbps
LPDDR-LVCMOS 1.8 V mode			400	Mbps

2.3.5.5 Detailed I/O Characteristics

Table 24 • **Input Capacitance, Leakage Current, and Ramp Time**

Symbol	Description	Maximum	Unit	Conditions
C_{IN}	Input capacitance	10	pF	
I_{IL} (dc)	Input current low (Applicable to HSTL/SSTL inputs only)	400	µA	V_{DDI} = 2.5 V
		500	µA	V_{DDI} = 1.8 V
		600	µA	V_{DDI} = 1.5 V[1]
	Input current low (Applicable to all other digital inputs)	10	µA	
I_{IH} (dc)	Input current high (Applicable to HSTL/SSTL inputs only)	400	µA	V_{DDI} = 2.5 V
		500	µA	V_{DDI} = 1.8 V
		600	µA	V_{DDI} = 1.5 V[1]
	Input current high (Applicable to all other digital inputs)	10	µA	
T_{RAMPIN}[2]	Input ramp time (Applicable to all digital inputs)	50	ns	

1. Applicable when I/O pair is programmed with an HSTL/SSTL I/O type on IOP and an un-terminated I/O type (LVCMOS, for example) on ION pad.
2. Voltage ramp must be monotonic.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of DDRIO I/O bank at V_{OH}/V_{OL} Level.

Table 25 • **I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank**

	R(WEAK PULL-UP) at V_{OH} (Ω)		R(WEAK PULL-DOWN) at V_{OL} (Ω)	
V_{DDI} Domain	Min	Max	Min	Max
2.5 V[1, 2]	10K	17.8K	9.98K	18K
1.8 V[1, 2]	10.3K	19.1K	10.3K	19.5K
1.5 V[1, 2]	10.6K	20.2K	10.6K	21.1K
1.2 V[1, 2]	11.1K	22.7K	11.2K	24.6K

1. R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX).
2. R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN).

Table 43 • **LVCMOS 2.5 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.2	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ωσ
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 44 • **LVCMOS 2.5 V Transmitter Drive Strength Specifications**

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (With Software Default Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	V_{DDI} – 0.4	0.4	2	2
4 mA	4 mA	4 mA	V_{DDI} – 0.4	0.4	4	4
6 mA	6 mA	6 mA	V_{DDI} – 0.4	0.4	6	6
8 mA	8 mA	8 mA	V_{DDI} – 0.4	0.4	8	8
12 mA	12 mA	12 mA	V_{DDI} – 0.4	0.4	12	12
16 mA		16 mA	V_{DDI} – 0.4	0.4	16	16

Note: For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V

Table 45 • **LVCMOS 2.5 V Receiver Characteristics (Input Buffers)**

	On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
		–1	–Std	–1	–Std	
LVCMOS 2.5 V (for DDRIO I/O bank)	None	1.823	2.145	1.932	2.274	ns
LVCMOS 2.5 V (for MSIO I/O bank)	None	2.486	2.925	2.495	2.935	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	None	2.29	2.694	2.305	2.712	ns

Table 46 • **LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		Unit
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	
2 mA	Slow	3.657	4.302	3.393	3.991	3.675	4.323	3.894	4.582	3.552	4.18	ns
	Medium	3.374	3.97	3.139	3.693	3.396	3.995	3.635	4.277	3.253	3.828	ns
	Medium fast	3.239	3.811	3.036	3.572	3.261	3.836	3.519	4.141	3.128	3.681	ns
	Fast	3.224	3.793	3.029	3.563	3.246	3.818	3.512	4.132	3.119	3.67	ns

Table 62 • LVCMOS 1.5 V DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC output logic high	VOH	V_{DDI} × 0.75		V
DC output logic low	VOL		V_{DDI} × 0.25	V

Table 63 • LVCMOS 1.5 V AC Minimum and Maximum Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	235	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D_{MAX}	160	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	220	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 64 • LVCMOS 1.5 V AC Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CAL	75, 60, 50, 40	Ω

Table 65 • LVCMOS 1.5 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point	V_{TRIP}	0.75	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 66 • LVCMOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			V_{OH} (V)	V_{OL} (V)	IOH (at V_{OH})	IOL (at V_{OL})
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max	mA	mA
2 mA	2 mA	2 mA	V_{DDI} × 0.75	V_{DDI} × 0.25	2	2
4 mA	4 mA	4 mA	V_{DDI} × 0.75	V_{DDI} × 0.25	4	4
6 mA	6 mA	6 mA	V_{DDI} × 0.75	V_{DDI} × 0.25	6	6
8 mA		8 mA	V_{DDI} × 0.75	V_{DDI} × 0.25	8	8
		10 mA	V_{DDI} × 0.75	V_{DDI} × 0.25	10	10
		12 mA	V_{DDI} × 0.75	V_{DDI} × 0.25	12	12

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

Table 131 • **SSTL15 DC Output Voltage Specification (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DDR3/SSTL15 Class I (DDR3 Reduced Drive)				
DC output logic high	V_{OH}	0.8 × V_{DDI}		V
DC output logic low	V_{OL}		0.2 × V_{DDI}	V
Output minimum source DC current	I_{OH} at V_{OH}	6.5		mA
Output minimum sink current	I_{OL} at V_{OL}	–6.5		mA
DDR3/SSTL15 Class II (DDR3 Full Drive)				
DC output logic high	V_{OH}	0.8 × V_{DDI}		V
DC output logic low	V_{OL}		0.2 × V_{DDI}	V
Output minimum source DC current	I_{OH} at V_{OH}	7.6		mA
Output minimum sink current	I_{OL} at V_{OL}	–7.6		mA

Table 132 • **SSTL15 DC Differential Voltage Specification (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID}	0.2	V

Note: To meet JEDEC electrical compliance, use DDR3 full drive transmitter.

Table 133 • **SSTL15 AC SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF} (AC)	0.3		V
AC differential cross point voltage	V_x (AC)	0.5 × V_{DDI} – 0.150	0.5 × V_{DDI} + 0.150	V

Table 134 • **SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	667	Mbps	AC loading: per JEDEC specifications

Table 135 • **SSTL15 AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	R_{REF}	34, 40	Ω	Reference resistor = 240 Ω
Effective impedance value (ODT)	R_{TT}	20, 30, 40, 60, 120	Ω	Reference resistor = 240 Ω

Table 156 • LPDDR-LVCMOS 1.8 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.9	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 157 • LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification for DDRIO Bank

Output Drive Selection	V_{OH} (V) Min	V_{OL} (V) Max	I_{OH} (at V_{OH}) mA	I_{OL} (at V_{OL}) mA
2 mA	V_{DDI} – 0.45	0.45	2	2
4 mA	V_{DDI} – 0.45	0.45	4	4
6 mA	V_{DDI} – 0.45	0.45	6	6
8 mA	V_{DDI} – 0.45	0.45	8	8
10 mA	V_{DDI} – 0.45	0.45	10	10
12 mA	V_{DDI} – 0.45	0.45	12	12
16 mA[1]	V_{DDI} – 0.45	0.45	16	16

1. 16 mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance.

Table 158 • LPDDR-LVCMOS 1.8V AC Switching Characteristics for Receiver (for DDRIO I/O Bank with Fixed Code - Input Buffers)

ODT (On Die Termination)	–1	–Std	–1	–Std	Unit
None	1.968	2.315	2.099	2.47	ns

Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	Unit
2 mA	slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	medium_fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4 mA	slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	medium_fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6 mA	slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	medium_fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns
8 mA	slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V.

Table 180 • **B-LVDS AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.738	3.221	ns
100	2.735	3.218	ns

Table 181 • **B-LVDS AC Switching Characteristics for Receiver for MSIOD I/O Bank (Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.495	2.934	ns
100	2.495	2.935	ns

Table 182 • **B-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
2.258	2.656	2.343	2.756	2.329	2.74	2.12	2.494	2.123	2.497	ns

2.3.7.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum Input and Output Levels

Table 183 • **M-LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage[1]	V_{DDI}	2.375	2.5	2.625	V

1. Only M-LVDS TYPE I is supported.

Table 184 • **M-LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	2.925	V
Input current high[1]	I_{IH} (DC)			
Input current low[2]	I_{IL} (DC)			

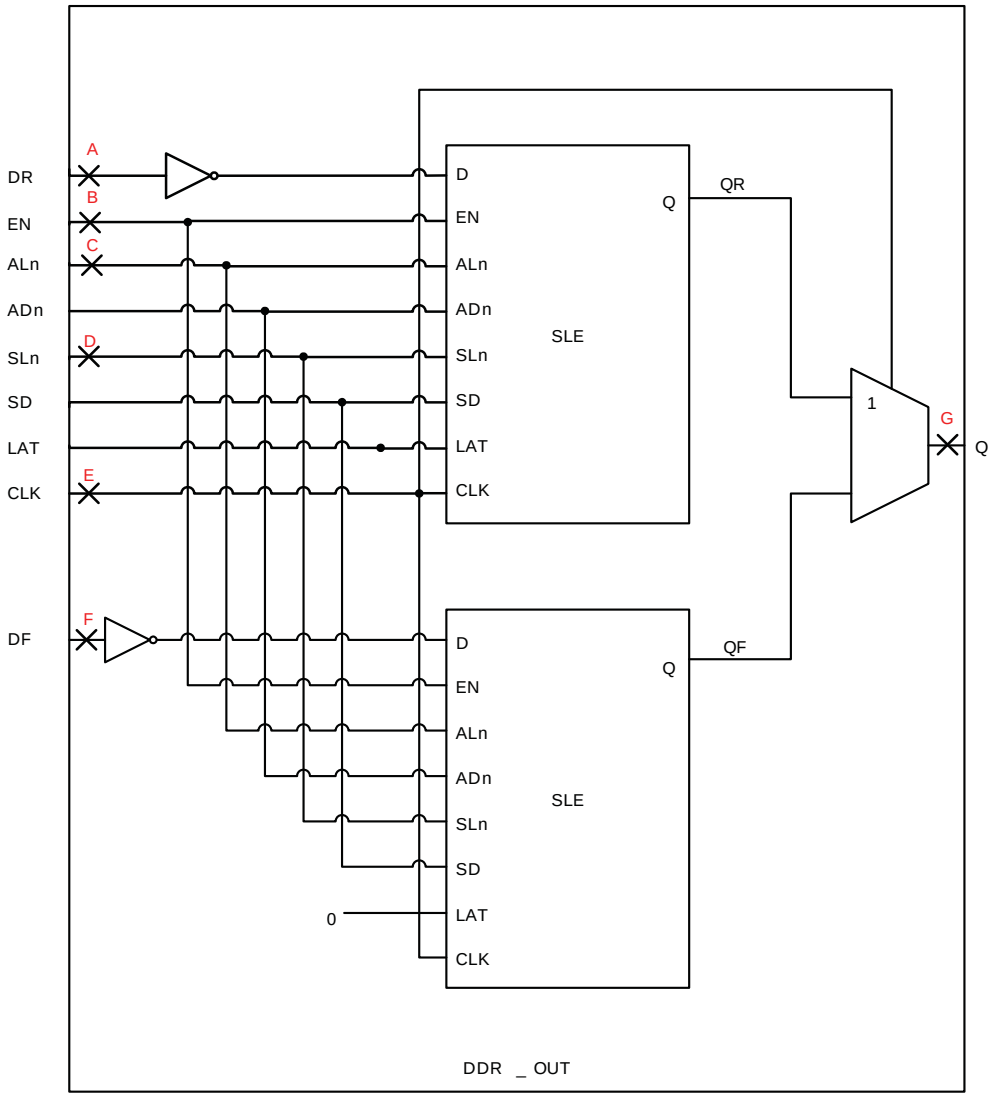
1. See Table 24, page 22.

Table 221 • **Input DDR Propagation Delays *(continued)***

Symbol	Description	Measuring Nodes (from, to)	–1	–Std	Unit
$T_{DDRIWAL}$	Asynchronous load minimum pulse width for input DDR	F, F	0.304	0.357	ns
$T_{DDRICKMPWH}$	Clock minimum pulse width high for input DDR	B, B	0.075	0.088	ns
$T_{DDRICKMPWL}$	Clock minimum pulse width low for input DDR	B, B	0.159	0.187	ns

2.3.9.4 Output DDR Module

Figure 12 • Output DDR Module



2.3.10.2 Timing Characteristics

The following table lists the combinatorial cell propagation delays in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 223 • **Combinatorial Cell Propagation Delays**

Combinatorial Cell	Equation	Symbol	–1	–Std	Unit
INV	Y = !A	T_{PD}	0.1	0.118	ns
AND2	Y = A · B	T_{PD}	0.164	0.193	ns
NAND2	Y = !(A · B)	T_{PD}	0.147	0.173	ns
OR2	Y = A + B	T_{PD}	0.164	0.193	ns
NOR2	Y = !(A + B)	T_{PD}	0.147	0.173	ns
XOR2	Y = A ⊕ B	T_{PD}	0.164	0.193	ns
XOR3	Y = A ⊕ B ⊕ C	T_{PD}	0.225	0.265	ns
AND3	Y = A · B · C	T_{PD}	0.209	0.246	ns
AND4	Y = A · B · C · D	T_{PD}	0.287	0.338	ns

2.3.10.3 Sequential Module

IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

Figure 15 • **Sequential Module**

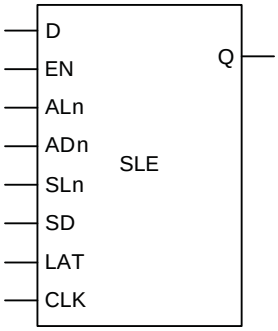


Table 238 • **µSRAM (RAM64x16) in 64 × 16 Mode *(continued)***

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the µSRAM in 128 × 9 mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 239 • **µSRAM (RAM128x9) in 128 × 9 Mode**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		–0.778		–0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns

The following table lists the µSRAM in 256 × 4 mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 241 • **µSRAM (RAM256x4) in 256 × 4 Mode**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.27		0.31	ns
Read access time without pipeline register			1.75		2.06	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.931		2.272		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.121		0.142		ns
Read address hold time in asynchronous mode		–0.65		–0.76		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.77		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.09		2.46	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.02		–0.03		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.83		0.98	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.101		0.118		ns
Write input data hold time	T_{DINCHD}	0.137		0.161		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns

The following table lists the programming times in worst-case conditions when T_J = 100 °C, V_{DD} = 1.14 V. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 256 • **JTAG Programming (Fabric Only)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	302672	44	10	Sec
010	568784	50	18	Sec
025	1223504	73	26	Sec
050	2424832	88	54	Sec
060	2418896	99	54	Sec
090	3645968	135	126	Sec
150	6139184	177	193	Sec

Table 257 • **JTAG Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	137536	61	4	Sec
010	274816	100	9	Sec
025	274816	100	9	Sec
050	2,78,528	106	8	Sec
060	268480	98	8	Sec
090	544496	176	15	Sec
150	544496	177	15	Sec

Table 258 • **JTAG Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	439296	71	11	Sec
010	842688	129	20	Sec
025	1497408	142	35	Sec
050	2695168	184	59	Sec
060	2686464	180	70	Sec
090	4190208	288	147	Sec
150	6682768	338	231	Sec

Table 259 • **2 Step IAP Programming (Fabric Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	302672	4	39	6	Sec
010	568784	7	45	12	Sec
025	1223504	14	55	23	Sec
050	2424832	29	74	40	Sec
060	2418896	39	83	50	Sec
090	3645968	60	106	73	Sec
150	6139184	100	154	120	Sec

Table 260 • **2 Step IAP Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	137536	2	59	5	Sec
010	274816	4	98	11	Sec
025	274816	4	100	10	Sec
050	2,78,528	3	107	9	Sec
060	268480	5	98	22	Sec
090	544496	10	174	43	Sec
150	544496	10	175	44	Sec

Table 261 • **2 Step IAP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	6	78	11	Sec
010	842688	11	122	21	Sec
025	1497408	19	135	32	Sec
050	2695168	32	158	48	Sec
060	2686464	43	159	70	Sec
090	4190208	68	258	115	Sec
150	6682768	109	308	162	Sec

2.3.22 JTAG

Table 284 • **JTAG 1532 for 005, 010, 025, and 050 Devices**

		005		010		025		050		Unit
Parameter	**Symbol**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	
Clock to Q (data out)	T_{TCK2Q}	7.47	8.79	7.73	9.09	7.75	9.12	7.89	9.28	ns
Reset to Q (data out)	T_{RSTB2Q}	7.65	9	6.43	7.56	6.13	7.21	7.40	8.70	ns
Test data input setup time	T_{DISU}	–1.05	–0.89	–0.69	–0.59	–0.67	–0.57	–0.30	–0.25	ns
Test data input hold time	T_{DIHD}	2.38	2.8	2.38	2.8	2.42	2.85	2.09	2.45	ns
Test mode select setup time	T_{TMSSU}	–0.73	–0.62	–1.03	–1.21	–1.1	–0.94	0.28	0.33	ns
Test mode select hold time	T_{TMDHD}	1.36	1.6	1.43	1.68	1.93	2.27	0.16	0.19	ns
ResetB removal time	$T_{TRSTREM}$	–0.77	–0.65	–1.08	–0.92	–1.33	–1.13	–0.45	–0.38	ns
ResetB recovery time	$T_{TRSTREC}$	–0.76	–0.65	–1.07	–0.91	–1.34	–1.14	–0.45	–0.38	ns
TCK maximum frequency	F_{TCKMAX}	25	21.25	25	21.25	25	21.25	25.00	21.25	MHz

Table 285 • **JTAG 1532 for 060, 090, and 150 Devices**

		060		090		150		
Parameter	**Symbol**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
Clock to Q (data out)	T_{TCK2Q}	8.38	9.86	8.96	10.54	8.66	10.19	ns
Reset to Q (data out)	T_{RSTB2Q}	8.54	10.04	7.75	9.12	8.79	10.34	ns
Test data input setup time	T_{DISU}	–1.18	–1	–1.31	–1.11	–0.96	–0.82	ns
Test data input hold time	T_{DIHD}	2.52	2.97	2.68	3.15	2.57	3.02	ns
Test mode select setup time	T_{TMSSU}	–0.97	–0.83	–1.02	–0.87	–0.53	–0.45	ns
Test mode select hold time	T_{TMDHD}	1.7	2	1.67	1.96	1.02	1.2	ns
ResetB removal time	$T_{TRSTREM}$	–1.21	–1.03	–0.76	–0.65	–1.03	–0.88	ns
ResetB recovery time	$T_{TRSTREC}$	–1.21	–1.03	–0.77	–0.65	–1.03	–0.88	ns
TCK maximum frequency	F_{TCKMAX}	25	21.25	25	21.25	25	21.25	MHz

2.3.23 System Controller SPI Characteristics

2.3.24 Power-up to Functional Times

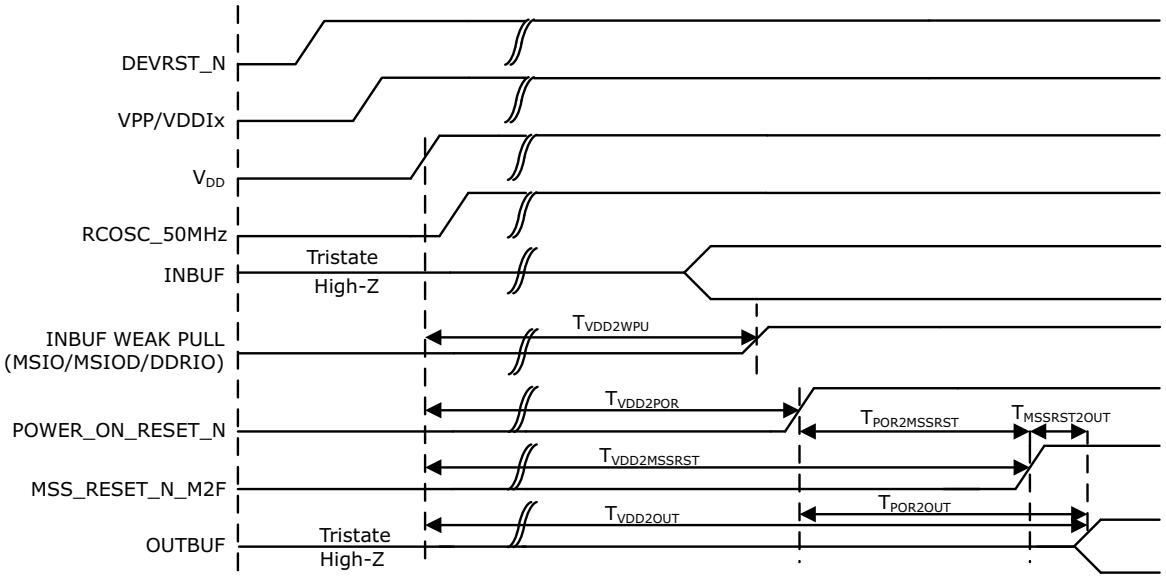
The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 288 • **Power-up to Functional Times for SmartFusion2**

				Maximum Power-up to Functional Time for SmartFusion2 (uS)						
Symbol	**From**	**To**	**Description**	**005**	**010**	**025**	**050**	**060**	**090**	**150**
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	647	500	531	483	474	524	647
$T_{POR2MSSRST}$	POWER_ON_RESET_N	MSS_RESET_N_M2F	Fabric to MSS	644	497	528	480	468	518	641
$T_{MSSRST2OUT}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.6	3.6	3.6	3.4	4.9	4.8	4.8
$T_{VDD2OUT}$	V_{DD}	Output available at I/O	V_{DD} at its minimum threshold level to output	3096	2975	3012	2959	2869	2992	3225
$T_{VDD2POR}$	V_{DD}	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	2476	2487	2496	2486	2406	2563	2602
$T_{VDD2MSSRST}$	V_{DD}	MSS_RESET_N_M2F	V_{DD} at its minimum threshold level to MSS	3093	2972	3008	2956	2864	2987	3220
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

Figure 17 • **Power-up to Functional Timing Diagram for SmartFusion2**



The following table lists the IGLOO2 power-up to functional times in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 289 • **Power-up to Functional Times for IGLOO2**

				Maximum Power-up to Functional Time for IGLOO2 (uS)						
Symbol	**From**	**To**	**Description**	**005**	**010**	**025**	**050**	**060**	**090**	**150**
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	114	114	113	114	114	114
$T_{VDD2OUT}$	V_{DD}	Output available at I/O	V_{DD} at its minimum threshold level to output	2587	2600	2607	2558	2591	2600	2699
$T_{VDD2POR}$	V_{DD}	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	2474	2486	2493	2445	2477	2486	2585
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide*.