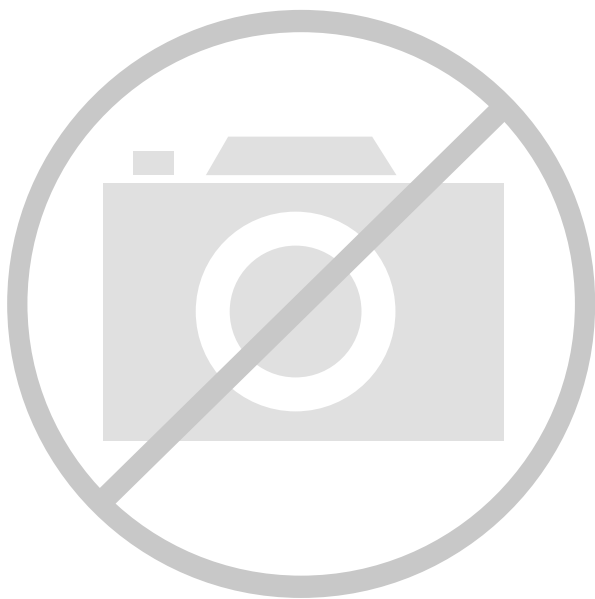




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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                                                   |
|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Active                                                                                                                                                            |
| Number of LABs/CLBs            | -                                                                                                                                                                 |
| Number of Logic Elements/Cells | 56520                                                                                                                                                             |
| Total RAM Bits                 | 1869824                                                                                                                                                           |
| Number of I/O                  | 200                                                                                                                                                               |
| Number of Gates                | -                                                                                                                                                                 |
| Voltage - Supply               | 1.14V ~ 2.625V                                                                                                                                                    |
| Mounting Type                  | Surface Mount                                                                                                                                                     |
| Operating Temperature          | -40°C ~ 100°C (TJ)                                                                                                                                                |
| Package / Case                 | 325-TFBGA, FCBGA                                                                                                                                                  |
| Supplier Device Package        | 325-FCBGA (11x11)                                                                                                                                                 |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/microchip-technology/m2gl060-fcs325i">https://www.e-xfl.com/product-detail/microchip-technology/m2gl060-fcs325i</a> |

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## 2.2 References

The following documents are recommended references:

PB0121: IGLOO2 Product Brief  
 DS0124: IGLOO2 Pin Descriptions  
 PB0115: SmartFusion2 SoC FPGA Product Brief  
 DS0115: SmartFusion2 Pin Descriptions

All product documentation for IGLOO2 and SmartFusion2 is available at:  
<http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga>  
<http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#overview>

## 2.3 Electrical Specifications

### 2.3.1 Operating Conditions

The following table lists the stress limits. Stress applied above the specified limit may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table are not implied.

Table 3 Absolute Maximum Ratings

| Parameter                                                                                                  | Symbol                       | Min | Max  | Unit |
|------------------------------------------------------------------------------------------------------------|------------------------------|-----|------|------|
| DC core supply voltage. Must always power this pin.                                                        | V <sub>DD</sub>              | 0.3 | 1.32 | V    |
| Power supply for charge pumps (for normal operation and programming). Must always power this pin.          | V <sub>PP</sub>              | 0.3 | 3.63 | V    |
| Analog power pad for MDDR PLL                                                                              | MSS_MDDR_PLL_VDDA            | 0.3 | 3.63 | V    |
| Analog power pad for MDDR PLL                                                                              | HPMS_MDDR_PLL_VDDA           | 0.3 | 3.63 | V    |
| Analog power pad for FDDR PLL                                                                              | FDDR_PLL_VDDA                | 0.3 | 3.63 | V    |
| Analog power pad for MDDR PLL                                                                              | PLL0_PLL1_MSS_MDDR_VDDA      | 0.3 | 3.63 | V    |
| Analog power pad for MDDR PLL                                                                              | PLL0_PLL1_HPMS_MDDR_VDDA     | 0.3 | 3.63 | V    |
| Analog power pad for PLL0 5                                                                                | CCC_XX[01]_PLL_VDDA          | 0.3 | 3.63 | V    |
| High supply voltage for PLL SerDes[01]                                                                     | SERDES_[01]_PLL_VDDA         | 0.3 | 3.63 | V    |
| Analog power for SerDes[01] PLL lane0 to lane3. This is a 2.5 V SerDes internal PLL supply.                | SERDES_[01]_L[0123]_VDDAPLL  | 0.3 | 2.75 | V    |
| TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply. | SERDES_[01]_L[0123]_VDDAIO   | 0.3 | 1.32 | V    |
| PCIe/PCS power supply                                                                                      | SERDES_[01]_VDD              | 0.3 | 1.32 | V    |
| DC FPGA I/O buffer supply voltage for MSIO I/O bank                                                        | V <sub>DDI<sub>x</sub></sub> | 0.3 | 3.63 | V    |
| DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks                                                | V <sub>DDI<sub>x</sub></sub> | 0.3 | 2.75 | V    |
| I/O Input voltage for MSIO I/O bank                                                                        | V <sub>I</sub>               | 0.3 | 3.63 | V    |
| I/O Input voltage for MSIOD/DDRIO I/O bank                                                                 | V <sub>I</sub>               | 0.3 | 2.75 | V    |
| Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to V <sub>PP</sub> .    | V <sub>PPNVM</sub>           | 0.3 | 3.63 | V    |
| Storage temperature <sup>1</sup>                                                                           | T <sub>STG</sub>             | 65  | 150  | °C   |
| Junction temperature                                                                                       | T <sub>J</sub>               | 55  | 135  | °C   |













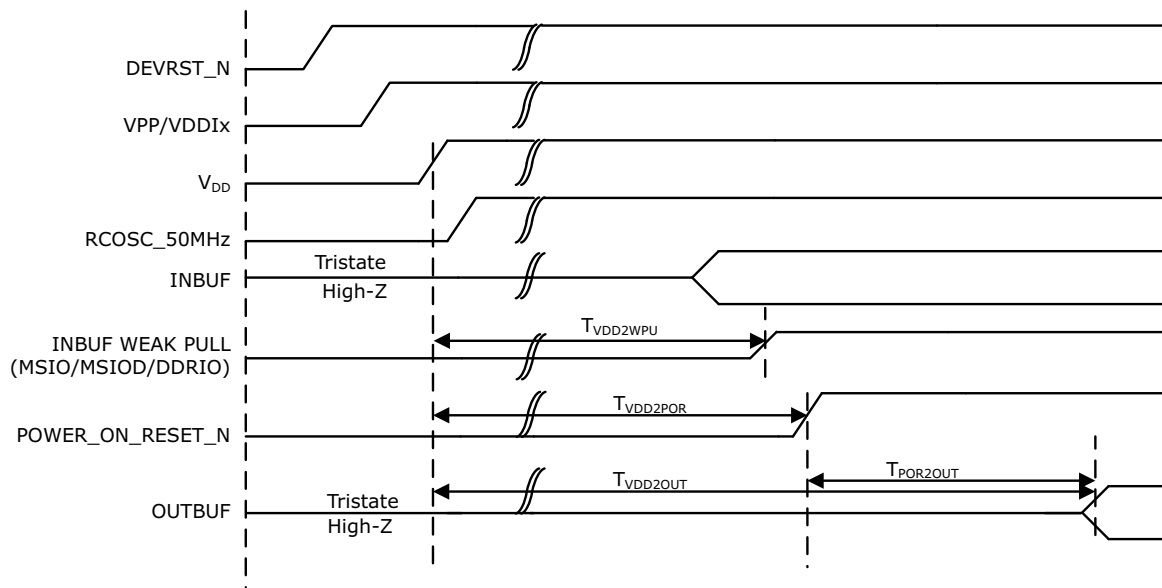
## 2.3.24 Power-up to Functional Times

The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when  $T_J = 100\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 288 • Power-up to Functional Times for SmartFusion2**

| Symbol           | From             | To                      | Description                                       | Maximum Power-up to Functional Time for SmartFusion2 (uS) |      |      |      |      |      |      |
|------------------|------------------|-------------------------|---------------------------------------------------|-----------------------------------------------------------|------|------|------|------|------|------|
|                  |                  |                         |                                                   | 005                                                       | 010  | 025  | 050  | 060  | 090  | 150  |
| $T_{POR2OUT}$    | POWER_ON_RESET_N | Output available at I/O | Fabric to output                                  | 647                                                       | 500  | 531  | 483  | 474  | 524  | 647  |
| $T_{POR2MSSRST}$ | POWER_ON_RESET_N | MSS_RESE T_N_M2F        | Fabric to MSS                                     | 644                                                       | 497  | 528  | 480  | 468  | 518  | 641  |
| $T_{MSSRST2OUT}$ | MSS_RESET_N_M2F  | Output available at I/O | MSS to output                                     | 3.6                                                       | 3.6  | 3.6  | 3.4  | 4.9  | 4.8  | 4.8  |
| $T_{VDD2OUT}$    | $V_{DD}$         | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 3096                                                      | 2975 | 3012 | 2959 | 2869 | 2992 | 3225 |
| $T_{VDD2POR}$    | $V_{DD}$         | POWER_ON_RESET_N        | $V_{DD}$ at its minimum threshold level to fabric | 2476                                                      | 2487 | 2496 | 2486 | 2406 | 2563 | 2602 |
| $T_{VDD2MSSRST}$ | $V_{DD}$         | MSS_RESE T_N_M2F        | $V_{DD}$ at its minimum threshold level to MSS    | 3093                                                      | 2972 | 3008 | 2956 | 2864 | 2987 | 3220 |
| $T_{VDD2WPU}$    | DEV_RST_N        | DDRIO Inbuf weak pull   | DEV_RST_N to Inbuf weak pull                      | 2500                                                      | 2487 | 2509 | 2475 | 2507 | 2519 | 2617 |
|                  | DEV_RST_N        | MSIO Inbuf weak pull    | DEV_RST_N to Inbuf weak pull                      | 2504                                                      | 2491 | 2510 | 2478 | 2517 | 2525 | 2620 |
|                  | DEV_RST_N        | MSIOD Inbuf weak pull   | DEV_RST_N to Inbuf weak pull                      | 2479                                                      | 2468 | 2493 | 2458 | 2486 | 2499 | 2595 |

**Note:** For more information about power-up times, see *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

**Figure 18 • Power-up to Functional Timing Diagram for IGLOO2**

### 2.3.25 DEVRST\_N Characteristics

**Table 290 • DEVRST\_N Characteristics for All Devices**

| Parameter             | Symbol            | Max | Unit |
|-----------------------|-------------------|-----|------|
| DEVRST_N ramp rate    | $T_{RAMPDEVRSTN}$ | 1   | us   |
| DEVRST_N cycling rate | $F_{MAXPDEVRSTN}$ | 100 | kHz  |

### 2.3.26 DEVRST\_N to Functional Times

The following table lists the SmartFusion2 DEVRST\_N to functional times in worst-case industrial conditions when  $T_J = 100^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 291 • DEVRST\_N to Functional Times for SmartFusion2**

| Symbol           | From             | To                      | Description                                       | Maximum Power-up to Functional Time for SmartFusion2 (uS) |     |     |     |     |     |     |
|------------------|------------------|-------------------------|---------------------------------------------------|-----------------------------------------------------------|-----|-----|-----|-----|-----|-----|
|                  |                  |                         |                                                   | 005                                                       | 010 | 025 | 050 | 060 | 090 | 150 |
| $T_{POR2OUT}$    | POWER_ON_RESET_N | Output available at I/O | Fabric to output                                  | 518                                                       | 501 | 527 | 521 | 422 | 419 | 694 |
| $T_{POR2MSSRST}$ | POWER_ON_RESET_N | MSS_RESET_N_M2F         | Fabric to MSS                                     | 515                                                       | 497 | 524 | 518 | 417 | 414 | 689 |
| $T_{MSSRST2OUT}$ | MSS_RESET_N_M2F  | Output available at I/O | MSS to output                                     | 3.5                                                       | 3.5 | 3.5 | 3.3 | 4.8 | 4.8 | 4.8 |
| $T_{DEVRST2OUT}$ | DEVRST_N         | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 706                                                       | 768 | 715 | 691 | 641 | 635 | 871 |





















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