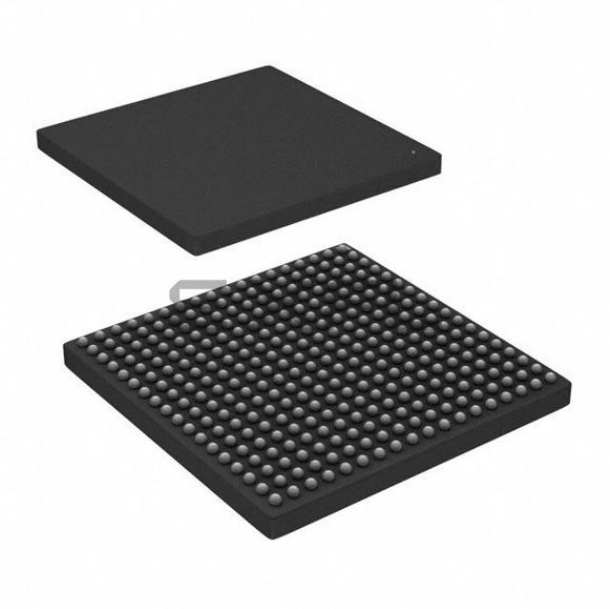

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	56520
Total RAM Bits	1869824
Number of I/O	200
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	325-TFBGA, FCBGA
Supplier Device Package	325-FCBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl060-fcsg325i

Tables

Table 1 IGLOO2 and SmartFusion2 Design Security Densities 4
Table 2 IGLOO2 and SmartFusion2 Data Security Densities 4
Table 3 Absolute Maximum Ratings 5
Table 4 Recommended Operating Conditions 6
Table 5 FPGA Operating Limits 7
Table 6 Embedded Operating Flash Limits 8
Table 7 Device Storage Temperature and Retention 8
Table 8 High Temperature Data Retention (HTR) Lifetime 8
Table 9 Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices 10
Table 10 Quiescent Supply Current Characteristics 12
Table 11 SmartFusion2 and IGLOO2 Quiescent Supply Current (V_{DD} = 1.2 V) – Typical Process 12
Table 12 Currents During Program Cycle, 0 °C < = T_J <= 85 °C – Typical Process 13
Table 13 Currents During Verify Cycle, 0 °C <= T_J <= 85 °C – Typical Process 13
Table 14 SmartFusion2 and IGLOO2 Quiescent Supply Current (V_{DD} = 1.26 V) – Worst-Case Process 13
Table 15 Average Junction Temperature and Voltage Derating Factors for Fabric Timing Delays 14
Table 16 Inrush Currents at Power up, –40 °C <= T_J <= 100 °C – Typical Process 14
Table 17 Timing Model Parameters 15
Table 18 Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions . 19
Table 19 Maximum Data Rate Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions 20
Table 20 Maximum Data Rate Summary Table for Differential I/O in Worst-Case Industrial Conditions . . . 20
Table 21 Maximum Frequency Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions . 20
Table 22 Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions 21
Table 23 Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions . . . 21
Table 24 Input Capacitance, Leakage Current, and Ramp Time 22
Table 25 I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank 22
Table 26 I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank 23
Table 27 I/O Weak Pull-up/Pull-down Resistances for MSIOD I/O Bank 23
Table 28 Schmitt Trigger Input Hysteresis 23
Table 29 LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only) 24
Table 30 LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only) 24
Table 31 LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only) 24
Table 32 LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only) 24
Table 33 LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only) 24
Table 34 LVTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers) 25
Table 35 LVTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers) 25
Table 36 LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only) . . 25
Table 37 LVTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank 25
Table 38 LVCMOS 2.5 V DC Recommended DC Operating Conditions 26
Table 39 LVCMOS 2.5 V DC Input Voltage Specification 26
Table 40 LVCMOS 2.5 V DC Output Voltage Specification 26
Table 41 LVCMOS 2.5 V AC Minimum and Maximum Switching Speed 26
Table 42 LVCMOS 2.5 V AC Calibrated Impedance Option 26
Table 43 LVCMOS 2.5 V Receiver Characteristics (Input Buffers) 27
Table 44 LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers) 27
Table 45 LVCMOS 2.5 V AC Test Parameter Specifications 27
Table 46 LVCMOS 2.5 V Transmitter Drive Strength Specifications 27
Table 47 LVCMOS 2.5 V Transmitter Characteristics for MSIO Bank (Output and Tristate Buffers) 28
Table 48 LVCMOS 1.8 V DC Recommended Operating Conditions 29
Table 49 LVCMOS 1.8 V DC Input Voltage Specification 29
Table 50 LVCMOS 1.8 V DC Output Voltage Specification 29

2.3.5.3 Tristate Buff er and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

Figure 5 • Tristate Buffer for Enable Path Test Point

2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

Table 18 • Maximum Data Rate Summary Table fo r Single-Ended I/O in Worst-Case Industrial Conditions

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	630			Mbps
LVTTL 3.3 V	600			Mbps

Table 254 • **Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only) *(continued)***

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	
	100 kHz	25 MHz	12.5 MHz	Unit
150	161	161	161	Sec

Table 255 • **Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	
	100 kHz	25 MHz	12.5 MHz	Unit
005	47	27	28	Sec
010	77	35	35	Sec
025	150	42	41	Sec
050	33[1]	Not Supported	Not Supported	Sec
060	291	83	82	Sec
090	427	109	108	Sec
150	708	157	160	Sec
005	41	48	49	Sec
010	86	87	87	Sec
025	87	85	86	Sec
050	85	Not Supported	Not Supported	Sec
060	78	86	86	Sec
090	154	162	162	Sec
150	161	161	161	Sec
005	87	67	66	Sec
010	161	113	113	Sec
025	229	120	121	Sec
050	112	Not Supported	Not Supported	Sec
060	368	161	158	Sec
090	582	261	260	Sec
150	867	309	310	Sec

1. Auto Programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

2.3.21 Clock Conditioning Circuits (CCC)

The following table lists the CCC/PLL specifications in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 282 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**

Parameter	Min	Typ	Max	Unit	Conditions
Clock conditioning circuitry input frequency F_{IN_CCC}	1		200	MHz	All CCC
	0.032		200	MHz	32 kHz capable CCC
Clock conditioning circuitry output frequency F_{OUT_CCC}[1]	0.078		400	MHz	
PLL VCO frequency[2]	500		1000	MHz	
Delay increments in programmable delay blocks		75	100	ps	
Number of programmable values in each programmable delay block			64		
Acquisition time		70	100	µs	F_{IN} >= 1 MHz
		1	16	ms	F_{IN} = 32 kHz
Input duty cycle (reference clock)					Internal Feedback
	10		90	%	1 MHz ≤ F_{IN_CCC} ≤ 25 MHz
	25		75	%	25 MHz ≤ F_{IN_CCC}≤ 100 MHz
	35		65	%	100 MHz ≤ F_{IN_CCC} ≤ 150 MHz
	45		55	%	150 MHz ≤ F_{IN_CCC} ≤ 200 MHz
					External Feedback (CCC, FPGA, Off-chip)
	25		75	%	1 MHz ≤ F_{IN_CCC} ≤ 25 MHz
	35		65	%	25 MHz ≤ F_{IN_CCC} ≤ 35 MHz
	45		55	%	35 MHz ≤ F_{IN_CCC} ≤ 50 MHz
Output duty cycle	48		52	%	050 devices F_{OUT} ≤ 400 MHz
	48		52	%	005, 010, and 025 devices F_{OUT} < 350 MHz
	46		54	%	005, 010, and 025 devices 350 MHz ≤ F_{out} ≤ 400 MHz
	48		52	%	060 and 090 devices F_{OUT} ≤ 100 MHz
	44		52	%	060 and 090 devices 100 MHz ≤ F_{OUT} ≤ 400 MHz
	48		52	%	150 devices F_{OUT} ≤ 120 MHz
	45		52	%	150 devices 120 MHz ≤ F_{OUT} ≤ 400 MHz
Spread Spectrum Characteristics					
Modulation frequency range	25	35	50	k	
Modulation depth range	0		1.5	%	
Modulation depth control		0.5		%	

The following table lists the system controller characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 286 • **System Controller SPI Characteristics for All Devices**

Symbol	Description	Conditions	Min	Typ	Unit
sp1	SC_SPI_SCK minimum period		20		ns
sp2	SC_SPI_SCK minimum pulse width high		10		ns
sp3	SC_SPI_SCK minimum pulse width low		10		ns
sp4[1]	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%–90%) 1	I/O configuration: LVTTL 3.3 V–20 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C		1.239	ns
sp5[1]	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%–90%) 1	I/O configuration: LVTTL 3.3 V–20 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C		1.245	ns
sp6	Data from master (SC_SPI_SDO) setup time		160		ns
sp7	Data from master (SC_SPI_SDO) hold time		160		ns
sp8	SC_SPI_SDI setup time		20		ns
sp9	SC_SPI_SDI hold time		20		ns

1. For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx. Use the supported I/O Configurations for the System Controller SPI in the following table.

Table 287 • **Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)**

Voltage Supply	I/O Drive Configuration	Unit
3.3 V	20	mA
2.5 V	16	mA
1.8 V	12	mA
1.5 V	8	mA
1.2 V	4	mA