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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	56520
Total RAM Bits	1869824
Number of I/O	387
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl060t-1fgg676

1. For flash programming and retention maximum limits, see Table 5, page 7. For recommended operating conditions, see Table 4, page 6.

Table 4 • Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Operating junction temperature	T_J	0	25	85	°C	Commercial
		–40	25	100	°C	Industrial
Programming junction temperatures ¹	T_J	0	25	85	°C	Commercial
		–40	25	100	°C	Industrial
DC core supply voltage. Must always power this pin.	V_{DD}	1.14	1.2	1.26	V	
Power supply for charge pumps (for normal operation and programming) for the 005, 010, 025, 050, 060 devices	V_{PP}	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Power supply for charge pumps (for normal operation and programming) for the 090 and 150 devices	V_{PP}	3.15	3.3	3.45	V	3.3 V range
Analog power pad for MDDR PLL	MSS_MDDR_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for MDDR PLL	HPMS_MDDR_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for FDDR PLL	FDDR_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for MDDR PLL	PLL0_PLL1_MSS_MDDR_V DDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for MDDR PLL	PLL0_PLL1_HPMS_MDDR_ VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for PLL0 to PLL5	CCC_XX[01]_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
High supply voltage for PLL SerDes[01]	SERDES_[01]_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power for SerDes[01] PLL Lane 0 to Lane 3. This is a 2.5 V SerDes internal PLL supply.	SERDES_[01]_L[0123]_VD DAPLL	2.375	2.5	2.625	V	
TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply.	SERDES_[01]_L[0123]_VD DAIO	1.14	1.2	1.26	V	
PCIe/PCS power supply	SERDES_[01]_VDD	1.14	1.2	1.26	V	
1.2 V DC supply voltage	V_{DDIx}	1.14	1.2	1.26	V	
1.5 V DC supply voltage	V_{DDIx}	1.425	1.5	1.575	V	
1.8 V DC supply voltage	V_{DDIx}	1.71	1.8	1.89	V	
2.5 V DC supply voltage	V_{DDIx}	2.375	2.5	2.625	V	

Table 9 • Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices (continued)

	Still Air	1.0 m/s	2.5 m/s			
Device	θ_{JA}			θ_{JB}	θ_{JC}	Unit
150						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W
FCS536	15.01	12.06	10.76	3.69	1.55	°C/W
FCV484	16.21	13.11	11.84	6.73	0.10	°C/W

2.3.1.2.1 Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in the actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package with another.

The maximum power dissipation allowed is calculated using EQ4.

$$\text{Maximum power allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100 °C. EQ5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where:

$$\theta_{JA} = 14.7 \text{ °C/W (taken from Table 9, page 10).}$$

$$T_A = 85 \text{ °C}$$

$$\text{Maximum power allowed} = \frac{100 \text{ °C} - 85 \text{ °C}}{14.7 \text{ °C/W}} = 1.088 \text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink may be attached to the top of the case, or the airflow inside the system must be increased.

2.3.1.2.2 Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from the junction to the board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

2.3.1.2.3 Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable to packages used with external heat sinks. Constant temperature is applied to the surface, which acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

2.3.1.3 ESD Performance

See RT0001: Microsemi Corporation - SoC Products Reliability Report for information about ESD.

Table 72 • LVCMOS 1.5 V Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	2.735	3.218	3.371	3.966	3.618	4.257	6.03	7.095	5.705	6.712	ns
4 mA	Slow	2.426	2.854	2.992	3.521	3.221	3.79	6.738	7.927	6.298	7.41	ns
6 mA	Slow	2.433	2.862	2.81	3.306	3.031	3.566	7.123	8.38	6.596	7.76	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

2.3.5.10 1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-12A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 73 • LVCMOS 1.2 V DC Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.140	1.2	1.26	V

Table 74 • LVCMOS 1.2 V DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	$V_{IH} (DC)$	$0.65 \times V_{DDI}$	1.26	V
DC input logic high (for MSIO I/O bank)	$V_{IH} (DC)$	$0.65 \times V_{DDI}$	3.45	V
DC input logic low	$V_{IL} (DC)$	-0.3	$0.35 \times V_{DDI}$	V
Input current high ¹	$I_{IH} (DC)$			
Input current low ¹	$I_{IL} (DC)$			

1. See Table 24, page 22.

Table 75 • LVCMOS 1.2 V DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	$V_{DDI} \times 0.75$		V
DC output logic low	V_{OL}		$V_{DDI} \times 0.25$	V

Table 76 • LVCMOS 1.2 V Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	200	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D_{MAX}	120	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	160	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 77 • LVCMOS 1.2 V AC Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CAL	75, 60, 50, 40	Ω

Table 78 • LVCMOS 1.2 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point	V_{TRIP}	0.6	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 79 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

Output Drive Selection			V_{OH} (V)	V_{OL} (V)	IOH (at V_{OH}) mA	IOL (at V_{OL}) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	2	2
4 mA	4 mA	4 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	4	4
		6 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	6	6

Note: For a detailed I/V curve, use the corresponding IBIS models:
www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.14\text{ V}$

Table 80 • LVCMOS 1.2 V Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	2.448	2.88	2.466	2.901	ns

Table 81 • LVCMOS 1.2 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On-Die Termination ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	4.714	5.545	4.675	5.5	ns
50	6.668	7.845	6.579	7.74	ns
75	5.832	6.862	5.76	6.777	ns
150	5.162	6.073	5.111	6.014	ns

Table 82 • LVCMOS 1.2 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	4.154	4.887	4.114	4.84	ns
50	6.918	8.139	6.806	8.008	ns
75	5.613	6.603	5.533	6.509	ns
150	4.716	5.549	4.657	5.479	ns

Table 83 • LVCMOS 1.2 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	6.713	7.897	5.362	6.308	6.723	7.909	7.233	8.51	6.375	7.499	ns
	Medium	5.912	6.955	4.616	5.43	5.915	6.959	6.887	8.102	6.009	7.069	ns
	Medium fast	5.5	6.469	4.231	4.978	5.5	6.471	6.672	7.849	5.835	6.865	ns
	Fast	5.462	6.426	4.194	4.935	5.463	6.427	6.646	7.819	5.828	6.857	ns
4 mA	Slow	6.109	7.186	4.708	5.539	6.098	7.174	8.005	9.418	7.033	8.274	ns
	Medium	5.355	6.299	4.034	4.746	5.338	6.28	7.637	8.985	6.672	7.849	ns
	Medium fast	4.953	5.826	3.685	4.336	4.932	5.802	7.44	8.752	6.499	7.646	ns
	Fast	4.911	5.777	3.658	4.303	4.89	5.754	7.427	8.737	6.488	7.632	ns
6 mA	Slow	5.89	6.929	4.506	5.301	5.874	6.911	8.337	9.808	7.315	8.605	ns
	Medium	5.176	6.089	3.862	4.543	5.155	6.065	7.986	9.394	6.943	8.168	ns
	Medium fast	4.792	5.637	3.523	4.145	4.765	5.606	7.808	9.186	6.775	7.97	ns
	Fast	4.754	5.593	3.486	4.101	4.728	5.563	7.777	9.149	6.769	7.963	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 84 • LVCMOS 1.2 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	6.746	7.937	7.458	8.774	8.172	9.614	9.867	11.608	8.393	9.874	ns
4 mA	Slow	7.068	8.315	6.678	7.857	7.474	8.793	10.986	12.924	9.043	10.638	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 85 • LVCMOS 1.2 V Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.883	4.568	4.868	5.726	5.329	6.269	7.994	9.404	7.527	8.855	ns
4 mA	Slow	3.774	4.44	4.188	4.926	4.613	5.426	8.972	10.555	8.315	9.782	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

2.3.5.11 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

Minimum and Maximum DC/AC Input and Output Levels Specification (Applicable to MSIO Bank Only)

Table 86 • PCI/PCI-X DC Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{DDI}	3.15	3.3	3.45	V

Table 87 • PCI/PCI-X DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input voltage	V _I	0	3.45	V
Input current high ¹	I _{IH} (DC)			
Input current low ¹	I _{IL} (DC)			

1. See Table 24, page 22.

Table 88 • PCI/PCI-X DC Output Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V _{OH}		Per PCI specification		V
DC output logic low	V _{OL}		Per PCI specification		V

Table 89 • PCI/PCI-X Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (MSIO I/O bank)	D _{MAX}	630	Mbps	AC Loading: per JEDEC specifications

Table 90 • PCI/PCI-X AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path (falling edge)	V _{TRIP}	0.615 × V _{DDI}	V
Measuring/trip point for data path (rising edge)	V _{TRIP}	0.285 × V _{DDI}	V
Resistance for data test path	RTT_TEST	25	Ω
Resistance for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	R _{ENT}	2K	Ω
Capacitive loading for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	C _{ENT}	5	pF
Capacitive loading for data path (T _{DP})	C _{LOAD}	10	pF

Table 107 • SSTL2 AC Differential Voltage Specifications

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	$V_{DIFF} (AC)$	0.7		V
AC differential cross point voltage	$V_x (AC)$	$0.5 \times V_{DDI} - 0.2$	$0.5 \times V_{DDI} + 0.2$	V

Table 108 • SSTL2 Minimum and Maximum AC Switching Speeds

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	400	Mbps	AC loading: per JEDEC specifications
Maximum data rate (for MSIO I/O bank)	D_{MAX}	575	Mbps	AC loading: 17pF load
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	700	Mbps	AC loading: 3 pF / 50 Ω load
		510	Mbps	AC loading: 17pF load

Table 109 • SSTL2 AC Impedance Specifications

Parameter	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	20, 42	Ω	Reference resistor = 150 Ω

Table 110 • DDR1/SSTL2 AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.25	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for SSTL2 Class I (T_{DP})	RTT_TEST	50	Ω
Reference resistance for data test path for SSTL2 Class II (T_{DP})	RTT_TEST	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 111 • SSTL2 Receiver Characteristics for DDRIO I/O Bank (Input Buffers)

		T_{PY}		Unit
	On-Die Termination (ODT)	-1	-Std	
Pseudo differential	None	1.549	1.821	ns
True differential	None	1.589	1.87	ns

Table 118 • DDR1/SSTL2 Class II Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.29	2.693	1.988	2.338	1.978	2.326	1.989	2.34	1.979	2.328	ns
Differential	2.418	2.846	2.304	2.711	2.297	2.702	2.131	2.506	2.124	2.499	ns

2.3.6.4 Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification**Table 119 • SSTL18 DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.71	1.8	1.89	V
Termination voltage	V_{TT}	0.838	0.900	0.964	V
Input reference voltage	V_{REF}	0.838	0.900	0.964	V

Table 120 • SSTL18 DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input logic high	V_{IH} (DC)	$V_{REF} + 0.125$	1.89	V
DC input logic low	V_{IL} (DC)	-0.3	$V_{REF} - 0.125$	V
Input current high ¹	I_{IH} (DC)			
Input current low ¹	I_{IL} (DC)			

1. See Table 24, page 22.

Table 121 • SSTL18 DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
SSTL18 Class I (DDR2 Reduced Drive)				
DC output logic high	V_{OH}	$V_{TT} + 0.603$		V
DC output logic low	V_{OL}		$V_{TT} - 0.603$	V
Output minimum source DC current (DDRIO I/O bank only)	I_{OH} at V_{OH}	6.5		mA
Output minimum sink current (DDRIO I/O bank only)	I_{OL} at V_{OL}	-6.5		mA
SSTL18 Class II (DDR2 Full Drive)¹				
DC output logic high	V_{OH}	$V_{TT} + 0.603$		V
DC output logic low	V_{OL}		$V_{TT} - 0.603$	V
Output minimum source DC current (DDRIO I/O bank only)	I_{OH} at V_{OH}	13.4		mA
Output minimum sink current (DDRIO I/O bank only)	I_{OL} at V_{OL}	-13.4		mA

1. To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.

2.3.6.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 139 • LPDDR DC Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max
Supply voltage	V_{DDI}	1.71	1.8	1.89
Termination voltage	V_{TT}	0.838	0.900	0.964
Input reference voltage	V_{REF}	0.838	0.900	0.964

Table 140 • LPDDR DC Input Voltage Specification

Parameter	Symbol	Min	Max
DC input logic high	V_{IH} (DC)	$0.7 \times V_{DDI}$	1.89
DC input logic low	V_{IL} (DC)	-0.3	$0.3 \times V_{DDI}$
Input current high ¹	I_{IH} (DC)		
Input current low ¹	I_{IL} (DC)		

1. See Table 24, page 22.

Table 141 • LPDDR DC Output Voltage Specification Reduced Drive

Parameter	Symbol	Min	Max
DC output logic high	V_{OH}	$0.9 \times V_{DDI}$	
DC output logic low	V_{OL}		$0.1 \times V_{DDI}$
Output minimum source DC current	I_{OH} at V_{OH}	0.1	
Output minimum sink current	I_{OL} at V_{OL}	-0.1	

Table 142 • LPDDR DC Output Voltage Specification Full Drive¹

Parameter	Symbol	Min	Max
DC output logic high	V_{OH}	$0.9 \times V_{DDI}$	
DC output logic low	V_{OL}		$0.1 \times V_{DDI}$
Output minimum source DC current	I_{OH} at V_{OH}	0.1	
Output minimum sink current	I_{OL} at V_{OL}	-0.1	

1. To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.

Table 143 • LPDDR DC Differential Voltage Specification

Parameter	Symbol	Min
DC input differential voltage	V_{ID} (DC)	$0.4 \times V_{DDI}$

Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers) (continued)

10 mA	medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	medium_fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
	slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
12 mA	medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	medium_fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
	slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
16 mA	medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	medium_fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
	slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	medium_fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management).

2.3.7 Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

2.3.7.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

Minimum and Maximum Input and Output Levels

Table 160 • LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{DDI}	2.375	2.5	2.625	V	2.5 V range
Supply voltage	V_{DDI}	3.15	3.3	3.45	V	3.3 V range

Table 161 • LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit	Conditions
DC Input voltage	V_I	0	2.925	V	2.5 V range
DC input voltage	V_I	0	3.45	V	3.3 V range
Input current high ¹	I_{IH} (DC)				
Input current low ¹	I_{IL} (DC)				

1. See Table 24, page 22.

Table 185 • M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 186 • M-LVDS Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	V_{OD}	300	650	mV
Output common mode voltage (for MSIO I/O bank only)	V_{OCM}	0.3	2.1	V
Input common mode voltage	V_{ICM}	0.3	1.2	V
Input differential voltage	V_{ID}	50	2400	mV

Table 187 • M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	500	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 188 • M-LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	50	Ω

Table 189 • M-LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 190 • M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.738	3.221	ns
100	2.735	3.218	ns

Table 191 • M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)

On-Die Termination (ODT)	T _{py}		Unit
	-1	-Std	
None	2.495	2.934	ns
100	2.495	2.935	ns

Table 192 • M-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)

T _{DP}		T _{ZL}		T _{ZH}		T _{HZ}		T _{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.258	2.656	2.348	2.762	2.334	2.746	2.123	2.497	2.125	2.5	ns

2.3.7.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

Mini-LVDS Minimum and Maximum Input and Output Levels

Table 193 • Mini-LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{DDI}	2.375	2.5	2.625	V

Table 194 • Mini-LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC Input voltage	V _I	0	2.925	V

Table 195 • Mini-LVDS DC Output Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V _{OH}	1.25	1.425	1.6	V
DC output logic low	V _{OL}	0.9	1.075	1.25	V

Table 196 • Mini-LVDS DC Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing	V _{OD}	300	600	mV
Output common mode voltage	V _{OCM}	1	1.4	V
Input common mode voltage	V _{ICM}	0.3	1.2	V
Input differential voltage	V _{ID}	100	600	mV

Table 197 • Mini-LVDS Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D _{MAX}	520	Mbps	AC loading: 2 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank)	D _{MAX}	700	Mbps	AC loading: 2 pF / 100 Ω differential load

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$.

Table 210 • RSDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.855	3.359	ns
100	2.85	3.353	ns

Table 211 • RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.602	3.061	ns
100	2.597	3.055	ns

Table 212 • RSDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.097	2.467	2.303	2.709	2.291	2.695	1.961	2.307	1.947	2.29	ns

Table 213 • RSDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
No pre-emphasis	1.614	1.899	1.559	1.834	1.55	1.823	1.59	1.87	1.575	1.852	ns
Min pre-emphasis	1.604	1.887	1.742	2.05	1.728	2.032	1.889	2.222	1.858	2.185	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

2.3.7.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

Minimum and Maximum Input and Output Levels (Applicable to MSIO I/O Bank Only)

Table 214 • LVPECL Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

Table 221 • Input DDR Propagation Delays (continued)

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
T _{DDRIWAL}	Asynchronous load minimum pulse width for input DDR	F, F	0.304	0.357	ns
T _{DDRICKMPWH}	Clock minimum pulse width high for input DDR	B, B	0.075	0.088	ns
T _{DDRICKMPWL}	Clock minimum pulse width low for input DDR	B, B	0.159	0.187	ns

Table 238 • μ SRAM (RAM64x16) in 64 × 16 Mode (continued)

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	-0.026		-0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 128 × 9 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 239 • μ SRAM (RAM128x9) in 128 × 9 Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		-0.778		-0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns

Table 262 • SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	302672	6	41	8	Sec
010	568784	10	48	14	Sec
025	1223504	21	61	29	Sec
050	2424832	39	82	50	Sec
060	2418896	44	87	54	Sec
090	3645968	66	112	79	Sec
150	6139184	108	162	128	Sec

Table 263 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	137536	3	64	4	Sec
010	274816	4	104	7	Sec
025	274816	4	104	8	Sec
050	2,78,528	4	102	8	Sec
060	268480	6	102	8	Sec
090	544496	10	179	15	Sec
150	544496	10	180	15	Sec

Table 264 • SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	9	83	11	Sec
010	842688	15	129	21	Sec
025	1497408	26	143	35	Sec
050	2695168	43	163	55	Sec
060	2686464	48	165	60	Sec
090	4190208	75	266	91	Sec
150	6682768	117	318	141	Sec

2.3.17 Non-Deterministic Random Bit Generator (NRBG) Characteristics

For more information about NRBG, see *AC407: Using NRBG Services in SmartFusion2 and IGLOO2 Devices Application Note*. The following table lists the NRBG in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 275 • Non-Deterministic Random Bit Generator (NRBG)

Service	Timing	Unit	Conditions	
			Prediction Resistance	Additional Input
Instantiate	85	ms	OFF	X
Generate (after Instantiate) ¹	4.5 ms + (6.25 us/byte x No. of Bytes)		OFF	0
	6.0 ms + (6.25 us/byte x No. of Bytes)		OFF	64
	7.0 ms + (6.25 us/byte x No. of Bytes)		OFF	128
Generate (after Instantiate)	47	ms	ON	X
Generate (subsequent) ¹	0.5 ms + (6.25 us/byte x No. of Bytes)		OFF	0
	2.0 ms + (6.25 us/byte x No. of Bytes)		OFF	64
	3.0 ms + (6.25 us/byte x No. of Bytes)		OFF	128
Generate (subsequent)	43	ms	ON	X
Reseed	40	ms		
Uninstantiate	0.16	ms		
Reset	0.10	ms		
Self test	20	ms	First time after power-up	
	6	ms	Subsequent	

1. If PUF_OFF, generate will incur additional PUF delay time for consecutive service calls.

2.3.18 Cryptographic Block Characteristics

For more information about cryptographic block and associated services, see *AC410: Using AES System Services in SmartFusion2 and IGLOO2 Devices Application Note* and *AC432: Using SHA-256 System Services in SmartFusion2 and IGLOO2 Devices Application Note*.

The following table lists the cryptographic block characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 276 • Cryptographic Block Characteristics

Service	Conditions	Timing	Unit
Any service	First certificate check penalty at boot	11.5	ms
AES128/256 (encoding / decoding) ¹	100 blocks up to 64k blocks	700	kbps

Table 277 • Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz) (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Startup time (with regard to stable oscillator output)	SUXTAL			0.8	ms	005, 010, 025, and 050 devices
				1.0	ms	090 and 150 devices

Table 278 • Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		2		MHz	
Accuracy	ACCXTAL			0.00105	%	050 devices
				0.003	%	005, 010, 025, 090, and 150 devices
				0.004	%	060 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		1	5	ns	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		1	5	ns	
Operating current	IDYNXTAL		0.3		mA	
Input logic level high	VIHXTAL	0.9 V _{PP}			V	
Input logic level low	VILXTAL			0.1 V _{PP}	V	
Startup time (with regard to stable oscillator output)	SUXTAL			4.5	ms	010 and 050 devices
				5	ms	005 and 025 devices
				7	ms	090 and 150 devices

Table 279 • Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		32		kHz	
Accuracy	ACCXTAL			0.004	%	005, 010, 025, 050, 060, and 090 devices
				0.005	%	150 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		150	300	ns	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		150	300	ns	
Operating current	IDYNXTAL		0.044		mA	010 and 050 devices
			0.060		mA	005, 025, 060, 090, and 150 devices
Input logic level high	VIHXTAL	0.9 V _{PP}			V	
Input logic level low	VILXTAL			0.1 V _{PP}	V	
Startup time (with regard to stable oscillator output)	SUXTAL			115	ms	005, 025, 050, 090, and 150 devices
				126	ms	010 devices

1. The minimum output clock frequency is limited by the PLL. For more information, see *UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide*.
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance is limited by the CCC output frequency.

The following table lists the CCC/PLL jitter specifications in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 283 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications

CCC Output Maximum Peak-to-Peak Period Jitter F _{OUT_CCC}						
Parameter		Conditions/Package Combinations				Unit
10 FG484, 050 FG896/FG484/FCS325 Packages¹	SSO = 0	0 < SSO <= 2	SSO <= 4	SSO <= 8	SSO <= 16	
20 MHz to 100 MHz	Max(110, ± 1% x (1/F _{OUT_CCC}))	Max(150, ± 1% x (1/F _{OUT_CCC}))				ps
100 MHz to 400 MHz	Max(120, ± 1% x (1/F _{OUT_CCC}))	Max(150, ± 1% x (1/F _{OUT_CCC}))			Max(170, ± 1% x (1/F _{OUT_CCC}))	ps
025 FG484/FCS325 Package¹	0 < SSO <=16					
20 MHz to 74 MHz	± 1% x (1/F _{OUT_CCC}))					ps
74 MHz to 400 MHz	210					ps
005 FG484 Package¹	0 < SSO <=16					
20 MHz to 53 MHz	± 1% x (1/F _{OUT_CCC}))					ps
53 MHz to 400 MHz	270					ps
090 FG676 and FC325 Package¹	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x (1/F _{OUT_CCC}))					ps
100 MHz to 400 MHz	150					ps
060 FG676 Package¹	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x (1/F _{OUT_CCC})					ps
100 MHz to 400 MHz	150					
150 FC1152 Package¹	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x (1/F _{OUT_CCC}))					ps
100 MHz to 400 MHz	120					ps

1. SSO data is based on LVCMOS 2.5 V MSIO and/or MSIOD bank I/Os.

The following table lists the receiver pa in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 297 • Receiver Parameters

Symbol	Description	Min	Typ	Max	Unit
VRX-IN-PP-CC	Differential input peak-to-peak sensitivity (2.5 Gbps)	0.238		1.2	V
	Differential input peak-to-peak sensitivity (2.5 Gbps, de-emphasized)	0.219		1.2	V
	Differential input peak-to-peak sensitivity (5.0 Gbps)	0.300		1.2	V
	Differential input peak-to-peak sensitivity (5.0 Gbps, de-emphasized)	0.300		1.2	V
VRX-CM-AC-P	Input common mode range (AC coupled)			150	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset			15	μs
RLRX-DIFF	Return loss differential mode (2.5 Gbps)	-10			dB
	Return loss differential mode (5.0 Gbps)				
	0.05 GHz to 1.25 GHz	-10			dB
	1.25 GHz to 2.5 GHz	-8			dB
RLRX-CM	Return loss common mode (2.5 Gbps, 5.0 Gbps)	-6			dB
RX-CID ¹	CID limit PCIe Gen1/2			200	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65		175	mV

1. AC-coupled, BER = e^{-12} , using synchronous clock.

Table 298 • SerDes Protocol Compliance

Protocol	Maximum Data Rate (Gbps)	-1	-Std
PCIe Gen 1	2.5	Yes	Yes
PCIe Gen 2	5.0	Yes	
XAUI	3.125	Yes	
Generic EPCS	3.2	Yes	
Generic EPCS	2.5	Yes	Yes