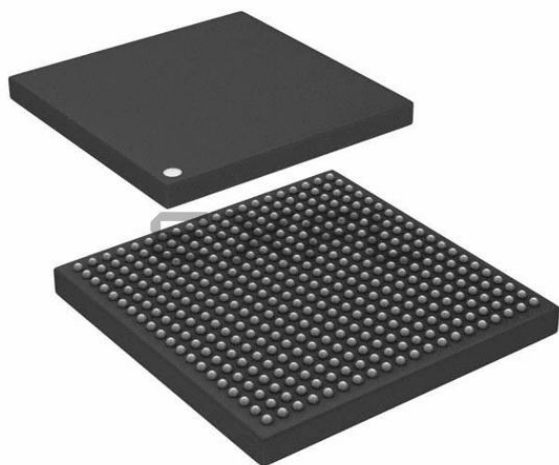




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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	56520
Total RAM Bits	1869824
Number of I/O	207
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	400-LFBGA
Supplier Device Package	400-VFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl060t-1vf400i

1.9 Revision 3.0

In revision 3.0 of this document, the Theta B/C columns and FCS325 package was updated. For more information, see Table 9, page 10 (SAR 62002).

1.10 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Table 1, page 4 was updated (SAR 59056).
- Table 7, page 8 temperature and data retention information was updated SAR (61363).
- Storage Operating Table was updated and split into three tables – Table 5, page 7, Table 7, page 8 (SAR 58725).
- Updated Theta B/C columns and FCS325 package in Table 9, page 10 (SAR 62002).
- Added 090-FCS325 thermal resistance to Table 9, page 10 (SAR 59384).
- TQ144 package was added to Table 9, page 10 (SAR 57708).
- Added PLL jitter data for the VF400 package (SAR 53162).
- Added Additional Worst Case IDD to Table 11, page 12 and Table 12, page 13 (SAR 59077).
- Table 13, page 13, Table 14, page 13, and Table 15, page 14 were added to verify Inrush currents (SAR 56348).
- Table 18, page 19 and Table 21, page 20 – I/O speeds were replaced.
- Max speed was changed in Table 41, page 26 (SAR 57221) and in Table 52, page 29 (SAR 57113).
- Minimum and Maximum DC/AC Input and Output Levels Specification, page 29 and Table 49, page 29–Table 57, page 31 were added.
- Added Cload to Table 89, page 39 (SAR 56238).
- Removed "Rs" information in DDR Timing Measurement Table 123, page 47, Table 133, page 49, and Table 144, page 52.
- Updated drive programming for M/B-LVDS outputs (SAR 58154).
- Added an inverter bubble to DDR_IN latch in Figure 10, page 70 (SAR 61418).
- QF waveform in Figure 11, page 71 was updated (SAR 59816).
- uSRAM Write Clock minimum values were updated in Table 237, page 86–Table 243, page 93 (SAR 55236).
- Fixed typo in the 32 kHz Crystal (XTAL) oscillator accuracy data section (SAR 59669).
- The "On-Chip Oscillator" section was split, and the Embedded NVM (eNVM) Characteristics, page 104 was added. Table 277, page 107–Table 281, page 109 were revised.(SARs 57898 and 59669).
- PLL VCP Frequency and conditions were added to Table 282, page 110 (SAR 57416).
- Fixed typo for PLL jitter data in the 100-400 MHz range (SAR 60727).
- Updated FCCC information in Table 282, page 110 and Table 283, page 111 (SAR 60799).
- Device 025 specifications were added to Table 283, page 111 (SAR 51625).
- JTAG Table 284, page 112 was replaced (SAR 51188).
- Flash*Freeze Table 293, page 119 was replaced (SAR 57828).
- Added support for HCSL I/O Standard for SERDES reference clocks in Table 300, page 123 and Table 301, page 123 (SAR 50748).
- Tir and Tif parameters were added to Table 303, page 124 (SAR 52203).
- Speed grade consistency was fixed in tables throughout the datasheet (SAR 50722).
- Added jitter attenuation information (SAR 59405).

1.11 Revision 1.0

The following is a summary of the changes in revision 1.0 of this document.

- The IGLOO2 v2 and the SmartFusion2 v5 datasheets are combined into this single product family datasheet.

Figure 1 • High Temperature Data Retention (HTR)**2.3.1.1 Overshoot/Undershoot Limits**

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to $V_{CCI} + 1.0$ V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

Note: The above specifications do not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant with the PCI standard including the PCI overshoot/undershoot specifications.

2.3.1.2 Thermal Characteristics

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ1 through EQ3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

2.3.2 Power Consumption

The following sections describe the power consumptions of the devices.

2.3.2.1 Quiescent Supply Current

Table 10 • Quiescent Supply Current Characteristics

Power Supplies/Blocks	Modes and Configurations	
	Non-Flash*Freeze	Flash*Freeze
FPGA Core	On	Off
V _{DD} /SERDES_[01]_VDD ¹	On	On
V _{PP} /V _{PPNVM}	On	On
HPMS_MDDR_PLL_VDDA/FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA/PLL0_PLL1_HPMS_MDDR_VDD A	0 V	0 V
SERDES_[01]_PLL_VDDA ²	0 V	0 V
SERDES_[01]_L[0123]_VDDAPLL/VDD_2V5 ²	On	On
SERDES_[01]_L[0123]_VDDAIIO ²	On	On
V _{DDI_x} ^{3, 4}	On	On
V _{REFx}	On	On
MSSDDR CLK	32 kHz	32 kHz
RAM	On	Sleep state
System controller	50 MHz	50 MHz
50 MHz oscillator (enable/disable)	Enable	Disabled
1 MHz oscillator (enable/disable)	Disabled	Disabled
Crystal oscillator (enable/disable)	Disabled	Disabled

1. SERDES_[01]_VDD Power Supply is shorted to V_{DD}.
2. SerDes and DDR blocks to be unused.
3. V_{DDI_x} has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate V_{DDI} bank supplies. For details on bank power supplies, see "Recommendation for Unused Bank Supplies" table in the AC393: *SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.
4. No Differential (that is to say, LVDS) I/Os or ODT attributes to be used.

Table 11 • SmartFusion2 and IGLOO2 Quiescent Supply Current (V_{DD} = 1.2 V) – Typical Process

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC1	Non-Flash*Freeze	6.2	6.9	8.9	13.1	15.3	15.4	27.5	mA	Typical (T _J = 25 °C)
		24.0	28.4	40.6	67.8	80.6	81.4	144.7	mA	Commercial (T _J = 85 °C)
		35.2	41.9	60.5	102.1	121.4	122.6	219.1	mA	Industrial (T _J = 100 °C)

Table 53 • LVCMOS 1.8 V AC Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	R _{odt_cal}	75, 60, 50, 33, 25, 20	Ω

Table 54 • LVCMOS 1.8 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V _{TRIP}	0.9	V
Resistance for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	R _{ENT}	2k	Ω
Capacitive loading for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	C _{ENT}	5	pF
Capacitive loading for data path (T _{DP})	C _{LOAD}	5	pF

Table 55 • LVCMOS 1.8 V Transmitter Drive Strength Specifications

Output Drive Selection			V _{OH} (V)	V _{OL} (V)	IOH (at V _{OH})	IOL (at V _{OL})
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max	mA	mA
2 mA	2 mA	2 mA	V _{DDI} – 0.45	0.45	2	2
4 mA	4 mA	4 mA	V _{DDI} – 0.45	0.45	4	4
6 mA	6 mA	6 mA	V _{DDI} – 0.45	0.45	6	6
8 mA	8 mA	8 mA	V _{DDI} – 0.45	0.45	8	8
10 mA	10 mA	10 mA	V _{DDI} – 0.45	0.45	10	10
12 mA		12 mA	V _{DDI} – 0.45	0.45	12	12
		16 mA ¹	V _{DDI} – 0.45	0.45	16	16

1. 16 mA drive strengths, all slews, meets LPDDR JEDEC electrical compliance.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 1.71 V

Table 56 • LVCMOS 1.8 V Receiver Characteristics (Input Buffers)

	On-Die Termination (ODT)	T _{Py}		T _{PYS}		Unit
		–1	–Std	–1	–Std	
LVCMOS 1.8 V (for DDRIO I/O bank with Fixed Codes)	None	1.968	2.315	2.099	2.47	ns
	None	2.898	3.411	2.883	3.393	ns
	50	3.05	3.59	3.044	3.583	ns
	75	2.999	3.53	2.987	3.516	ns
LVCMOS 1.8 V (for MSIO I/O bank)	150	2.947	3.469	2.933	3.452	ns
	None	2.611	3.071	2.598	3.057	ns
	50	2.775	3.264	2.775	3.265	ns
	75	2.72	3.2	2.712	3.19	ns
LVCMOS 1.8 V (for MSIOD I/O bank)	150	2.666	3.137	2.655	3.123	ns

Table 57 • LVCMOS 1.8 V Transmitter Characteristics for DDRIO I/O Bank with Fixed Code (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	Medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	Medium fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	Fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4 mA	Slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	Medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	Medium fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	Fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6 mA	Slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	Medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	Medium fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	Fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns
8 mA	Slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns
	Medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	Medium fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	Fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10 mA	Slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	Medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	Medium fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	Fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12 mA	Slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	Medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	Medium fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	Fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16 mA	Slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	Medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	Medium fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	Fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 62 • LVCMOS 1.5 V DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC output logic high	VOH	$V_{DDI} \times 0.75$		V
DC output logic low	VOL		$V_{DDI} \times 0.25$	V

Table 63 • LVCMOS 1.5 V AC Minimum and Maximum Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D _{MAX}	235	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D _{MAX}	160	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	D _{MAX}	220	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 64 • LVCMOS 1.5 V AC Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CA L	75, 60, 50, 40	Ω

Table 65 • LVCMOS 1.5 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point	V _{TRIP}	0.75	V
Resistance for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	R _{ENT}	2K	Ω
Capacitive loading for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	C _{ENT}	5	pF
Capacitive loading for data path (T _{DP})	C _{LOAD}	5	pF

Table 66 • LVCMOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			V _{OH} (V)	V _{OL} (V)	IOH (at V _{OH}) mA	IOL (at V _{OL}) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	2	2
4 mA	4 mA	4 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	4	4
6 mA	6 mA	6 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	6	6
8 mA		8 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	8	8
		10 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	10	10
		12 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	12	12

Note: For a detailed I/V curve, use the corresponding IBIS models:
www.microsemi.com/soc/download/ibis/default.aspx.

Table 131 • SSTL15 DC Output Voltage Specification (for DDRIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DDR3/SSTL15 Class I (DDR3 Reduced Drive)				
DC output logic high	V_{OH}	$0.8 \times V_{DDI}$		V
DC output logic low	V_{OL}		$0.2 \times V_{DDI}$	V
Output minimum source DC current	I_{OH} at V_{OH}	6.5		mA
Output minimum sink current	I_{OL} at V_{OL}	-6.5		mA
DDR3/SSTL15 Class II (DDR3 Full Drive)				
DC output logic high	V_{OH}	$0.8 \times V_{DDI}$		V
DC output logic low	V_{OL}		$0.2 \times V_{DDI}$	V
Output minimum source DC current	I_{OH} at V_{OH}	7.6		mA
Output minimum sink current	I_{OL} at V_{OL}	-7.6		mA

Table 132 • SSTL15 DC Differential Voltage Specification (for DDRIO I/O Bank Only)

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID}	0.2	V

Note: To meet JEDEC electrical compliance, use DDR3 full drive transmitter.

Table 133 • SSTL15 AC SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF} (AC)	0.3		V
AC differential cross point voltage	V_x (AC)	$0.5 \times V_{DDI} - 0.150$	$0.5 \times V_{DDI} + 0.150$	V

Table 134 • SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	667	Mbps	AC loading: per JEDEC specifications

Table 135 • SSTL15 AC Calibrated Impedance Option (for DDRIO I/O Bank Only)

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	R_{REF}	34, 40	Ω	Reference resistor = 240 Ω
Effective impedance value (ODT)	R_{TT}	20, 30, 40, 60, 120	Ω	Reference resistor = 240 Ω

Table 144 • LPDDR AC Differential Voltage Specifications (for DDRIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF}	$0.6 \times V_{DDI}$		V
AC differential cross point voltage	V_x	$0.4 \times V_{DDI}$	$0.6 \times V_{DDI}$	V

Table 145 • LPDDR AC Specifications (for DDRIO I/O Bank Only)

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	400	Mbps	AC loading: per JEDEC specifications

Table 146 • LPDDR AC Calibrated Impedance Option (for DDRIO I/O Bank Only)

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	R_{REF}	20, 42	Ω	Reference resistor = 150 Ω
Effective impedance value (ODT)	R_{TT}	50, 70, 150	Ω	Reference resistor = 150 Ω

Table 147 • LPDDR AC Test Parameter Specifications (for DDRIO I/O Bank Only)

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.9	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for LPDDR (T_{DP})	R_{TT_TEST}	50	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	Ω

AC Switching Characteristics

Worst-case commercial conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, worst-case V_{DDI} .

Table 148 • LPDDR Receiver Characteristics for DDRIO I/O Bank with Fixed Codes

		T_{PY}		Unit
On-Die Termination (ODT)		-1	-Std	
Pseudo differential	None	1.568	1.845	ns
True differential	None	1.588	1.869	ns

Table 149 • LPDDR Reduced Drive for DDRIO I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ENZL}		T_{ENZH}		T_{ENHZ}		T_{ENLZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.383	2.804	2.23	2.623	2.229	2.622	2.202	2.591	2.201	2.59	ns
Differential	2.396	2.819	2.764	3.252	2.764	3.252	2.255	2.653	2.255	2.653	ns

Table 150 • LPDDR Full Drive for DDRIO I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ENZL}		T_{ENZH}		T_{ENHZ}		T_{ENLZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.171	2.555	2.17	2.554	ns
Differential	2.298	2.703	2.288	2.692	2.288	2.692	2.593	3.051	2.593	3.051	ns

Minimum and Maximum DC/AC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode

Table 151 • LPDDR-LVCMOS 1.8 V Mode Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.710	1.8	1.89	V

Table 152 • LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	V_{IH} (DC)	$0.65 \times V_{DDI}$	1.89	V
DC input logic high (for MSIO I/O bank)	V_{IH} (DC)	$0.65 \times V_{DDI}$	3.45	V
DC input logic low	V_{IL} (DC)	-0.3	$0.35 \times V_{DDI}$	V
Input current high ¹	I_{IH} (DC)			
Input current low ¹	I_{IL} (DC)			

1. See Table 24, page 22.

Table 153 • LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	$V_{DDI} - 0.45$		V
DC output logic low	V_{OL}		0.45	V

Table 154 • LPDDR-LVCMOS 1.8 V Minimum and Maximum AC Switching Speeds

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	400	Mbps	AC loading: 17pf load, 8 ma drive and above/all slew

Table 155 • LPDDR-LVCMOS 1.8 V Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CAL	75, 60, 50, 33, 25, 20	Ω

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$.

Table 180 • B-LVDS AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.738	3.221	ns
100	2.735	3.218	ns

Table 181 • B-LVDS AC Switching Characteristics for Receiver for MSIOD I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.495	2.934	ns
100	2.495	2.935	ns

Table 182 • B-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.258	2.656	2.343	2.756	2.329	2.74	2.12	2.494	2.123	2.497	ns

2.3.7.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum Input and Output Levels

Table 183 • M-LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage ¹	V_{DDI}	2.375	2.5	2.625	V

1. Only M-LVDS TYPE I is supported.

Table 184 • M-LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	2.925	V
Input current high ¹	I_{IH} (DC)			
Input current low ²	I_{IL} (DC)			

1. See Table 24, page 22.

Table 185 • M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V _{OH}	1.25	1.425	1.6	V
DC output logic low	V _{OL}	0.9	1.075	1.25	V

Table 186 • M-LVDS Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	V _{OD}	300	650	mV
Output common mode voltage (for MSIO I/O bank only)	V _{OCM}	0.3	2.1	V
Input common mode voltage	V _{ICM}	0.3	1.2	V
Input differential voltage	V _{ID}	50	2400	mV

Table 187 • M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D _{MAX}	500	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 188 • M-LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R _T	50	Ω

Table 189 • M-LVDS AC Test Parameter Specifications

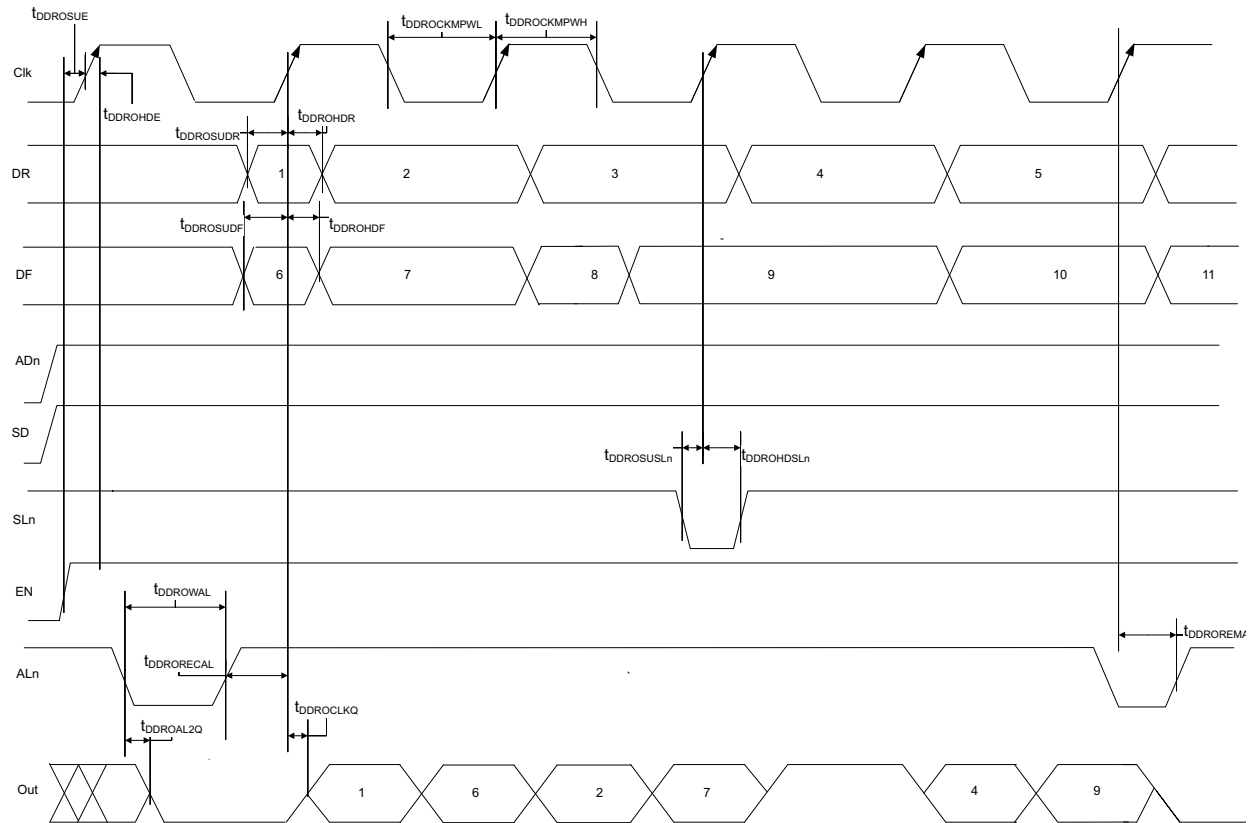
Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V _{TRIP}	Cross point	V
Resistance for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	R _{ENT}	2K	Ω
Capacitive loading for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	C _{ENT}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V

Table 190 • M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)

On-Die Termination (ODT)	T _{py}		Unit
	-1	-Std	
None	2.738	3.221	ns
100	2.735	3.218	ns

Figure 13 • Output DDR Timing Diagram**2.3.9.5 Timing Characteristics**

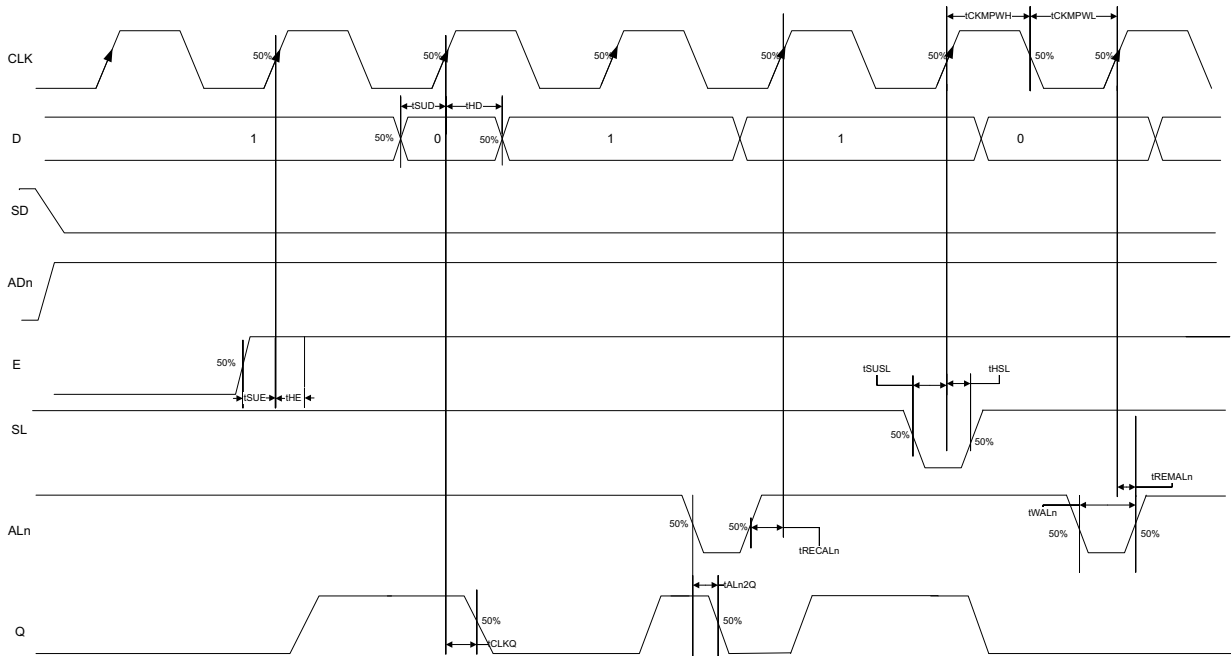
The following table lists the output DDR propagation delays in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 222 • Output DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDROCKLQ}$	Clock-to-out of DDR for output DDR	E, G	0.263	0.309	ns
$T_{DDROSUDF}$	Data_F data setup for output DDR	F, E	0.143	0.168	ns
$T_{DDROSUDR}$	Data_R data setup for output DDR	A, E	0.19	0.223	ns
$T_{DDROHDF}$	Data_F data hold for output DDR	F, E	0	0	ns
$T_{DDROHDR}$	Data_R data hold for output DDR	A, E	0	0	ns
$T_{DDROSUE}$	Enable setup for input DDR	B, E	0.419	0.493	ns
T_{DDROHE}	Enable hold for input DDR	B, E	0	0	ns
$T_{DDROSUSLn}$	Synchronous load setup for input DDR	D, E	0.196	0.231	ns
$T_{DDROHSLn}$	Synchronous load hold for input DDR	D, E	0	0	ns
$T_{DDROAL2Q}$	Asynchronous load-to-out for output DDR	C, G	0.528	0.621	ns
$T_{DDROREML}$	Asynchronous load removal time for output DDR	C, E	0	0	ns
$T_{DDRORECAL}$	Asynchronous load recovery time for output DDR	C, E	0.034	0.04	ns

The following figure shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

Figure 16 • Sequential Module Timing Diagram



2.3.10.3.1 Timing Characteristics

The following table lists the register delays in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 224 • Register Delays

Parameter	Symbol	-1	-Std	Unit
Clock-to-Q of the core register	T_{CLKQ}	0.108	0.127	ns
Data setup time for the core register	T_{SUD}	0.254	0.298	ns
Data hold time for the core register	T_{HD}	0	0	ns
Enable setup time for the core register	T_{SUE}	0.335	0.394	ns
Enable hold time for the core register	T_{HE}	0	0	ns
Synchronous load setup time for the core register	T_{SUSL}	0.335	0.394	ns
Synchronous load hold time for the core register	T_{HSL}	0	0	ns
Asynchronous Clear-to-Q of the core register (ADn = 1)	T_{ALN2Q}	0.473	0.556	ns
Asynchronous preset-to-Q of the core register (ADn = 0)		0.451	0.531	ns
Asynchronous load removal time for the core register	T_{RECALN}	0	0	ns
Asynchronous load recovery time for the core register	T_{RECALN}	0.353	0.415	ns
Asynchronous load minimum pulse width for the core register	T_{WALN}	0.266	0.313	ns
Clock minimum pulse width high for the core register	T_{CKMPWH}	0.065	0.077	ns
Clock minimum pulse width low for the core register	T_{CKMPWL}	0.139	0.164	ns

The following table lists the 010 device global resources in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 229 • 010 Device Global Resource

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.626	0.669	0.627	0.668	ns
Input high delay for global clock	T_{RCKH}	1.112	1.182	1.308	1.393	ns
Maximum skew for global clock	T_{RCKSW}		0.07		0.085	ns

The following table lists the 005 device global resources in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 230 • 005 Device Global Resource

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.625	0.66	0.628	0.66	ns
Input high delay for global clock	T_{RCKH}	1.126	1.187	1.325	1.397	ns
Maximum skew for global clock	T_{RCKSW}		0.061		0.072	ns

2.3.12 FPGA Fabric SRAM

See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for more information.

2.3.12.1 FPGA Fabric Large SRAM (LSRAM)

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 1K × 18 in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 231 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register			0.334		0.393	ns
Read access time without pipeline register	T_{CLK2Q}		2.273		2.674	ns
Access time with feed-through write timing			1.529		1.799	ns
Address setup time	T_{ADDRSU}	0.441		0.519		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.341		0.401		ns
Data hold time	T_{DHD}	0.107		0.126		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 8K × 2 in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 234 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register			0.32		0.377	ns
Read access time without pipeline register	T_{CLK2Q}		2.272		2.673	ns
Access time with feed-through write timing			1.511		1.778	ns
Address setup time	T_{ADDRSU}	0.612		0.72		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.33		0.388		ns
Data hold time	T_{DHD}	0.082		0.096		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		1.511		1.778	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.529		0.622		ns
Read enable hold time	T_{RDEHD}	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}		1.528		1.797	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.488		0.574		ns
Write enable hold time	T_{WEHD}	0.048		0.057		ns
Maximum frequency	F_{MAX}		400		340	MHz

Table 239 • μ SRAM (RAM128x9) in 128 × 9 Mode (continued)

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.982	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	-0.026		-0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 128 × 8 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 240 • μ SRAM (RAM128x8) in 128 × 8 Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 270 • Math Block with Input Register Used and Output in Bypass Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input register setup time	T_{MISU}	0.149		0.176		ns
Input register hold time	T_{MIHD}	0.185		0.218		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	0.08		0.094		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	-0.012		-0.014		ns
Asynchronous reset removal time	$T_{MARSTREM}$	-0.005		-0.005		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.088		0.104		ns
Input register clock to output delay	T_{MICQ}		2.52		2.964	ns
CDIN to output delay	$T_{MCDIN2Q}$		1.951		2.295	ns

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 271 • Math Block with Input and Output in Bypass Mode

Parameter	Symbol	-1	-Std	Unit
		Max	Max	
Input to output delay	T_{MIQ}	2.568	3.022	ns
CDIN to output delay	$T_{MCDIN2Q}$	1.951	2.295	ns

2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when $V_{DD} = 1.14\text{ V}$, $V_{PPNVM} = V_{PP} = 2.375\text{ V}$.

Table 272 • eNVM Read Performance

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
T_J	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$F_{MAXREAD}$	eNVM maximum read frequency	25	25	25	25	25	25	MHz

The following table lists the eNVM page programming in worst-case conditions when $V_{DD} = 1.14\text{ V}$, $V_{PPNVM} = V_{PP} = 2.375\text{ V}$.

Table 273 • eNVM Page Programming

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
T_J	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$T_{PAGEPGM}$	eNVM page programming time	40	40	40	40	40	40	ms

2.3.16 SRAM PUF

For more details on static random-access memory (SRAM) physical unclonable functions (PUF) services, see *AC434: Using SRAM PUF System Service in SmartFusion2 Application Note*.

The following table lists the SRAM PUF in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 274 • SRAM PUF

Service	PUF Off		PUF On		Unit
	Typ	Max	Typ	Max	
Create activation code	709.1	746.4	754.4	762.5	ms
Delete activation code	1329.3	1399.3	1414.1	1429.3	ms
Create intrinsic keycode	656.6	691.1	698.5	706.0	ms
Create extrinsic keycode	656.6	691.1	698.5	706.0	ms
Get number of keys	1.3	1.4	1.4	1.4	ms
Export (Kc0, Kc1)	998.0	1050.5	1061.7	1073.1	ms
Export 2 keycodes	2020.2	2126.5	2149.2	2172.3	ms
Export 4 keycodes	3065.7	3227.0	3261.3	3296.4	ms
Export 8 keycodes	5101.0	5369.5	5426.6	5485.0	ms
Export 16 keycodes	9212.1	9697.0	9800.1	9905.5	ms
Import (Kc0, Kc1)	39.7	41.8	42.2	42.7	ms
Import 2 keycodes	50.1	52.7	53.3	53.9	ms
Import 4 keycodes	60.6	63.8	64.5	65.2	ms
Import 8 keycodes	80.9	85.1	86.1	87.0	ms
Import 16 keycodes	123.8	130.4	131.7	133.2	ms
Delete keycode	552.5	581.6	587.8	594.1	ms
Fetch key	31.4	33.0	33.4	33.7	ms
Fetch ecc key	20.0	21.1	21.3	21.5	ms
Get seed	2.0	2.1	2.2	2.2	ms

2.3.21 Clock Conditioning Circuits (CCC)

The following table lists the CCC/PLL specifications in worst-case industrial conditions when $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 282 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification

Parameter	Min	Typ	Max	Unit	Conditions	
Clock conditioning circuitry input frequency F_{IN_CCC}	1		200	MHz	All CCC	
	0.032		200	MHz	32 kHz capable CCC	
Clock conditioning circuitry output frequency $F_{OUT_CCC}^1$	0.078		400	MHz		
PLL VCO frequency ²	500		1000	MHz		
Delay increments in programmable delay blocks		75	100	ps		
Number of programmable values in each programmable delay block			64			
Acquisition time		70	100	μ s	$F_{IN} \geq 1$ MHz	
		1	16	ms	$F_{IN} = 32$ kHz	
Input duty cycle (reference clock)					Internal Feedback	
	10		90	%	$1\text{ MHz} \leq F_{IN_CCC} \leq 25\text{ MHz}$	
	25		75	%	$25\text{ MHz} \leq F_{IN_CCC} \leq 100\text{ MHz}$	
	35		65	%	$100\text{ MHz} \leq F_{IN_CCC} \leq 150\text{ MHz}$	
	45		55	%	$150\text{ MHz} \leq F_{IN_CCC} \leq 200\text{ MHz}$	
					External Feedback (CCC, FPGA, Off-chip)	
	25		75	%	$1\text{ MHz} \leq F_{IN_CCC} \leq 25\text{ MHz}$	
	35		65	%	$25\text{ MHz} \leq F_{IN_CCC} \leq 35\text{ MHz}$	
	45		55	%	$35\text{ MHz} \leq F_{IN_CCC} \leq 50\text{ MHz}$	
	Output duty cycle	48		52	%	050 devices $F_{OUT} \leq 400\text{ MHz}$
		48		52	%	005, 010, and 025 devices $F_{OUT} < 350\text{ MHz}$
		46		54	%	005, 010, and 025 devices $350\text{ MHz} \leq F_{out} \leq 400\text{ MHz}$
48			52	%	060 and 090 devices $F_{OUT} \leq 100\text{ MHz}$	
44			52	%	060 and 090 devices $100\text{ MHz} \leq F_{OUT} \leq 400\text{ MHz}$	
48			52	%	150 devices $F_{OUT} \leq 120\text{ MHz}$	
45			52	%	150 devices $120\text{ MHz} \leq F_{OUT} \leq 400\text{ MHz}$	
Spread Spectrum Characteristics						
Modulation frequency range	25	35	50	k		
Modulation depth range	0		1.5	%		
Modulation depth control		0.5		%		

2.3.30 SerDes Electrical and Timing AC and DC Characteristics

PCIe is a high-speed, packet-based, point-to-point, low-pin-count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block.

The following table lists the transmitter parameters in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 296 • Transmitter Parameters

Symbol	Description	Min	Max	Unit
VTX-DIFF-PP	Differential swing (2.5 Gbps, 5.0 Gbps)	0.8	1.2	V
VTX-CM-AC-P	Output common mode voltage (2.5 Gbps)		20	mV
VTX-CM-AC-PP	Output common mode voltage (5.0 Gbps)		100	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%, 2.5 Gbps)	0.125		UI
	Rise and fall time (20% to 80%, 5.0 Gbps)	0.15		UI
ZTX-DIFF-DC	Output impedance—differential	80	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SerDes block (2.5 Gbps)		500 ps + 2 UI	ps
	Lane-to-lane TX skew within a SerDes block (5.0 Gbps)		500 ps + 4 UI	ps
RLTX-DIFF	Return loss differential mode (2.5 Gbps)	–10		dB
	Return loss differential mode (5.0 Gbps) 0.05 GHz to 1.25 GHz	–10		dB
	1.25 GHz to 2.5 GHz	–8		dB
RLTX-CM	Return loss common mode (2.5 Gbps, 5.0 Gbps)	–6		dB
TX-LOCK-RST	Transmit PLL lock time from reset		10	μs
VTX-AMP	100 mV setting	90	150	mV
	400 mV setting	320	480	mV
	800 mV setting	660	940	mV
	1200 mV setting	950	1400	mV