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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                                                   |
|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Active                                                                                                                                                            |
| Number of LABs/CLBs            | -                                                                                                                                                                 |
| Number of Logic Elements/Cells | 56520                                                                                                                                                             |
| Total RAM Bits                 | 1869824                                                                                                                                                           |
| Number of I/O                  | 207                                                                                                                                                               |
| Number of Gates                | -                                                                                                                                                                 |
| Voltage - Supply               | 1.14V ~ 2.625V                                                                                                                                                    |
| Mounting Type                  | Surface Mount                                                                                                                                                     |
| Operating Temperature          | -40°C ~ 100°C (TJ)                                                                                                                                                |
| Package / Case                 | 400-LFBGA                                                                                                                                                         |
| Supplier Device Package        | 400-VFBGA (17x17)                                                                                                                                                 |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/microchip-technology/m2gl060t-vf400i">https://www.e-xfl.com/product-detail/microchip-technology/m2gl060t-vf400i</a> |

# Contents

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|          |                                                               |          |
|----------|---------------------------------------------------------------|----------|
| <b>1</b> | <b>Revision History</b>                                       | <b>1</b> |
| 1.1      | Revision 11.0                                                 | 1        |
| 1.2      | Revision 10.0                                                 | 1        |
| 1.3      | Revision 9.0                                                  | 1        |
| 1.4      | Revision 8.0                                                  | 2        |
| 1.5      | Revision 7.0                                                  | 2        |
| 1.6      | Revision 6.0                                                  | 2        |
| 1.7      | Revision 5.0                                                  | 2        |
| 1.8      | Revision 4.0                                                  | 2        |
| 1.9      | Revision 3.0                                                  | 3        |
| 1.10     | Revision 2.0                                                  | 3        |
| 1.11     | Revision 1.0                                                  | 3        |
| <b>2</b> | <b>IGLOO2 FPGA and SmartFusion2 SoC FPGA</b>                  | <b>4</b> |
| 2.1      | Device Status                                                 | 4        |
| 2.2      | References                                                    | 5        |
| 2.3      | Electrical Specifications                                     | 5        |
| 2.3.1    | Operating Conditions                                          | 5        |
| 2.3.2    | Power Consumption                                             | 12       |
| 2.3.3    | Average Fabric Temperature and Voltage Derating Factors       | 14       |
| 2.3.4    | Timing Model                                                  | 15       |
| 2.3.5    | User I/O Characteristics                                      | 17       |
| 2.3.6    | Logic Element Specifications                                  | 75       |
| 2.3.7    | Global Resource Characteristics                               | 78       |
| 2.3.8    | FPGA Fabric SRAM                                              | 79       |
| 2.3.9    | Programming Times                                             | 94       |
| 2.3.10   | Math Block Timing Characteristics                             | 103      |
| 2.3.11   | Embedded NVM (eNVM) Characteristics                           | 104      |
| 2.3.12   | SRAM PUF                                                      | 105      |
| 2.3.13   | Non-Deterministic Random Bit Generator (NRBG) Characteristics | 106      |
| 2.3.14   | Cryptographic Block Characteristics                           | 106      |
| 2.3.15   | Crystal Oscillator                                            | 107      |
| 2.3.16   | On-Chip Oscillator                                            | 109      |
| 2.3.17   | Clock Conditioning Circuits (CCC)                             | 110      |
| 2.3.18   | JTAG                                                          | 112      |
| 2.3.19   | System Controller SPI Characteristics                         | 113      |
| 2.3.20   | Power-up to Functional Times                                  | 114      |
| 2.3.21   | DEVRST_N Characteristics                                      | 116      |
| 2.3.22   | DEVRST_N to Functional Times                                  | 116      |
| 2.3.23   | Flash*Freeze Timing Characteristics                           | 119      |
| 2.3.24   | DDR Memory Interface Characteristics                          | 120      |
| 2.3.25   | SFP Transceiver Characteristics                               | 120      |
| 2.3.26   | SerDes Electrical and Timing AC and DC Characteristics        | 121      |
| 2.3.27   | SmartFusion2 Specifications                                   | 123      |
| 2.3.28   | CAN Controller Characteristics                                | 128      |
| 2.3.29   | USB Characteristics                                           | 128      |
| 2.3.30   | MMUART Characteristics                                        | 129      |
| 2.3.31   | IGLOO2 Specifications                                         | 129      |

# Tables

|          |                                                                                                                        |    |
|----------|------------------------------------------------------------------------------------------------------------------------|----|
| Table 1  | IGLOO2 and SmartFusion2 Design Security Densities                                                                      | 4  |
| Table 2  | IGLOO2 and SmartFusion2 Data Security Densities                                                                        | 4  |
| Table 3  | Absolute Maximum Ratings                                                                                               | 5  |
| Table 4  | Recommended Operating Conditions                                                                                       | 6  |
| Table 5  | FPGA Operating Limits                                                                                                  | 7  |
| Table 6  | Embedded Operating Flash Limits                                                                                        | 8  |
| Table 7  | Device Storage Temperature and Retention                                                                               | 8  |
| Table 8  | High Temperature Data Retention (HTR) Lifetime                                                                         | 8  |
| Table 9  | Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices                                                          | 10 |
| Table 10 | Quiescent Supply Current Characteristics                                                                               | 12 |
| Table 11 | SmartFusion2 and IGLOO2 Quiescent Supply Current ( $V_{DD} = 1.2\text{ V}$ ) – Typical Process                         | 12 |
| Table 12 | Currents During Program Cycle, $0\text{ }^{\circ}\text{C} \leq T_J \leq 85\text{ }^{\circ}\text{C}$ – Typical Process  | 13 |
| Table 13 | Currents During Verify Cycle, $0\text{ }^{\circ}\text{C} \leq T_J \leq 85\text{ }^{\circ}\text{C}$ – Typical Process   | 13 |
| Table 14 | SmartFusion2 and IGLOO2 Quiescent Supply Current ( $V_{DD} = 1.26\text{ V}$ ) – Worst-Case Process                     | 13 |
| Table 15 | Average Junction Temperature and Voltage Derating Factors for Fabric Timing Delays                                     | 14 |
| Table 16 | Inrush Currents at Power up, $-40\text{ }^{\circ}\text{C} \leq T_J \leq 100\text{ }^{\circ}\text{C}$ – Typical Process | 14 |
| Table 17 | Timing Model Parameters                                                                                                | 15 |
| Table 18 | Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions                               | 19 |
| Table 19 | Maximum Data Rate Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions                         | 20 |
| Table 20 | Maximum Data Rate Summary Table for Differential I/O in Worst-Case Industrial Conditions                               | 20 |
| Table 21 | Maximum Frequency Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions                               | 20 |
| Table 22 | Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions                         | 21 |
| Table 23 | Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions                               | 21 |
| Table 24 | Input Capacitance, Leakage Current, and Ramp Time                                                                      | 22 |
| Table 25 | I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank                                                              | 22 |
| Table 26 | I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank                                                               | 23 |
| Table 27 | I/O Weak Pull-up/Pull-down Resistances for MSIOD I/O Bank                                                              | 23 |
| Table 28 | Schmitt Trigger Input Hysteresis                                                                                       | 23 |
| Table 29 | LVTTL/LVC MOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)                          | 24 |
| Table 30 | LVTTL/LVC MOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)                                     | 24 |
| Table 31 | LVC MOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)                                       | 24 |
| Table 32 | LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)                                         | 24 |
| Table 33 | LVTTL/LVC MOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)                                      | 24 |
| Table 34 | LVTTL/LVC MOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)                                         | 25 |
| Table 35 | LVTTL/LVC MOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)                        | 25 |
| Table 36 | LVTTL/LVC MOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only)                                | 25 |
| Table 37 | LVTTL/LVC MOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank                                        | 25 |
| Table 38 | LVC MOS 2.5 V DC Recommended DC Operating Conditions                                                                   | 26 |
| Table 39 | LVC MOS 2.5 V DC Input Voltage Specification                                                                           | 26 |
| Table 40 | LVC MOS 2.5 V DC Output Voltage Specification                                                                          | 26 |
| Table 41 | LVC MOS 2.5 V AC Minimum and Maximum Switching Speed                                                                   | 26 |
| Table 42 | LVC MOS 2.5 V AC Calibrated Impedance Option                                                                           | 26 |
| Table 43 | LVC MOS 2.5 V Receiver Characteristics (Input Buffers)                                                                 | 27 |
| Table 44 | LVC MOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)                                 | 27 |
| Table 45 | LVC MOS 2.5 V AC Test Parameter Specifications                                                                         | 27 |
| Table 46 | LVC MOS 2.5 V Transmitter Drive Strength Specifications                                                                | 27 |
| Table 47 | LVC MOS 2.5 V Transmitter Characteristics for MSIO Bank (Output and Tristate Buffers)                                  | 28 |
| Table 48 | LVC MOS 1.8 V DC Recommended Operating Conditions                                                                      | 29 |
| Table 49 | LVC MOS 1.8 V DC Input Voltage Specification                                                                           | 29 |
| Table 50 | LVC MOS 1.8 V DC Output Voltage Specification                                                                          | 29 |

|           |                                                                                                            |    |
|-----------|------------------------------------------------------------------------------------------------------------|----|
| Table 51  | LVC MOS 1.8 V Minimum and Maximum AC Switching Speed                                                       | 29 |
| Table 52  | LVC MOS 2.5 V Transmitter Characteristics for MSIOD Bank (Output and Tristate Buffers)                     | 29 |
| Table 53  | LVC MOS 1.8 V Receiver Characteristics (Input Buffers)                                                     | 30 |
| Table 54  | LVC MOS 1.8 V AC Calibrated Impedance Option                                                               | 30 |
| Table 55  | LVC MOS 1.8 V AC Test Parameter Specifications                                                             | 30 |
| Table 56  | LVC MOS 1.8 V Transmitter Drive Strength Specifications                                                    | 30 |
| Table 57  | LVC MOS 1.8 V Transmitter Characteristics for DDRIO I/O Bank with Fixed Code (Output and Tristate Buffers) | 31 |
| Table 58  | LVC MOS 1.5 V DC Recommended Operating Conditions                                                          | 32 |
| Table 59  | LVC MOS 1.5 V DC Input Voltage Specification                                                               | 32 |
| Table 60  | LVC MOS 1.8 V Transmitter Characteristics for MSIO I/O Bank                                                | 32 |
| Table 61  | LVC MOS 1.8 V Transmitter Characteristics for MSIOD I/O Bank                                               | 32 |
| Table 62  | LVC MOS 1.5 V DC Output Voltage Specification                                                              | 33 |
| Table 63  | LVC MOS 1.5 V AC Minimum and Maximum Switching Speed                                                       | 33 |
| Table 64  | LVC MOS 1.5 V AC Calibrated Impedance Option                                                               | 33 |
| Table 65  | LVC MOS 1.5 V AC Test Parameter Specifications                                                             | 33 |
| Table 66  | LVC MOS 1.5 V Transmitter Drive Strength Specifications                                                    | 33 |
| Table 67  | LVC MOS 1.5 V Receiver Characteristics for DDRIO I/O Bank with Fixed Codes (Input Buffers)                 | 34 |
| Table 68  | LVC MOS 1.5 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)                                   | 34 |
| Table 69  | LVC MOS 1.5 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)                                  | 34 |
| Table 70  | LVC MOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)                 | 34 |
| Table 71  | LVC MOS 1.5 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)                  | 35 |
| Table 72  | LVC MOS 1.2 V DC Recommended DC Operating Conditions                                                       | 36 |
| Table 73  | LVC MOS 1.2 V DC Input Voltage Specification                                                               | 36 |
| Table 74  | LVC MOS 1.2 V DC Output Voltage Specification                                                              | 36 |
| Table 75  | LVC MOS 1.2 V Minimum and Maximum AC Switching Speed                                                       | 36 |
| Table 76  | LVC MOS 1.5 V Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)                 | 36 |
| Table 77  | LVC MOS 1.2 V Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)                  | 37 |
| Table 78  | LVC MOS 1.2 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)                                   | 37 |
| Table 79  | LVC MOS 1.2 V AC Calibrated Impedance Option                                                               | 37 |
| Table 80  | LVC MOS 1.2 V AC Test Parameter Specifications                                                             | 37 |
| Table 81  | LVC MOS 1.2 V Transmitter Drive Strength Specifications                                                    | 37 |
| Table 82  | LVC MOS 1.2 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)                                  | 38 |
| Table 83  | LVC MOS 1.2 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)                 | 38 |
| Table 84  | LVC MOS 1.2 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)                  | 38 |
| Table 85  | PCI/PCI-X DC Recommended Operating Conditions                                                              | 39 |
| Table 86  | PCI/PCI-X DC Input Voltage Specification                                                                   | 39 |
| Table 87  | PCI/PCI-X DC Output Voltage Specification                                                                  | 39 |
| Table 88  | PCI/PCI-X Minimum and Maximum AC Switching Speed                                                           | 39 |
| Table 89  | PCI/PCI-X AC Test Parameter Specifications                                                                 | 39 |
| Table 90  | LVC MOS 1.2 V Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)                 | 39 |
| Table 91  | PCI/PCIX AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)                       | 40 |
| Table 92  | PCI/PCIX AC Switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)      | 40 |
| Table 93  | HSTL Recommended DC Operating Conditions                                                                   | 40 |
| Table 94  | HSTL DC Input Voltage Specification                                                                        | 40 |
| Table 95  | HSTL DC Output Voltage Specification Applicable to DDRIO I/O Bank Only                                     | 41 |
| Table 96  | HSTL DC Differential Voltage Specification                                                                 | 41 |
| Table 97  | HSTL AC Differential Voltage Specifications                                                                | 41 |
| Table 98  | HSTL Minimum and Maximum AC Switching Speed                                                                | 41 |
| Table 99  | HSTL Impedance Specification                                                                               | 41 |
| Table 100 | HSTL Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)                           | 42 |
| Table 101 | HSTL Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)                          | 42 |
| Table 102 | HSTL AC Test Parameter Specification                                                                       | 42 |
| Table 103 | DDR1/SSTL2 DC Recommended Operating Conditions                                                             | 43 |
| Table 104 | DDR1/SSTL2 DC Input Voltage Specification                                                                  | 43 |
| Table 105 | DDR1/SSTL2 DC Output Voltage Specification                                                                 | 43 |
| Table 106 | DDR1/SSTL2 DC Differential Voltage Specification                                                           | 43 |
| Table 107 | SSTL2 Receiver Characteristics for DDRIO I/O Bank (Input Buffers)                                          | 44 |

|           |                                                                                                           |    |
|-----------|-----------------------------------------------------------------------------------------------------------|----|
| Table 161 | LVDS DC Input Voltage Specification                                                                       | 55 |
| Table 162 | LVDS25 Receiver Characteristics for MSIO I/O Bank (Input Buffers)                                         | 56 |
| Table 163 | LVDS DC Output Voltage Specification                                                                      | 56 |
| Table 164 | LVDS DC Differential Voltage Specification                                                                | 56 |
| Table 165 | LVDS Minimum and Maximum AC Switching Speed                                                               | 56 |
| Table 166 | LVDS AC Impedance Specifications                                                                          | 56 |
| Table 167 | LVDS AC Test Parameter Specifications                                                                     | 56 |
| Table 168 | LVDS33 Receiver Characteristics for MSIO I/O Bank (Input Buffers)                                         | 57 |
| Table 169 | LVDS33 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)                        | 57 |
| Table 170 | LVDS25 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)                                        | 57 |
| Table 171 | LVDS25 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)                        | 57 |
| Table 172 | LVDS25 Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)                       | 57 |
| Table 173 | B-LVDS Recommended DC Operating Conditions                                                                | 58 |
| Table 174 | B-LVDS DC Input Voltage Specification                                                                     | 58 |
| Table 175 | B-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)                                           | 58 |
| Table 176 | B-LVDS DC Differential Voltage Specification                                                              | 58 |
| Table 177 | B-LVDS Minimum and Maximum AC Switching Speed                                                             | 58 |
| Table 178 | B-LVDS AC Impedance Specifications                                                                        | 58 |
| Table 179 | B-LVDS AC Test Parameter Specifications                                                                   | 58 |
| Table 180 | B-LVDS AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)                        | 59 |
| Table 181 | B-LVDS AC Switching Characteristics for Receiver for MSIOD I/O Bank (Input Buffers)                       | 59 |
| Table 182 | B-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)     | 59 |
| Table 183 | M-LVDS Recommended DC Operating Conditions                                                                | 59 |
| Table 184 | M-LVDS DC Input Voltage Specification                                                                     | 59 |
| Table 185 | M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)                      | 60 |
| Table 186 | M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)                     | 60 |
| Table 187 | M-LVDS Differential Voltage Specification                                                                 | 60 |
| Table 188 | M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank                                           | 60 |
| Table 189 | M-LVDS AC Impedance Specifications                                                                        | 60 |
| Table 190 | M-LVDS AC Test Parameter Specifications                                                                   | 60 |
| Table 191 | Mini-LVDS Recommended DC Operating Conditions                                                             | 61 |
| Table 192 | Mini-LVDS DC Input Voltage Specification                                                                  | 61 |
| Table 193 | Mini-LVDS DC Output Voltage Specification                                                                 | 61 |
| Table 194 | Mini-LVDS DC Differential Voltage Specification                                                           | 61 |
| Table 195 | Mini-LVDS Minimum and Maximum AC Switching Speed                                                          | 61 |
| Table 196 | M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)                     | 61 |
| Table 197 | M-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)     | 61 |
| Table 198 | Mini-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)                   | 62 |
| Table 199 | Mini-LVDS AC Switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)    | 62 |
| Table 200 | Mini-LVDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers) | 62 |
| Table 201 | Mini-LVDS AC Impedance Specifications                                                                     | 62 |
| Table 202 | Mini-LVDS AC Test Parameter Specifications                                                                | 62 |
| Table 203 | RSDS Recommended DC Operating Conditions                                                                  | 63 |
| Table 204 | RSDS DC Input Voltage Specification                                                                       | 63 |
| Table 205 | RSDS DC Output Voltage Specification                                                                      | 63 |
| Table 206 | RSDS Differential Voltage Specification                                                                   | 63 |
| Table 207 | RSDS Minimum and Maximum AC Switching Speed                                                               | 63 |
| Table 208 | RSDS AC Impedance Specifications                                                                          | 63 |
| Table 209 | RSDS AC Test Parameter Specifications                                                                     | 63 |
| Table 210 | RSDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)                        | 64 |
| Table 211 | RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)                       | 64 |
| Table 212 | RSDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)       | 64 |
| Table 213 | RSDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)      | 64 |

## 2 IGLOO2 FPGA and SmartFusion2 SoC FPGA

Microsemi's mainstream SmartFusion<sup>®</sup>2 SoC and IGLOO<sup>®</sup>2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated math blocks, multiple embedded memory blocks, and high-performance SerDes communication interfaces on a single chip. Both families benefit from low-power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to 5 MBs of embedded RAM, up to 16 SerDes lanes, and up to four PCI Express Gen 2 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 devices integrate an entire low-power, real-time microcontroller subsystem (MSS) with a rich set of industry-standard peripherals including Ethernet, USB, and CAN, while IGLOO2 devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

### 2.1 Device Status

The following table shows the design security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

**Table 1 • IGLOO2 and SmartFusion2 Design Security Densities**

| Design Security Device Densities | Status     |
|----------------------------------|------------|
| 005                              | Production |
| 010, 010T                        | Production |
| 025, 025T                        | Production |
| 050, 050T                        | Production |
| 060, 060T                        | Production |
| 090, 090T                        | Production |
| 150, 150T                        | Production |

The following table shows the data security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

**Table 2 • IGLOO2 and SmartFusion2 Data Security Densities**

| Data Security Device Densities | Status     |
|--------------------------------|------------|
| 005S                           | Production |
| 010TS                          | Production |
| 025TS                          | Production |
| 050TS                          | Production |
| 060TS                          | Production |
| 090TS                          | Production |
| 150TS                          | Production |

## 2.3.2 Power Consumption

The following sections describe the power consumptions of the devices.

### 2.3.2.1 Quiescent Supply Current

**Table 10 • Quiescent Supply Current Characteristics**

| Power Supplies/Blocks                                                                 | Modes and Configurations |              |
|---------------------------------------------------------------------------------------|--------------------------|--------------|
|                                                                                       | Non-Flash*Freeze         | Flash*Freeze |
| FPGA Core                                                                             | On                       | Off          |
| V <sub>DD</sub> /SERDES_[01]_VDD <sup>1</sup>                                         | On                       | On           |
| V <sub>PP</sub> /V <sub>PPNVM</sub>                                                   | On                       | On           |
| HPMS_MDDR_PLL_VDDA/FDDR_PLL_VDDA/<br>CCC_XX[01]_PLL_VDDA/PLL0_PLL1_HPMS_MDDR_VDD<br>A | 0 V                      | 0 V          |
| SERDES_[01]_PLL_VDDA <sup>2</sup>                                                     | 0 V                      | 0 V          |
| SERDES_[01]_L[0123]_VDDAPLL/VDD_2V5 <sup>2</sup>                                      | On                       | On           |
| SERDES_[01]_L[0123]_VDDAIIO <sup>2</sup>                                              | On                       | On           |
| V <sub>DDI<sub>x</sub></sub> <sup>3, 4</sup>                                          | On                       | On           |
| V <sub>REFx</sub>                                                                     | On                       | On           |
| MSSDDR CLK                                                                            | 32 kHz                   | 32 kHz       |
| RAM                                                                                   | On                       | Sleep state  |
| System controller                                                                     | 50 MHz                   | 50 MHz       |
| 50 MHz oscillator (enable/disable)                                                    | Enable                   | Disabled     |
| 1 MHz oscillator (enable/disable)                                                     | Disabled                 | Disabled     |
| Crystal oscillator (enable/disable)                                                   | Disabled                 | Disabled     |

1. SERDES\_[01]\_VDD Power Supply is shorted to V<sub>DD</sub>.
2. SerDes and DDR blocks to be unused.
3. V<sub>DDI<sub>x</sub></sub> has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate V<sub>DDI</sub> bank supplies. For details on bank power supplies, see "Recommendation for Unused Bank Supplies" table in the *AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.
4. No Differential (that is to say, LVDS) I/Os or ODT attributes to be used.

**Table 11 • SmartFusion2 and IGLOO2 Quiescent Supply Current (V<sub>DD</sub> = 1.2 V) – Typical Process**

| Symbol | Modes            | 005  | 010  | 025  | 050   | 060   | 090   | 150   | Unit | Conditions                           |
|--------|------------------|------|------|------|-------|-------|-------|-------|------|--------------------------------------|
| IDC1   | Non-Flash*Freeze | 6.2  | 6.9  | 8.9  | 13.1  | 15.3  | 15.4  | 27.5  | mA   | Typical (T <sub>J</sub> = 25 °C)     |
|        |                  | 24.0 | 28.4 | 40.6 | 67.8  | 80.6  | 81.4  | 144.7 | mA   | Commercial (T <sub>J</sub> = 85 °C)  |
|        |                  | 35.2 | 41.9 | 60.5 | 102.1 | 121.4 | 122.6 | 219.1 | mA   | Industrial (T <sub>J</sub> = 100 °C) |

**Table 15 • Inrush Currents at Power up,  $-40\text{ }^{\circ}\text{C} \leq T_J \leq 100\text{ }^{\circ}\text{C}$  – Typical Process**

| Power Supplies  | Voltage (V) | 005 | 010 | 025 | 050 | 060 | 090 | 150 | Unit |
|-----------------|-------------|-----|-----|-----|-----|-----|-----|-----|------|
| $V_{DD}$        | 1.26        | 25  | 32  | 38  | 48  | 45  | 77  | 109 | mA   |
| $V_{PP}$        | 3.46        | 33  | 49  | 36  | 180 | 13  | 36  | 51  | mA   |
| $V_{DDI}$       | 2.62        | 134 | 141 | 161 | 187 | 93  | 272 | 388 | mA   |
| Number of banks |             | 7   | 8   | 8   | 10  | 10  | 9   | 19  |      |

### 2.3.3 Average Fabric Temperature and Voltage Derating Factors

The following table lists the average temperature and voltage derating factors for fabric timing delays normalized to  $T_J = 85\text{ }^{\circ}\text{C}$ , in worst-case  $V_{DD} = 1.14\text{ V}$ .

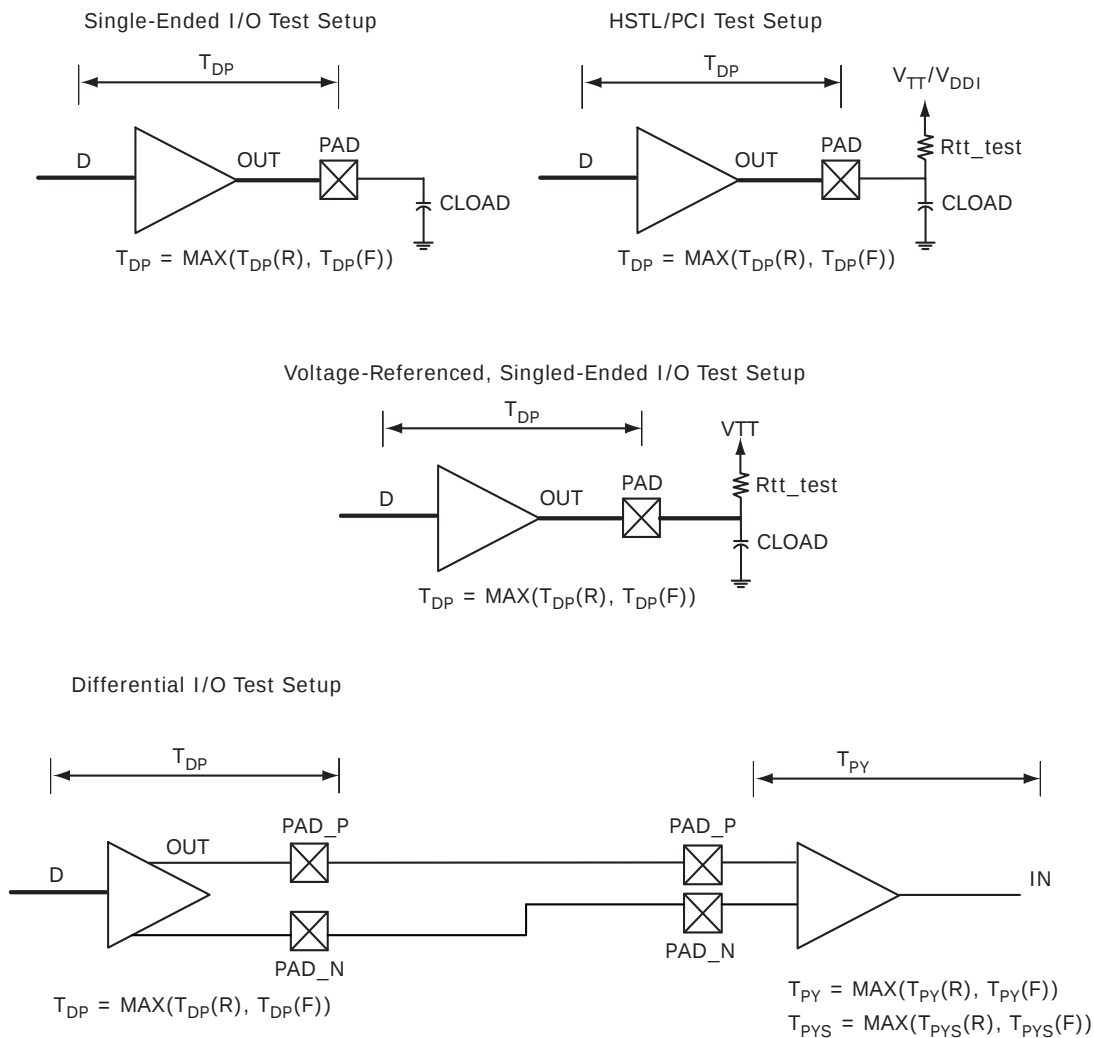
**Table 16 • Average Junction Temperature and Voltage Derating Factors for Fabric Timing Delays**

| Array Voltage $V_{DD}$ (V) | $-40\text{ }^{\circ}\text{C}$ | $0\text{ }^{\circ}\text{C}$ | $25\text{ }^{\circ}\text{C}$ | $70\text{ }^{\circ}\text{C}$ | $85\text{ }^{\circ}\text{C}$ | $100\text{ }^{\circ}\text{C}$ |
|----------------------------|-------------------------------|-----------------------------|------------------------------|------------------------------|------------------------------|-------------------------------|
| 1.14                       | 0.83                          | 0.89                        | 0.92                         | 0.98                         | <b>1.00</b>                  | 1.02                          |
| 1.2                        | 0.75                          | 0.80                        | 0.83                         | 0.89                         | 0.91                         | 0.93                          |
| 1.26                       | 0.69                          | 0.73                        | 0.76                         | 0.81                         | 0.83                         | 0.85                          |

### 2.3.5.2 Output Buffer and AC Loading

The following figure shows the output buffer and AC loading.

**Figure 4 • Output Buffer AC Loading**



**Table 53 • LVCMOS 1.8 V AC Calibrated Impedance Option**

| Parameter                                                         | Symbol               | Typ                    | Unit |
|-------------------------------------------------------------------|----------------------|------------------------|------|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | R <sub>odt_cal</sub> | 75, 60, 50, 33, 25, 20 | Ω    |

**Table 54 • LVCMOS 1.8 V AC Test Parameter Specifications**

| Parameter                                                                                                   | Symbol            | Typ | Unit |
|-------------------------------------------------------------------------------------------------------------|-------------------|-----|------|
| Measuring/trip point for data path                                                                          | V <sub>TRIP</sub> | 0.9 | V    |
| Resistance for enable path (T <sub>ZH</sub> , T <sub>ZL</sub> , T <sub>HZ</sub> , T <sub>LZ</sub> )         | R <sub>ENT</sub>  | 2k  | Ω    |
| Capacitive loading for enable path (T <sub>ZH</sub> , T <sub>ZL</sub> , T <sub>HZ</sub> , T <sub>LZ</sub> ) | C <sub>ENT</sub>  | 5   | pF   |
| Capacitive loading for data path (T <sub>DP</sub> )                                                         | C <sub>LOAD</sub> | 5   | pF   |

**Table 55 • LVCMOS 1.8 V Transmitter Drive Strength Specifications**

| Output Drive Selection |                |                    | V <sub>OH</sub> (V)     | V <sub>OL</sub> (V) | IOH (at V <sub>OH</sub> ) | IOL (at V <sub>OL</sub> ) |
|------------------------|----------------|--------------------|-------------------------|---------------------|---------------------------|---------------------------|
| MSIO I/O Bank          | MSIOD I/O Bank | DDRIO I/O Bank     | Min                     | Max                 | mA                        | mA                        |
| 2 mA                   | 2 mA           | 2 mA               | V <sub>DDI</sub> – 0.45 | 0.45                | 2                         | 2                         |
| 4 mA                   | 4 mA           | 4 mA               | V <sub>DDI</sub> – 0.45 | 0.45                | 4                         | 4                         |
| 6 mA                   | 6 mA           | 6 mA               | V <sub>DDI</sub> – 0.45 | 0.45                | 6                         | 6                         |
| 8 mA                   | 8 mA           | 8 mA               | V <sub>DDI</sub> – 0.45 | 0.45                | 8                         | 8                         |
| 10 mA                  | 10 mA          | 10 mA              | V <sub>DDI</sub> – 0.45 | 0.45                | 10                        | 10                        |
| 12 mA                  |                | 12 mA              | V <sub>DDI</sub> – 0.45 | 0.45                | 12                        | 12                        |
|                        |                | 16 mA <sup>1</sup> | V <sub>DDI</sub> – 0.45 | 0.45                | 16                        | 16                        |

1. 16 mA drive strengths, all slews, meets LPDDR JEDEC electrical compliance.

### AC Switching Characteristics

Worst commercial-case conditions: T<sub>J</sub> = 85 °C, V<sub>DD</sub> = 1.14 V, V<sub>DDI</sub> = 1.71 V

**Table 56 • LVCMOS 1.8 V Receiver Characteristics (Input Buffers)**

|                                                                     | On-Die Termination (ODT) | T <sub>Py</sub> |       | T <sub>PYS</sub> |       | Unit |
|---------------------------------------------------------------------|--------------------------|-----------------|-------|------------------|-------|------|
|                                                                     |                          | –1              | –Std  | –1               | –Std  |      |
| <b>LVCMOS 1.8 V</b><br><b>(for DDRIO I/O bank with Fixed Codes)</b> | None                     | 1.968           | 2.315 | 2.099            | 2.47  | ns   |
|                                                                     | None                     | 2.898           | 3.411 | 2.883            | 3.393 | ns   |
|                                                                     | 50                       | 3.05            | 3.59  | 3.044            | 3.583 | ns   |
|                                                                     | 75                       | 2.999           | 3.53  | 2.987            | 3.516 | ns   |
| <b>LVCMOS 1.8 V</b><br><b>(for MSIO I/O bank)</b>                   | 150                      | 2.947           | 3.469 | 2.933            | 3.452 | ns   |
|                                                                     | None                     | 2.611           | 3.071 | 2.598            | 3.057 | ns   |
|                                                                     | 50                       | 2.775           | 3.264 | 2.775            | 3.265 | ns   |
|                                                                     | 75                       | 2.72            | 3.2   | 2.712            | 3.19  | ns   |
| <b>LVCMOS 1.8 V</b><br><b>(for MSIOD I/O bank)</b>                  | 150                      | 2.666           | 3.137 | 2.655            | 3.123 | ns   |

**Table 82 • LVCMOS 1.2 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

| On-Die Termination (ODT) | T <sub>PY</sub> |       | T <sub>PYS</sub> |       | Unit |
|--------------------------|-----------------|-------|------------------|-------|------|
|                          | -1              | -Std  | -1               | -Std  |      |
| None                     | 4.154           | 4.887 | 4.114            | 4.84  | ns   |
| 50                       | 6.918           | 8.139 | 6.806            | 8.008 | ns   |
| 75                       | 5.613           | 6.603 | 5.533            | 6.509 | ns   |
| 150                      | 4.716           | 5.549 | 4.657            | 5.479 | ns   |

**Table 83 • LVCMOS 1.2 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | T <sub>DP</sub> |       | T <sub>ZL</sub> |       | T <sub>ZH</sub> |       | T <sub>HZ</sub> <sup>1</sup> |       | T <sub>LZ</sub> <sup>1</sup> |       | Unit |
|------------------------|--------------|-----------------|-------|-----------------|-------|-----------------|-------|------------------------------|-------|------------------------------|-------|------|
|                        |              | -1              | -Std  | -1              | -Std  | -1              | -Std  | -1                           | -Std  | -1                           | -Std  |      |
| 2 mA                   | Slow         | 6.713           | 7.897 | 5.362           | 6.308 | 6.723           | 7.909 | 7.233                        | 8.51  | 6.375                        | 7.499 | ns   |
|                        | Medium       | 5.912           | 6.955 | 4.616           | 5.43  | 5.915           | 6.959 | 6.887                        | 8.102 | 6.009                        | 7.069 | ns   |
|                        | Medium fast  | 5.5             | 6.469 | 4.231           | 4.978 | 5.5             | 6.471 | 6.672                        | 7.849 | 5.835                        | 6.865 | ns   |
|                        | Fast         | 5.462           | 6.426 | 4.194           | 4.935 | 5.463           | 6.427 | 6.646                        | 7.819 | 5.828                        | 6.857 | ns   |
| 4 mA                   | Slow         | 6.109           | 7.186 | 4.708           | 5.539 | 6.098           | 7.174 | 8.005                        | 9.418 | 7.033                        | 8.274 | ns   |
|                        | Medium       | 5.355           | 6.299 | 4.034           | 4.746 | 5.338           | 6.28  | 7.637                        | 8.985 | 6.672                        | 7.849 | ns   |
|                        | Medium fast  | 4.953           | 5.826 | 3.685           | 4.336 | 4.932           | 5.802 | 7.44                         | 8.752 | 6.499                        | 7.646 | ns   |
|                        | Fast         | 4.911           | 5.777 | 3.658           | 4.303 | 4.89            | 5.754 | 7.427                        | 8.737 | 6.488                        | 7.632 | ns   |
| 6 mA                   | Slow         | 5.89            | 6.929 | 4.506           | 5.301 | 5.874           | 6.911 | 8.337                        | 9.808 | 7.315                        | 8.605 | ns   |
|                        | Medium       | 5.176           | 6.089 | 3.862           | 4.543 | 5.155           | 6.065 | 7.986                        | 9.394 | 6.943                        | 8.168 | ns   |
|                        | Medium fast  | 4.792           | 5.637 | 3.523           | 4.145 | 4.765           | 5.606 | 7.808                        | 9.186 | 6.775                        | 7.97  | ns   |
|                        | Fast         | 4.754           | 5.593 | 3.486           | 4.101 | 4.728           | 5.563 | 7.777                        | 9.149 | 6.769                        | 7.963 | ns   |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 84 • LVCMOS 1.2 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | T <sub>DP</sub> |       | T <sub>ZL</sub> |       | T <sub>ZH</sub> |       | T <sub>HZ</sub> <sup>1</sup> |        | T <sub>LZ</sub> <sup>1</sup> |        | Unit |
|------------------------|--------------|-----------------|-------|-----------------|-------|-----------------|-------|------------------------------|--------|------------------------------|--------|------|
|                        |              | -1              | -Std  | -1              | -Std  | -1              | -Std  | -1                           | -Std   | -1                           | -Std   |      |
| 2 mA                   | Slow         | 6.746           | 7.937 | 7.458           | 8.774 | 8.172           | 9.614 | 9.867                        | 11.608 | 8.393                        | 9.874  | ns   |
| 4 mA                   | Slow         | 7.068           | 8.315 | 6.678           | 7.857 | 7.474           | 8.793 | 10.986                       | 12.924 | 9.043                        | 10.638 | ns   |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 95 • HSTL DC Output Voltage Specification Applicable to DDRIO I/O Bank Only**

| Parameter                                                   | Symbol               | Min             | Max | Unit |
|-------------------------------------------------------------|----------------------|-----------------|-----|------|
| <b>HSTL Class I</b>                                         |                      |                 |     |      |
| DC output logic high                                        | $V_{OH}$             | $V_{DDI} - 0.4$ |     | V    |
| DC output logic low                                         | $V_{OL}$             |                 | 0.4 | V    |
| Output minimum source DC current (MSIO and DDRIO I/O banks) | $I_{OH}$ at $V_{OH}$ | -8.0            |     | mA   |
| Output minimum sink current (MSIO and DDRIO I/O banks)      | $I_{OL}$ at $V_{OL}$ | 8.0             |     | mA   |
| <b>HSTL Class II</b>                                        |                      |                 |     |      |
| DC output logic high                                        | $V_{OH}$             | $V_{DDI} - 0.4$ |     | V    |
| DC output logic low                                         | $V_{OL}$             |                 | 0.4 | V    |
| Output minimum source DC current                            | $I_{OH}$ at $V_{OH}$ | -16.0           |     | mA   |
| Output minimum sink current                                 | $I_{OL}$ at $V_{OL}$ | 16.0            |     | mA   |

**Table 96 • HSTL DC Differential Voltage Specification**

| Parameter                     | Symbol        | Min | Unit |
|-------------------------------|---------------|-----|------|
| DC input differential voltage | $V_{ID}$ (DC) | 0.2 | V    |

**Table 97 • HSTL AC Differential Voltage Specifications**

| Parameter                           | Symbol     | Min  | Max | Unit |
|-------------------------------------|------------|------|-----|------|
| AC input differential voltage       | $V_{DIFF}$ | 0.4  |     | V    |
| AC differential cross point voltage | $V_x$      | 0.68 | 0.9 | V    |

**Table 98 • HSTL Minimum and Maximum AC Switching Speed**

| Parameter         | Symbol    | Max | Unit | Conditions                           |
|-------------------|-----------|-----|------|--------------------------------------|
| Maximum data rate | $D_{MAX}$ | 400 | Mbps | AC loading: per JEDEC specifications |

**Table 99 • HSTL Impedance Specification**

| Parameter                                                         | Symbol    | Typ        | Unit     | Conditions                          |
|-------------------------------------------------------------------|-----------|------------|----------|-------------------------------------|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | $R_{REF}$ | 25.5, 47.8 | $\Omega$ | Reference resistance = 191 $\Omega$ |
| Effective impedance value (ODT for DDRIO I/O bank only)           | $R_{TT}$  | 47.8       | $\Omega$ | Reference resistance = 191 $\Omega$ |

**Table 131 • SSTL15 DC Output Voltage Specification (for DDRIO I/O Bank Only)**

| Parameter                                       | Symbol               | Min                  | Max                  | Unit |
|-------------------------------------------------|----------------------|----------------------|----------------------|------|
| <b>DDR3/SSTL15 Class I (DDR3 Reduced Drive)</b> |                      |                      |                      |      |
| DC output logic high                            | $V_{OH}$             | $0.8 \times V_{DDI}$ |                      | V    |
| DC output logic low                             | $V_{OL}$             |                      | $0.2 \times V_{DDI}$ | V    |
| Output minimum source DC current                | $I_{OH}$ at $V_{OH}$ | 6.5                  |                      | mA   |
| Output minimum sink current                     | $I_{OL}$ at $V_{OL}$ | -6.5                 |                      | mA   |
| <b>DDR3/SSTL15 Class II (DDR3 Full Drive)</b>   |                      |                      |                      |      |
| DC output logic high                            | $V_{OH}$             | $0.8 \times V_{DDI}$ |                      | V    |
| DC output logic low                             | $V_{OL}$             |                      | $0.2 \times V_{DDI}$ | V    |
| Output minimum source DC current                | $I_{OH}$ at $V_{OH}$ | 7.6                  |                      | mA   |
| Output minimum sink current                     | $I_{OL}$ at $V_{OL}$ | -7.6                 |                      | mA   |

**Table 132 • SSTL15 DC Differential Voltage Specification (for DDRIO I/O Bank Only)**

| Parameter                     | Symbol   | Min | Unit |
|-------------------------------|----------|-----|------|
| DC input differential voltage | $V_{ID}$ | 0.2 | V    |

**Note:** To meet JEDEC electrical compliance, use DDR3 full drive transmitter.

**Table 133 • SSTL15 AC SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

| Parameter                           | Symbol          | Min                          | Max                          | Unit |
|-------------------------------------|-----------------|------------------------------|------------------------------|------|
| AC input differential voltage       | $V_{DIFF}$ (AC) | 0.3                          |                              | V    |
| AC differential cross point voltage | $V_x$ (AC)      | $0.5 \times V_{DDI} - 0.150$ | $0.5 \times V_{DDI} + 0.150$ | V    |

**Table 134 • SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

| Parameter         | Symbol    | Max | Unit | Conditions                           |
|-------------------|-----------|-----|------|--------------------------------------|
| Maximum data rate | $D_{MAX}$ | 667 | Mbps | AC loading: per JEDEC specifications |

**Table 135 • SSTL15 AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

| Parameter                                    | Symbol    | Typ                 | Unit     | Conditions                        |
|----------------------------------------------|-----------|---------------------|----------|-----------------------------------|
| Supported output driver calibrated impedance | $R_{REF}$ | 34, 40              | $\Omega$ | Reference resistor = 240 $\Omega$ |
| Effective impedance value (ODT)              | $R_{TT}$  | 20, 30, 40, 60, 120 | $\Omega$ | Reference resistor = 240 $\Omega$ |

**Table 144 • LPDDR AC Differential Voltage Specifications (for DDRIO I/O Bank Only)**

| Parameter                           | Symbol     | Min                  | Max                  | Unit |
|-------------------------------------|------------|----------------------|----------------------|------|
| AC input differential voltage       | $V_{DIFF}$ | $0.6 \times V_{DDI}$ |                      | V    |
| AC differential cross point voltage | $V_x$      | $0.4 \times V_{DDI}$ | $0.6 \times V_{DDI}$ | V    |

**Table 145 • LPDDR AC Specifications (for DDRIO I/O Bank Only)**

| Parameter         | Symbol    | Max | Unit | Conditions                           |
|-------------------|-----------|-----|------|--------------------------------------|
| Maximum data rate | $D_{MAX}$ | 400 | Mbps | AC loading: per JEDEC specifications |

**Table 146 • LPDDR AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

| Parameter                                    | Symbol    | Typ         | Unit     | Conditions                        |
|----------------------------------------------|-----------|-------------|----------|-----------------------------------|
| Supported output driver calibrated impedance | $R_{REF}$ | 20, 42      | $\Omega$ | Reference resistor = 150 $\Omega$ |
| Effective impedance value (ODT)              | $R_{TT}$  | 50, 70, 150 | $\Omega$ | Reference resistor = 150 $\Omega$ |

**Table 147 • LPDDR AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

| Parameter                                                                        | Symbol         | Typ | Unit     |
|----------------------------------------------------------------------------------|----------------|-----|----------|
| Measuring/trip point for data path                                               | $V_{TRIP}$     | 0.9 | V        |
| Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )         | $R_{ENT}$      | 2K  | $\Omega$ |
| Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ ) | $C_{ENT}$      | 5   | pF       |
| Reference resistance for data test path for LPDDR ( $T_{DP}$ )                   | $R_{TT\_TEST}$ | 50  | $\Omega$ |
| Capacitive loading for data path ( $T_{DP}$ )                                    | $C_{LOAD}$     | 5   | $\Omega$ |

**AC Switching Characteristics**

Worst-case commercial conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ , worst-case  $V_{DDI}$ .

**Table 148 • LPDDR Receiver Characteristics for DDRIO I/O Bank with Fixed Codes**

|                          |      | $T_{PY}$ |       | Unit |
|--------------------------|------|----------|-------|------|
| On-Die Termination (ODT) |      | -1       | -Std  |      |
| Pseudo differential      | None | 1.568    | 1.845 | ns   |
| True differential        | None | 1.588    | 1.869 | ns   |

**Table 149 • LPDDR Reduced Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

|              | $T_{DP}$ |       | $T_{ENZL}$ |       | $T_{ENZH}$ |       | $T_{ENHZ}$ |       | $T_{ENLZ}$ |       | Unit |
|--------------|----------|-------|------------|-------|------------|-------|------------|-------|------------|-------|------|
|              | -1       | -Std  | -1         | -Std  | -1         | -Std  | -1         | -Std  | -1         | -Std  |      |
| Single-ended | 2.383    | 2.804 | 2.23       | 2.623 | 2.229      | 2.622 | 2.202      | 2.591 | 2.201      | 2.59  | ns   |
| Differential | 2.396    | 2.819 | 2.764      | 3.252 | 2.764      | 3.252 | 2.255      | 2.653 | 2.255      | 2.653 | ns   |

**Table 221 • Input DDR Propagation Delays (continued)**

| Symbol                  | Description                                         | Measuring Nodes<br>(from, to) | -1    | -Std  | Unit |
|-------------------------|-----------------------------------------------------|-------------------------------|-------|-------|------|
| T <sub>DDRIWAL</sub>    | Asynchronous load minimum pulse width for input DDR | F, F                          | 0.304 | 0.357 | ns   |
| T <sub>DDRICKMPWH</sub> | Clock minimum pulse width high for input DDR        | B, B                          | 0.075 | 0.088 | ns   |
| T <sub>DDRICKMPWL</sub> | Clock minimum pulse width low for input DDR         | B, B                          | 0.159 | 0.187 | ns   |

**Table 239 •  $\mu$ SRAM (RAM128x9) in 128 × 9 Mode (continued)**

| Parameter                                                                             | Symbol         | -1     |       | -Std   |       | Unit |
|---------------------------------------------------------------------------------------|----------------|--------|-------|--------|-------|------|
|                                                                                       |                | Min    | Max   | Min    | Max   |      |
| Read asynchronous reset removal time (pipelined clock)                                | $T_{RSTREM}$   | -0.023 |       | -0.027 |       | ns   |
| Read asynchronous reset removal time (non-pipelined clock)                            |                | 0.046  |       | 0.054  |       | ns   |
| Read asynchronous reset recovery time (pipelined clock)                               | $T_{RSTREC}$   | 0.507  |       | 0.597  |       | ns   |
| Read asynchronous reset recovery time (non-pipelined clock)                           |                | 0.236  |       | 0.278  |       | ns   |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$      |        | 0.835 |        | 0.982 | ns   |
| Read synchronous reset setup time                                                     | $T_{SRSTSU}$   | 0.271  |       | 0.319  |       | ns   |
| Read synchronous reset hold time                                                      | $T_{SRSTHD}$   | 0.061  |       | 0.071  |       | ns   |
| Write clock period                                                                    | $T_{CCY}$      | 4      |       | 4      |       | ns   |
| Write clock minimum pulse width high                                                  | $T_{CCLKMPWH}$ | 1.8    |       | 1.8    |       | ns   |
| Write clock minimum pulse width low                                                   | $T_{CCLKMPWL}$ | 1.8    |       | 1.8    |       | ns   |
| Write block setup time                                                                | $T_{BLKCSU}$   | 0.404  |       | 0.476  |       | ns   |
| Write block hold time                                                                 | $T_{BLKCHD}$   | 0.007  |       | 0.008  |       | ns   |
| Write input data setup time                                                           | $T_{DINCSU}$   | 0.115  |       | 0.135  |       | ns   |
| Write input data hold time                                                            | $T_{DINCHD}$   | 0.15   |       | 0.177  |       | ns   |
| Write address setup time                                                              | $T_{ADDRCSU}$  | 0.088  |       | 0.104  |       | ns   |
| Write address hold time                                                               | $T_{ADDRCHD}$  | 0.128  |       | 0.15   |       | ns   |
| Write enable setup time                                                               | $T_{WECSU}$    | 0.397  |       | 0.467  |       | ns   |
| Write enable hold time                                                                | $T_{WECHD}$    | -0.026 |       | -0.03  |       | ns   |
| Maximum frequency                                                                     | $F_{MAX}$      |        | 250   |        | 250   | MHz  |

The following table lists the  $\mu$ SRAM in 128 × 8 mode in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 240 •  $\mu$ SRAM (RAM128x8) in 128 × 8 Mode**

| Parameter                                    | Symbol          | -1    |       | -Std  |       | Unit |
|----------------------------------------------|-----------------|-------|-------|-------|-------|------|
|                                              |                 | Min   | Max   | Min   | Max   |      |
| Read clock period                            | $T_{CY}$        | 4     |       | 4     |       | ns   |
| Read clock minimum pulse width high          | $T_{CLKMPWH}$   | 1.8   |       | 1.8   |       | ns   |
| Read clock minimum pulse width low           | $T_{CLKMPWL}$   | 1.8   |       | 1.8   |       | ns   |
| Read pipeline clock period                   | $T_{PLCY}$      | 4     |       | 4     |       | ns   |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8   |       | 1.8   |       | ns   |
| Read pipeline clock minimum pulse width low  | $T_{PLCLKMPWL}$ | 1.8   |       | 1.8   |       | ns   |
| Read access time with pipeline register      | $T_{CLK2Q}$     |       | 0.266 |       | 0.313 | ns   |
| Read access time without pipeline register   |                 |       | 1.677 |       | 1.973 | ns   |
| Read address setup time in synchronous mode  | $T_{ADDRSU}$    | 0.301 |       | 0.354 |       | ns   |
| Read address setup time in asynchronous mode |                 | 1.856 |       | 2.184 |       | ns   |

**Table 254 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only) (continued)**

| M2S/M2GL Device | Auto Programming | Auto Update | Programming Recovery | Unit |
|-----------------|------------------|-------------|----------------------|------|
|                 | 100 kHz          | 25 MHz      | 12.5 MHz             |      |
| 150             | 161              | 161         | 161                  | Sec  |

**Table 255 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

| M2S/M2GL Device | Auto Programming | Auto Update   | Programming Recovery | Unit |
|-----------------|------------------|---------------|----------------------|------|
|                 | 100 kHz          | 25 MHz        | 12.5 MHz             |      |
| 005             | 47               | 27            | 28                   | Sec  |
| 010             | 77               | 35            | 35                   | Sec  |
| 025             | 150              | 42            | 41                   | Sec  |
| 050             | 33 <sup>1</sup>  | Not Supported | Not Supported        | Sec  |
| 060             | 291              | 83            | 82                   | Sec  |
| 090             | 427              | 109           | 108                  | Sec  |
| 150             | 708              | 157           | 160                  | Sec  |
| 005             | 41               | 48            | 49                   | Sec  |
| 010             | 86               | 87            | 87                   | Sec  |
| 025             | 87               | 85            | 86                   | Sec  |
| 050             | 85               | Not Supported | Not Supported        | Sec  |
| 060             | 78               | 86            | 86                   | Sec  |
| 090             | 154              | 162           | 162                  | Sec  |
| 150             | 161              | 161           | 161                  | Sec  |
| 005             | 87               | 67            | 66                   | Sec  |
| 010             | 161              | 113           | 113                  | Sec  |
| 025             | 229              | 120           | 121                  | Sec  |
| 050             | 112              | Not Supported | Not Supported        | Sec  |
| 060             | 368              | 161           | 158                  | Sec  |
| 090             | 582              | 261           | 260                  | Sec  |
| 150             | 867              | 309           | 310                  | Sec  |

1. Auto Programming in 050 device is done through SC\_SPI, and SPI CLK is set to 6.25 MHz.

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when  $T_J = 85\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 270 • Math Block with Input Register Used and Output in Bypass Mode**

| Parameter                            | Symbol          | -1     |       | -Std   |       | Unit |
|--------------------------------------|-----------------|--------|-------|--------|-------|------|
|                                      |                 | Min    | Max   | Min    | Max   |      |
| Input register setup time            | $T_{MISU}$      | 0.149  |       | 0.176  |       | ns   |
| Input register hold time             | $T_{MIHD}$      | 0.185  |       | 0.218  |       | ns   |
| Synchronous reset/enable setup time  | $T_{MSRSTENSU}$ | 0.08   |       | 0.094  |       | ns   |
| Synchronous reset/enable hold time   | $T_{MSRSTENHD}$ | -0.012 |       | -0.014 |       | ns   |
| Asynchronous reset removal time      | $T_{MARSTREM}$  | -0.005 |       | -0.005 |       | ns   |
| Asynchronous reset recovery time     | $T_{MARSTREC}$  | 0.088  |       | 0.104  |       | ns   |
| Input register clock to output delay | $T_{MICQ}$      |        | 2.52  |        | 2.964 | ns   |
| CDIN to output delay                 | $T_{MCDIN2Q}$   |        | 1.951 |        | 2.295 | ns   |

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when  $T_J = 85\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 271 • Math Block with Input and Output in Bypass Mode**

| Parameter             | Symbol        | -1    | -Std  | Unit |
|-----------------------|---------------|-------|-------|------|
|                       |               | Max   | Max   |      |
| Input to output delay | $T_{MIQ}$     | 2.568 | 3.022 | ns   |
| CDIN to output delay  | $T_{MCDIN2Q}$ | 1.951 | 2.295 | ns   |

### 2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when  $V_{DD} = 1.14\text{ V}$ ,  $V_{PPNVM} = V_{PP} = 2.375\text{ V}$ .

**Table 272 • eNVM Read Performance**

| Symbol        | Description                 | Operating Temperature Range |      |                  |      |               |      | Unit |
|---------------|-----------------------------|-----------------------------|------|------------------|------|---------------|------|------|
|               |                             | -1                          | -Std | -1               | -Std | -1            | -Std |      |
| $T_J$         | Junction temperature range  | -55 °C to 125 °C            |      | -40 °C to 100 °C |      | 0 °C to 85 °C |      | °C   |
| $F_{MAXREAD}$ | eNVM maximum read frequency | 25                          | 25   | 25               | 25   | 25            | 25   | MHz  |

The following table lists the eNVM page programming in worst-case conditions when  $V_{DD} = 1.14\text{ V}$ ,  $V_{PPNVM} = V_{PP} = 2.375\text{ V}$ .

**Table 273 • eNVM Page Programming**

| Symbol        | Description                | Operating Temperature Range |      |                  |      |               |      | Unit |
|---------------|----------------------------|-----------------------------|------|------------------|------|---------------|------|------|
|               |                            | -1                          | -Std | -1               | -Std | -1            | -Std |      |
| $T_J$         | Junction temperature range | -55 °C to 125 °C            |      | -40 °C to 100 °C |      | 0 °C to 85 °C |      | °C   |
| $T_{PAGEPGM}$ | eNVM page programming time | 40                          | 40   | 40               | 40   | 40            | 40   | ms   |

## 2.3.17 Non-Deterministic Random Bit Generator (NRBG) Characteristics

For more information about NRBG, see [AC407: Using NRBG Services in SmartFusion2 and IGLOO2 Devices Application Note](#). The following table lists the NRBG in worst-case industrial conditions when  $T_J = 100\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 275 • Non-Deterministic Random Bit Generator (NRBG)**

| Service                                   | Timing                                 | Unit | Conditions                |                  |
|-------------------------------------------|----------------------------------------|------|---------------------------|------------------|
|                                           |                                        |      | Prediction Resistance     | Additional Input |
| Instantiate                               | 85                                     | ms   | OFF                       | X                |
| Generate (after Instantiate) <sup>1</sup> | 4.5 ms + (6.25 us/byte x No. of Bytes) |      | OFF                       | 0                |
|                                           | 6.0 ms + (6.25 us/byte x No. of Bytes) |      | OFF                       | 64               |
|                                           | 7.0 ms + (6.25 us/byte x No. of Bytes) |      | OFF                       | 128              |
| Generate (after Instantiate)              | 47                                     | ms   | ON                        | X                |
| Generate (subsequent) <sup>1</sup>        | 0.5 ms + (6.25 us/byte x No. of Bytes) |      | OFF                       | 0                |
|                                           | 2.0 ms + (6.25 us/byte x No. of Bytes) |      | OFF                       | 64               |
|                                           | 3.0 ms + (6.25 us/byte x No. of Bytes) |      | OFF                       | 128              |
| Generate (subsequent)                     | 43                                     | ms   | ON                        | X                |
| Reseed                                    | 40                                     | ms   |                           |                  |
| Uninstantiate                             | 0.16                                   | ms   |                           |                  |
| Reset                                     | 0.10                                   | ms   |                           |                  |
| Self test                                 | 20                                     | ms   | First time after power-up |                  |
|                                           | 6                                      | ms   | Subsequent                |                  |

1. If PUF\_OFF, generate will incur additional PUF delay time for consecutive service calls.

## 2.3.18 Cryptographic Block Characteristics

For more information about cryptographic block and associated services, see [AC410: Using AES System Services in SmartFusion2 and IGLOO2 Devices Application Note](#) and [AC432: Using SHA-256 System Services in SmartFusion2 and IGLOO2 Devices Application Note](#).

The following table lists the cryptographic block characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 276 • Cryptographic Block Characteristics**

| Service                                      | Conditions                              | Timing | Unit |
|----------------------------------------------|-----------------------------------------|--------|------|
| Any service                                  | First certificate check penalty at boot | 11.5   | ms   |
| AES128/256 (encoding-/decoding) <sup>1</sup> | 100 blocks up to 64k blocks             | 700    | kbps |

## 2.3.24 Power-up to Functional Times

The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when  $T_J = 100\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 288 • Power-up to Functional Times for SmartFusion2**

| Symbol           | From             | To                      | Description                                       | Maximum Power-up to Functional Time for SmartFusion2 (uS) |      |      |      |      |      |      |
|------------------|------------------|-------------------------|---------------------------------------------------|-----------------------------------------------------------|------|------|------|------|------|------|
|                  |                  |                         |                                                   | 005                                                       | 010  | 025  | 050  | 060  | 090  | 150  |
| $T_{POR2OUT}$    | POWER_ON_RESET_N | Output available at I/O | Fabric to output                                  | 647                                                       | 500  | 531  | 483  | 474  | 524  | 647  |
| $T_{POR2MSSRST}$ | POWER_ON_RESET_N | MSS_RESE T_N_M2F        | Fabric to MSS                                     | 644                                                       | 497  | 528  | 480  | 468  | 518  | 641  |
| $T_{MSSRST2OUT}$ | MSS_RESET_N_M2F  | Output available at I/O | MSS to output                                     | 3.6                                                       | 3.6  | 3.6  | 3.4  | 4.9  | 4.8  | 4.8  |
| $T_{VDD2OUT}$    | $V_{DD}$         | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 3096                                                      | 2975 | 3012 | 2959 | 2869 | 2992 | 3225 |
| $T_{VDD2POR}$    | $V_{DD}$         | POWER_ON_RESET_N        | $V_{DD}$ at its minimum threshold level to fabric | 2476                                                      | 2487 | 2496 | 2486 | 2406 | 2563 | 2602 |
| $T_{VDD2MSSRST}$ | $V_{DD}$         | MSS_RESE T_N_M2F        | $V_{DD}$ at its minimum threshold level to MSS    | 3093                                                      | 2972 | 3008 | 2956 | 2864 | 2987 | 3220 |
| $T_{VDD2WPU}$    | DEV_RST_N        | DDRIO Inbuf weak pull   | DEV_RST_N to Inbuf weak pull                      | 2500                                                      | 2487 | 2509 | 2475 | 2507 | 2519 | 2617 |
|                  | DEV_RST_N        | MSIO Inbuf weak pull    | DEV_RST_N to Inbuf weak pull                      | 2504                                                      | 2491 | 2510 | 2478 | 2517 | 2525 | 2620 |
|                  | DEV_RST_N        | MSIOD Inbuf weak pull   | DEV_RST_N to Inbuf weak pull                      | 2479                                                      | 2468 | 2493 | 2458 | 2486 | 2499 | 2595 |

**Note:** For more information about power-up times, see [UG0331: SmartFusion2 Microcontroller Subsystem User Guide](#).

**Table 310 • SPI Characteristics for All Devices (continued)**

| Symbol                                                                   | Description                                                                      | Min                         | Typ   | Max | Unit | Conditions                                                                                                         |
|--------------------------------------------------------------------------|----------------------------------------------------------------------------------|-----------------------------|-------|-----|------|--------------------------------------------------------------------------------------------------------------------|
| sp2                                                                      | SPI_[0 1]_CLK minimum pulse width high                                           |                             |       |     |      |                                                                                                                    |
|                                                                          | SPI_[0 1]_CLK = PCLK/2                                                           | 6                           |       |     | ns   |                                                                                                                    |
|                                                                          | SPI_[0 1]_CLK = PCLK/4                                                           | 12.05                       |       |     | ns   |                                                                                                                    |
|                                                                          | SPI_[0 1]_CLK = PCLK/8                                                           | 24.1                        |       |     | ns   |                                                                                                                    |
|                                                                          | SPI_[0 1]_CLK = PCLK/16                                                          | 0.05                        |       |     | µs   |                                                                                                                    |
|                                                                          | SPI_[0 1]_CLK = PCLK/32                                                          | 0.095                       |       |     | µs   |                                                                                                                    |
|                                                                          | SPI_[0 1]_CLK = PCLK/64                                                          | 0.195                       |       |     | µs   |                                                                                                                    |
|                                                                          | SPI_[0 1]_CLK = PCLK/128                                                         | 0.385                       |       |     | µs   |                                                                                                                    |
| sp3                                                                      | SPI_[0 1]_CLK minimum pulse width low                                            |                             |       |     |      |                                                                                                                    |
|                                                                          | SPI_[0 1]_CLK = PCLK/2                                                           | 6                           |       |     | ns   |                                                                                                                    |
|                                                                          | SPI_[0 1]_CLK = PCLK/4                                                           | 12.05                       |       |     | ns   |                                                                                                                    |
|                                                                          | SPI_[0 1]_CLK = PCLK/8                                                           | 24.1                        |       |     | ns   |                                                                                                                    |
|                                                                          | SPI_[0 1]_CLK = PCLK/16                                                          | 0.05                        |       |     | µs   |                                                                                                                    |
|                                                                          | SPI_[0 1]_CLK = PCLK/32                                                          | 0.095                       |       |     | µs   |                                                                                                                    |
|                                                                          | SPI_[0 1]_CLK = PCLK/64                                                          | 0.195                       |       |     | µs   |                                                                                                                    |
|                                                                          | SPI_[0 1]_CLK = PCLK/128                                                         | 0.385                       |       |     | µs   |                                                                                                                    |
| sp4                                                                      | SPI_[0 1]_CLK,<br>SPI_[0 1]_DO, SPI_[0 1]_SS<br>rise time (10%–90%) <sup>1</sup> |                             | 2.77  |     | ns   | I/O Configuration:<br>LVCMOS 2.5 V -<br>8 mA<br>AC loading: 35 pF<br>test conditions:<br>Typical voltage,<br>25 °C |
| sp5                                                                      | SPI_[0 1]_CLK,<br>SPI_[0 1]_DO, SPI_[0 1]_SS<br>fall time (10%–90%) <sup>1</sup> |                             | 2.906 |     | ns   | I/O Configuration:<br>LVCMOS 2.5 V -<br>8 mA<br>AC loading: 35 pF<br>test conditions:<br>Typical voltage,<br>25 °C |
| SPI master configuration (applicable for 005, 010, 025, and 050 devices) |                                                                                  |                             |       |     |      |                                                                                                                    |
| sp6m                                                                     | SPI_[0 1]_DO setup time <sup>2</sup>                                             | (SPI_x_CLK_period/2) – 8.0  |       |     | ns   |                                                                                                                    |
| sp7m                                                                     | SPI_[0 1]_DO hold time <sup>2</sup>                                              | (SPI_x_CLK_period/2) – 2.5  |       |     | ns   |                                                                                                                    |
| sp8m                                                                     | SPI_[0 1]_DI setup time <sup>2</sup>                                             | 12                          |       |     | ns   |                                                                                                                    |
| sp9m                                                                     | SPI_[0 1]_DI hold time <sup>2</sup>                                              | 2.5                         |       |     | ns   |                                                                                                                    |
| SPI slave configuration (applicable for 005, 010, 025, and 050 devices)  |                                                                                  |                             |       |     |      |                                                                                                                    |
| sp6s                                                                     | SPI_[0 1]_DO setup time <sup>2</sup>                                             | (SPI_x_CLK_period/2) – 17.0 |       |     | ns   |                                                                                                                    |
| sp7s                                                                     | SPI_[0 1]_DO hold time <sup>2</sup>                                              | (SPI_x_CLK_period/2) + 3.0  |       |     | ns   |                                                                                                                    |
| sp8s                                                                     | SPI_[0 1]_DI setup time <sup>2</sup>                                             | 2                           |       |     | ns   |                                                                                                                    |
| sp9s                                                                     | SPI_[0 1]_DI hold time <sup>2</sup>                                              | 7                           |       |     | ns   |                                                                                                                    |