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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	56520
Total RAM Bits	1869824
Number of I/O	207
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-LFBGA
Supplier Device Package	400-VFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl060ts-1vfg400

Table 214	LVPECL Recommended DC Operating Conditions	64
Table 215	LVPECL Receiver Characteristics for MSIO I/O Bank	65
Table 216	LVPECL DC Input Voltage Specification	65
Table 217	LVPECL DC Differential Voltage Specification	65
Table 218	LVPECL Minimum and Maximum AC Switching Speeds	65
Table 219	Input Data Register Propagation Delays	67
Table 220	Output/Enable Data Register Propagation Delays	69
Table 221	Input DDR Propagation Delays	71
Table 222	Output DDR Propagation Delays	74
Table 223	Combinatorial Cell Propagation Delays	76
Table 224	Register Delays	77
Table 225	150 Device Global Resource	78
Table 226	090 Device Global Resource	78
Table 227	050 Device Global Resource	78
Table 228	025 Device Global Resource	78
Table 229	010 Device Global Resource	79
Table 230	005 Device Global Resource	79
Table 231	RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18	79
Table 232	RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9	80
Table 233	RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4	81
Table 234	RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2	83
Table 235	RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1	84
Table 236	RAM1K18 – Two-Port Mode for Depth × Width Configuration 512 × 36	85
Table 237	μSRAM (RAM64x18) in 64 × 18 Mode	86
Table 238	μSRAM (RAM64x16) in 64 × 16 Mode	87
Table 239	μSRAM (RAM128x9) in 128 × 9 Mode	88
Table 240	μSRAM (RAM128x8) in 128 × 8 Mode	89
Table 241	μSRAM (RAM256x4) in 256 × 4 Mode	91
Table 242	μSRAM (RAM512x2) in 512 × 2 Mode	92
Table 243	μSRAM (RAM1024x1) in 1024 × 1 Mode	93
Table 244	JTAG Programming (Fabric Only)	94
Table 245	JTAG Programming (eNVM Only)	95
Table 246	JTAG Programming (Fabric and eNVM)	95
Table 247	2 Step IAP Programming (Fabric Only)	95
Table 248	2 Step IAP Programming (eNVM Only)	96
Table 249	2 Step IAP Programming (Fabric and eNVM)	96
Table 250	SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)	96
Table 251	SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)	96
Table 252	SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)	97
Table 253	Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)	97
Table 254	Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)	97
Table 255	Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)	98
Table 256	JTAG Programming (Fabric Only)	99
Table 257	JTAG Programming (eNVM Only)	99
Table 258	JTAG Programming (Fabric and eNVM)	99
Table 259	2 Step IAP Programming (Fabric Only)	100
Table 260	2 Step IAP Programming (eNVM Only)	100
Table 261	2 Step IAP Programming (Fabric and eNVM)	100
Table 262	SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)	101
Table 263	SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)	101
Table 264	SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)	101
Table 265	Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)	102
Table 266	Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)	102
Table 267	Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)	102
Table 268	Math Blocks with all Registers Used	103
Table 269	Math Block with Input Bypassed and Output Registers Used	103
Table 270	Math Block with Input Register Used and Output in Bypass Mode	104
Table 271	Math Block with Input and Output in Bypass Mode	104
Table 272	eNVM Read Performance	104

1.9 Revision 3.0

In revision 3.0 of this document, the Theta B/C columns and FCS325 package was updated. For more information, see Table 9, page 10 (SAR 62002).

1.10 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Table 1, page 4 was updated (SAR 59056).
- Table 7, page 8 temperature and data retention information was updated SAR (61363).
- Storage Operating Table was updated and split into three tables – Table 5, page 7, Table 7, page 8 (SAR 58725).
- Updated Theta B/C columns and FCS325 package in Table 9, page 10 (SAR 62002).
- Added 090-FCS325 thermal resistance to Table 9, page 10 (SAR 59384).
- TQ144 package was added to Table 9, page 10 (SAR 57708).
- Added PLL jitter data for the VF400 package (SAR 53162).
- Added Additional Worst Case IDD to Table 11, page 12 and Table 12, page 13 (SAR 59077).
- Table 13, page 13, Table 14, page 13, and Table 15, page 14 were added to verify Inrush currents (SAR 56348).
- Table 18, page 19 and Table 21, page 20 – I/O speeds were replaced.
- Max speed was changed in Table 41, page 26 (SAR 57221) and in Table 52, page 29 (SAR 57113).
- Minimum and Maximum DC/AC Input and Output Levels Specification, page 29 and Table 49, page 29–Table 57, page 31 were added.
- Added Cload to Table 89, page 39 (SAR 56238).
- Removed "Rs" information in DDR Timing Measurement Table 123, page 47, Table 133, page 49, and Table 144, page 52.
- Updated drive programming for M/B-LVDS outputs (SAR 58154).
- Added an inverter bubble to DDR_IN latch in Figure 10, page 70 (SAR 61418).
- QF waveform in Figure 11, page 71 was updated (SAR 59816).
- uSRAM Write Clock minimum values were updated in Table 237, page 86–Table 243, page 93 (SAR 55236).
- Fixed typo in the 32 kHz Crystal (XTAL) oscillator accuracy data section (SAR 59669).
- The "On-Chip Oscillator" section was split, and the Embedded NVM (eNVM) Characteristics, page 104 was added. Table 277, page 107–Table 281, page 109 were revised.(SARs 57898 and 59669).
- PLL VCP Frequency and conditions were added to Table 282, page 110 (SAR 57416).
- Fixed typo for PLL jitter data in the 100-400 MHz range (SAR 60727).
- Updated FCCC information in Table 282, page 110 and Table 283, page 111 (SAR 60799).
- Device 025 specifications were added to Table 283, page 111 (SAR 51625).
- JTAG Table 284, page 112 was replaced (SAR 51188).
- Flash*Freeze Table 293, page 119 was replaced (SAR 57828).
- Added support for HCSL I/O Standard for SERDES reference clocks in Table 300, page 123 and Table 301, page 123 (SAR 50748).
- Tir and Tif parameters were added to Table 303, page 124 (SAR 52203).
- Speed grade consistency was fixed in tables throughout the datasheet (SAR 50722).
- Added jitter attenuation information (SAR 59405).

1.11 Revision 1.0

The following is a summary of the changes in revision 1.0 of this document.

- The IGLOO2 v2 and the SmartFusion2 v5 datasheets are combined into this single product family datasheet.

2.3.5.5 Detailed I/O Characteristics

Table 24 • Input Capacitance, Leakage Current, and Ramp Time

Symbol	Description	Maximum	Unit	Conditions
C_{IN}	Input capacitance	10	pF	
I_{IL} (dc)	Input current low (Applicable to HSTL/SSTL inputs only)	400	μA	$V_{DDI} = 2.5 V$
		500	μA	$V_{DDI} = 1.8 V$
		600	μA	$V_{DDI} = 1.5 V^1$
	Input current low (Applicable to all other digital inputs)	10	μA	
I_{IH} (dc)	Input current high (Applicable to HSTL/SSTL inputs only)	400	μA	$V_{DDI} = 2.5 V$
		500	μA	$V_{DDI} = 1.8 V$
		600	μA	$V_{DDI} = 1.5 V^1$
	Input current high (Applicable to all other digital inputs)	10	μA	
T_{RAMPIN}^2	Input ramp time (Applicable to all digital inputs)	50	ns	

1. Applicable when I/O pair is programmed with an HSTL/SSTL I/O type on IOP and an un-terminated I/O type (LVCMOS, for example) on ION pad.
2. Voltage ramp must be monotonic.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of DDRIO I/O bank at V_{OH}/V_{OL} Level.

Table 25 • I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank

V_{DDI} Domain	R(WEAK PULL-UP) at V_{OH} (Ω)		R(WEAK PULL-DOWN) at V_{OL} (Ω)	
	Min	Max	Min	Max
2.5 V ^{1, 2}	10K	17.8K	9.98K	18K
1.8 V ^{1, 2}	10.3K	19.1K	10.3K	19.5K
1.5 V ^{1, 2}	10.6K	20.2K	10.6K	21.1K
1.2 V ^{1, 2}	11.1K	22.7K	11.2K	24.6K

1. $R(\text{WEAK PULL-DOWN}) = (V_{OLspec})/I(\text{WEAK PULL-DOWN MAX})$.
2. $R(\text{WEAK PULL-UP}) = (V_{DDImax} - V_{OHspec})/I(\text{WEAK PULL-UP MIN})$.

Table 77 • LVCMOS 1.2 V AC Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CAL	75, 60, 50, 40	Ω

Table 78 • LVCMOS 1.2 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point	V_{TRIP}	0.6	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 79 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

Output Drive Selection			V_{OH} (V)	V_{OL} (V)	IOH (at V_{OH}) mA	IOL (at V_{OL}) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	2	2
4 mA	4 mA	4 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	4	4
		6 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	6	6

Note: For a detailed I/V curve, use the corresponding IBIS models:
www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.14\text{ V}$

Table 80 • LVCMOS 1.2 V Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	2.448	2.88	2.466	2.901	ns

Table 81 • LVCMOS 1.2 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On-Die Termination ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	4.714	5.545	4.675	5.5	ns
50	6.668	7.845	6.579	7.74	ns
75	5.832	6.862	5.76	6.777	ns
150	5.162	6.073	5.111	6.014	ns

Table 85 • LVCMOS 1.2 V Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.883	4.568	4.868	5.726	5.329	6.269	7.994	9.404	7.527	8.855	ns
4 mA	Slow	3.774	4.44	4.188	4.926	4.613	5.426	8.972	10.555	8.315	9.782	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

2.3.5.11 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

Minimum and Maximum DC/AC Input and Output Levels Specification (Applicable to MSIO Bank Only)

Table 86 • PCI/PCI-X DC Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

Table 87 • PCI/PCI-X DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	3.45	V
Input current high ¹	$I_{IH}(DC)$			
Input current low ¹	$I_{IL}(DC)$			

1. See Table 24, page 22.

Table 88 • PCI/PCI-X DC Output Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}		Per PCI specification		V
DC output logic low	V_{OL}		Per PCI specification		V

Table 89 • PCI/PCI-X Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (MSIO I/O bank)	D_{MAX}	630	Mbps	AC Loading: per JEDEC specifications

Table 90 • PCI/PCI-X AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path (falling edge)	V_{TRIP}	$0.615 \times V_{DDI}$	V
Measuring/trip point for data path (rising edge)	V_{TRIP}	$0.285 \times V_{DDI}$	V
Resistance for data test path	R_{TT_TEST}	25	Ω
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	10	pF

Table 131 • SSTL15 DC Output Voltage Specification (for DDRIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DDR3/SSTL15 Class I (DDR3 Reduced Drive)				
DC output logic high	V_{OH}	$0.8 \times V_{DDI}$		V
DC output logic low	V_{OL}		$0.2 \times V_{DDI}$	V
Output minimum source DC current	I_{OH} at V_{OH}	6.5		mA
Output minimum sink current	I_{OL} at V_{OL}	-6.5		mA
DDR3/SSTL15 Class II (DDR3 Full Drive)				
DC output logic high	V_{OH}	$0.8 \times V_{DDI}$		V
DC output logic low	V_{OL}		$0.2 \times V_{DDI}$	V
Output minimum source DC current	I_{OH} at V_{OH}	7.6		mA
Output minimum sink current	I_{OL} at V_{OL}	-7.6		mA

Table 132 • SSTL15 DC Differential Voltage Specification (for DDRIO I/O Bank Only)

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID}	0.2	V

Note: To meet JEDEC electrical compliance, use DDR3 full drive transmitter.

Table 133 • SSTL15 AC SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF} (AC)	0.3		V
AC differential cross point voltage	V_x (AC)	$0.5 \times V_{DDI} - 0.150$	$0.5 \times V_{DDI} + 0.150$	V

Table 134 • SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	667	Mbps	AC loading: per JEDEC specifications

Table 135 • SSTL15 AC Calibrated Impedance Option (for DDRIO I/O Bank Only)

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	R_{REF}	34, 40	Ω	Reference resistor = 240 Ω
Effective impedance value (ODT)	R_{TT}	20, 30, 40, 60, 120	Ω	Reference resistor = 240 Ω

2.3.7.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 173 • B-LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V

Table 174 • B-LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	2.925	V
Input current high ¹	I_{IH} (DC)			
Input current low ¹	I_{IL} (DC)			

1. See Table 24, page 22.

Table 175 • B-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 176 • B-LVDS DC Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	V_{OD}	65	460	mV
Output common mode voltage (for MSIO I/O bank only)	V_{OCM}	1.1	1.5	V
Input common mode voltage	V_{ICM}	0.05	2.4	V
Input differential voltage	V_{ID}	0.1	V_{DDI}	V

Table 177 • B-LVDS Minimum and Maximum AC Switching Speed

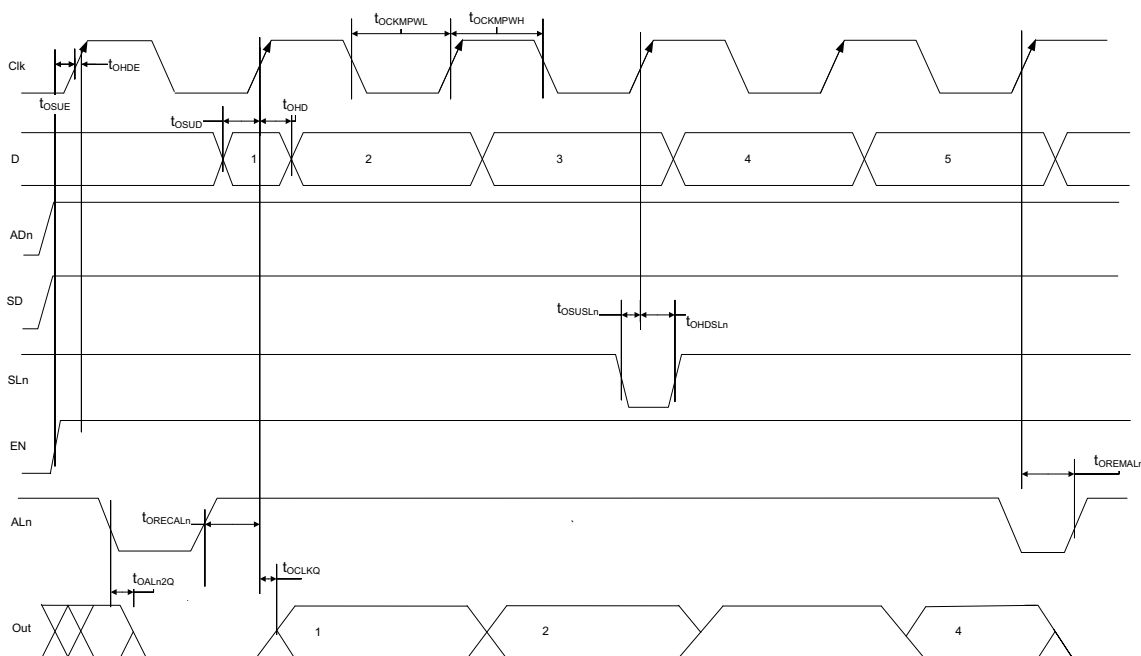
Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	500	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 178 • B-LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	27	Ω

Table 179 • B-LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

Figure 9 • I/O Register Output Timing Diagram

The following table lists the output/enable propagation delays in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 220 • Output/Enable Data Register Propagation Delays

Parameter	Symbol	Measuring Nodes (from, to) ¹	-1	-Std	Unit
Bypass delay of the output/enable register	T_{OBYP}	F, G or H, I	0.353	0.415	ns
Clock-to-Q of the output/enable register	T_{OCLKQ}	E, G or E, I	0.263	0.309	ns
Data setup time for the output/enable register	T_{OSUD}	A, E or J, E	0.19	0.223	ns
Data hold time for the output/enable register	T_{OHD}	A, E or J, E	0	0	ns
Enable setup time for the output/enable register	T_{OSUE}	B, E	0.419	0.493	ns
Enable hold time for the output/enable register	T_{OHE}	B, E	0	0	ns
Synchronous load setup time for the output/enable register	T_{OSUSL}	D, E	0.196	0.231	ns
Synchronous load hold time for the output/enable register	T_{OHSL}	D, E	0	0	ns
Asynchronous clear-to-q of the output/enable register ($ADn = 1$)	T_{OALN2Q}	C, G or C, I	0.505	0.594	ns
Asynchronous preset-to-q of the output/enable register ($ADn = 0$)		C, G or C, I	0.528	0.621	ns
Asynchronous load removal time for the output/enable register	$T_{OREMALN}$	C, E	0	0	ns
Asynchronous load recovery time for the output/enable register	$T_{ORECALN}$	C, E	0.034	0.04	ns
Asynchronous load minimum pulse width for the output/enable register	T_{OWALN}	C, C	0.304	0.357	ns
Clock minimum pulse width high for the output/enable register	$T_{OCKMPWH}$	E, E	0.075	0.088	ns
Clock minimum pulse width low for the output/enable register	$T_{OCKMPWL}$	E, E	0.159	0.187	ns

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

2.3.9 DDR Module Specification

This section describes input and output DDR module and timing specifications.

2.3.9.1 Input DDR Module

Figure 10 • Input DDR Module

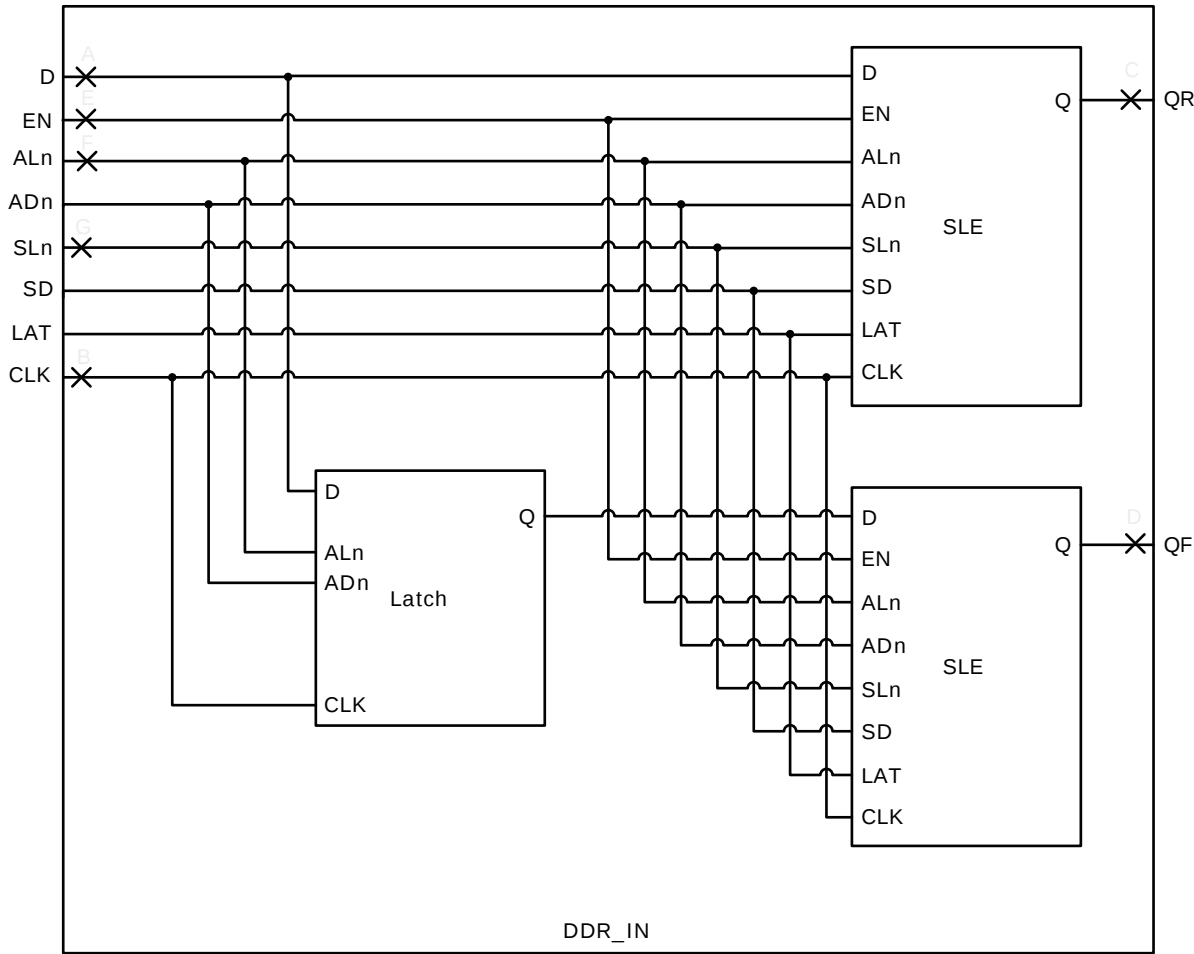
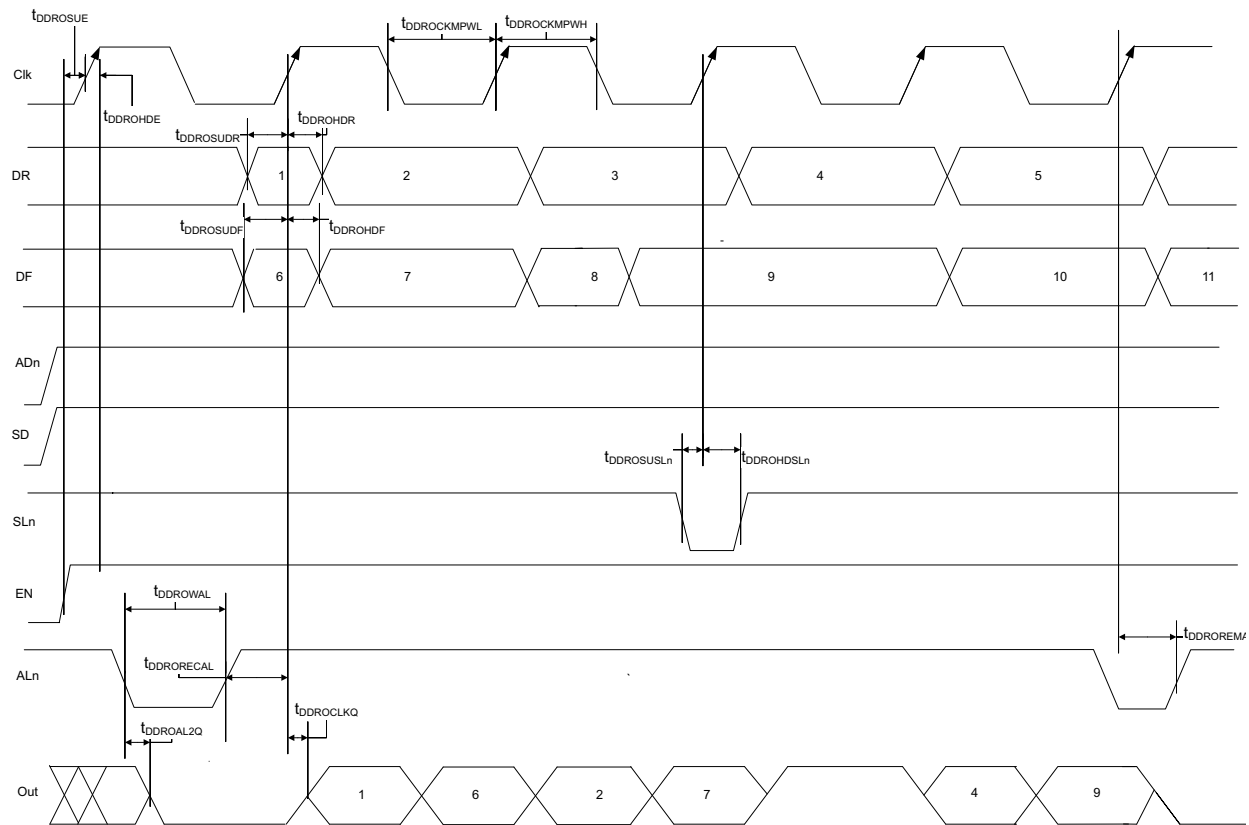


Figure 13 • Output DDR Timing Diagram**2.3.9.5 Timing Characteristics**

The following table lists the output DDR propagation delays in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 222 • Output DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDROCLKQ}$	Clock-to-out of DDR for output DDR	E, G	0.263	0.309	ns
$T_{DDROSUDF}$	Data_F data setup for output DDR	F, E	0.143	0.168	ns
$T_{DDROSUDR}$	Data_R data setup for output DDR	A, E	0.19	0.223	ns
$T_{DDROHDF}$	Data_F data hold for output DDR	F, E	0	0	ns
$T_{DDROHDF}$	Data_R data hold for output DDR	A, E	0	0	ns
$T_{DDROSUE}$	Enable setup for input DDR	B, E	0.419	0.493	ns
T_{DDROHE}	Enable hold for input DDR	B, E	0	0	ns
$T_{DDROSUSLn}$	Synchronous load setup for input DDR	D, E	0.196	0.231	ns
$T_{DDROHSLN}$	Synchronous load hold for input DDR	D, E	0	0	ns
$T_{DDROAL2Q}$	Asynchronous load-to-out for output DDR	C, G	0.528	0.621	ns
$T_{DDROREML}$	Asynchronous load removal time for output DDR	C, E	0	0	ns
$T_{DDRORECAL}$	Asynchronous load recovery time for output DDR	C, E	0.034	0.04	ns

2.3.11 Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for the positions of various global routing resources.

The following table lists the 150 device global resources in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 225 • 150 Device Global Resource

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.83	0.911	0.831	0.913	ns
Input high delay for global clock	T_{RCKH}	1.457	1.588	1.715	1.869	ns
Maximum skew for global clock	T_{RCKSW}		0.131		0.154	ns

The following table lists the 090 device global resources in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 226 • 090 Device Global Resource

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.835	0.888	0.833	0.886	ns
Input high delay for global clock	T_{RCKH}	1.405	1.489	1.654	1.752	ns
Maximum skew for global clock	T_{RCKSW}		0.084		0.098	ns

The following table lists the 050 device global resources in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 227 • 050 Device Global Resource

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.827	0.897	0.826	0.896	ns
Input high delay for global clock	T_{RCKH}	1.419	1.53	1.671	1.8	ns
Maximum skew for global clock	T_{RCKSW}		0.111		0.129	ns

The following table lists the 025 device global resources in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 228 • 025 Device Global Resource

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.747	0.799	0.745	0.797	ns
Input high delay for global clock	T_{RCKH}	1.294	1.378	1.522	1.621	ns
Maximum skew for global clock	T_{RCKSW}		0.084		0.099	ns

Table 231 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18 (continued)

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Block select hold time	$T_{BLKH D}$	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		1.529		1.799	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	$T_{RDES U}$	0.449		0.528		ns
Read enable hold time	$T_{RDEH D}$	0.167		0.197		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLES U}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEH D}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}	–	1.506	–	1.772	ns
Asynchronous reset removal time	$T_{RSTRE M}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTRE C}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTRE M}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTRE C}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTS U}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTH D}$	0.036		0.043		ns
Write enable setup time	$T_{WES U}$	0.39		0.458		ns
Write enable hold time	$T_{WEH D}$	0.242		0.285		ns
Maximum frequency	F_{MAX}		400		340	MHz

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 2K × 9 in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 232 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register			0.334		0.393	ns
Read access time without pipeline register	T_{CLK2Q}		2.273		2.674	ns
Access time with feed-through write timing			1.529		1.799	ns

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 16K × 1 in worst commercial-case conditions when $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 235 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register			0.32		0.377	ns
Read access time without pipeline register	T_{CLK2Q}		2.269		2.669	ns
Access time with feed-through write timing			1.51		1.777	ns
Address setup time	T_{ADDRSU}	0.626		0.737		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.322		0.378		ns
Data hold time	T_{DHD}	0.082		0.096		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		1.51		1.777	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.53		0.624		ns
Read enable hold time	T_{RDEHD}	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}		1.547		1.82	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.454		0.534		ns
Write enable hold time	T_{WEHD}	0.048		0.057		ns
Maximum frequency	F_{MAX}		400		340	MHz

The following table lists the RAM1K18 – two-port mode for depth × width configuration 512 × 36 in worst commercial-case conditions when $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 236 • RAM1K18 – Two-Port Mode for Depth × Width Configuration 512 × 36

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register	T_{CLK2Q}		0.334		0.393	ns
Read access time without pipeline register			2.25		2.647	ns
Address setup time	T_{ADDRSU}	0.313		0.368		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.337		0.396		ns
Data hold time	T_{DHD}	0.111		0.13		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.201		0.237		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.25		2.647	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.449		0.528		ns
Read enable hold time	T_{RDEHD}	0.167		0.197		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}		1.506		1.772	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.39		0.458		ns
Write enable hold time	T_{WEHD}	0.242		0.285		ns
Maximum frequency	F_{MAX}		400		340	MHz

Table 237 • μ SRAM (RAM64x18) in 64 × 18 Mode (continued)

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 64 × 16 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 238 • μ SRAM (RAM64x16) in 64 × 16 Mode

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		–0.778		–0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.983	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns

Table 238 • μ SRAM (RAM64x16) in 64 × 16 Mode (continued)

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 128 × 9 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 239 • μ SRAM (RAM128x9) in 128 × 9 Mode

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		–0.778		–0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns

The following table lists the μ SRAM in 256×4 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 241 • μ SRAM (RAM256x4) in 256×4 Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.27		0.31	ns
Read access time without pipeline register			1.75		2.06	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.931		2.272		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.121		0.142		ns
Read address hold time in asynchronous mode		-0.65		-0.76		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	-0.65		-0.77		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.09		2.46	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	-0.02		-0.03		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.83		0.98	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.101		0.118		ns
Write input data hold time	T_{DINCHD}	0.137		0.161		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns

Table 276 • Cryptographic Block Characteristics (continued)

Service	Conditions	Timing	Unit
SHA256	512 bits	540	kbps
	1024 bits	780	kbps
	2048 bits	950	kbps
	24 kbits	1140	kbps
HMAC	512 bytes	820	kbps
	1024 bytes	890	kbps
	2048 bytes	930	kbps
	24 kbytes	980	kbps
KeyTree		1.8	ms
Challenge-response	PUF = OFF	25	ms
	PUF = ON	7	ms
ECC point multiplication		590	ms
ECC point addition		8	ms

1. Using cypher block chaining (CBC) mode.

2.3.19 Crystal Oscillator

The following table describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

Table 277 • Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		20		MHz	
Accuracy	ACCXTAL			0.0047	%	005, 010, 025, 050, 060, and 090 devices
				0.0058	%	150 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		200	300	ps	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		200	300	ps	010, 025, 050, and 060 devices
			250	410	ps	150 devices
			250	550	ps	005 and 090 devices
Operating current	IDYNXTAL		1.5		mA	010, 050, and 060 devices
			1.65		mA	005, 025, 090, and 150 devices
Input logic level high	VIHXTAL	0.9 V _{PP}			V	
Input logic level low	VILXTAL			0.1 V _{PP}	V	

The following table lists the receiver pa in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 297 • Receiver Parameters

Symbol	Description	Min	Typ	Max	Unit
VRX-IN-PP-CC	Differential input peak-to-peak sensitivity (2.5 Gbps)	0.238		1.2	V
	Differential input peak-to-peak sensitivity (2.5 Gbps, de-emphasized)	0.219		1.2	V
	Differential input peak-to-peak sensitivity (5.0 Gbps)	0.300		1.2	V
	Differential input peak-to-peak sensitivity (5.0 Gbps, de-emphasized)	0.300		1.2	V
VRX-CM-AC-P	Input common mode range (AC coupled)			150	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset			15	μs
RLRX-DIFF	Return loss differential mode (2.5 Gbps)	-10			dB
	Return loss differential mode (5.0 Gbps)				
	0.05 GHz to 1.25 GHz	-10			dB
	1.25 GHz to 2.5 GHz	-8			dB
RLRX-CM	Return loss common mode (2.5 Gbps, 5.0 Gbps)	-6			dB
RX-CID ¹	CID limit PCIe Gen1/2			200	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65		175	mV

1. AC-coupled, BER = e^{-12} , using synchronous clock.

Table 298 • SerDes Protocol Compliance

Protocol	Maximum Data Rate (Gbps)	-1	-Std
PCIe Gen 1	2.5	Yes	Yes
PCIe Gen 2	5.0	Yes	
XAUI	3.125	Yes	
Generic EPCS	3.2	Yes	
Generic EPCS	2.5	Yes	Yes

2.3.31.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, see Figure 22, page 128.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Table 305 • SPI Characteristics for All Devices

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPIFMAX	Maximum operating frequency of SPI interface			20	MHz	
sp1	SPI_[0 1]_CLK minimum period					
	SPI_[0 1]_CLK = PCLK/2	12			ns	
	SPI_[0 1]_CLK = PCLK/4	24.1			ns	
	SPI_[0 1]_CLK = PCLK/8	48.2			ns	
	SPI_[0 1]_CLK = PCLK/16	0.1			μs	
	SPI_[0 1]_CLK = PCLK/32	0.19			μs	
	SPI_[0 1]_CLK = PCLK/64	0.39			μs	
	SPI_[0 1]_CLK = PCLK/128	0.77			μs	
sp2	SPI_[0 1]_CLK minimum pulse width high					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			μs	
	SPI_[0 1]_CLK = PCLK/32	0.095			μs	
	SPI_[0 1]_CLK = PCLK/64	0.195			μs	
	SPI_[0 1]_CLK = PCLK/128	0.385			μs	
sp3	SPI_[0 1]_CLK minimum pulse width low					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			μs	
	SPI_[0 1]_CLK = PCLK/32	0.095			μs	
	SPI_[0 1]_CLK = PCLK/64	0.195			μs	
	SPI_[0 1]_CLK = PCLK/128	0.385			μs	
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) ¹		2.77		ns	I/O Configuration: LVCMOS 2.5 V– 8 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C