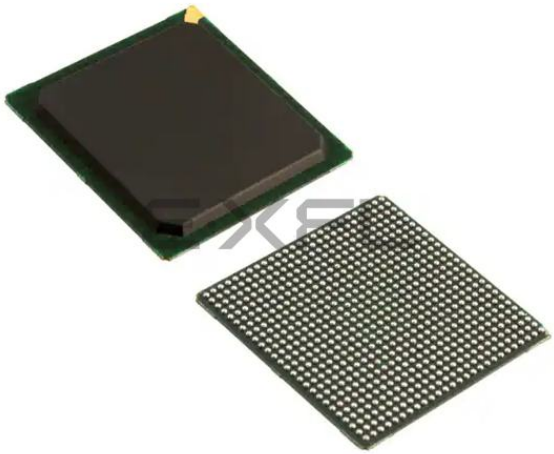

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	86316
Total RAM Bits	2648064
Number of I/O	425
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl090t-1fg676

1.9 Revision 3.0

In revision 3.0 of this document, the Theta B/C columns and FCS325 package was updated. For more information, see Table 9, page 10 (SAR 62002).

1.10 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Table 1, page 4 was updated (SAR 59056).
- Table 7, page 8 temperature and data retention information was updated SAR (61363).
- Storage Operating Table was updated and split into three tables – Table 5, page 7, Table 7, page 8 (SAR 58725).
- Updated Theta B/C columns and FCS325 package in Table 9, page 10 (SAR 62002).
- Added 090-FCS325 thermal resistance to Table 9, page 10 (SAR 59384).
- TQ144 package was added to Table 9, page 10 (SAR 57708).
- Added PLL jitter data for the VF400 package (SAR 53162).
- Added Additional Worst Case IDD to Table 11, page 12 and Table 12, page 13 (SAR 59077).
- Table 13, page 13, Table 14, page 13, and Table 15, page 14 were added to verify Inrush currents (SAR 56348).
- Table 18, page 19 and Table 21, page 20 – I/O speeds were replaced.
- Max speed was changed in Table 41, page 26 (SAR 57221) and in Table 52, page 29 (SAR 57113).
- Minimum and Maximum DC/AC Input and Output Levels Specification, page 29 and Table 49, page 29–Table 57, page 31 were added.
- Added Cload to Table 89, page 39 (SAR 56238).
- Removed "Rs" information in DDR Timing Measurement Table 123, page 47, Table 133, page 49, and Table 144, page 52.
- Updated drive programming for M/B-LVDS outputs (SAR 58154).
- Added an inverter bubble to DDR_IN latch in Figure 10, page 70 (SAR 61418).
- QF waveform in Figure 11, page 71 was updated (SAR 59816).
- uSRAM Write Clock minimum values were updated in Table 237, page 86–Table 243, page 93 (SAR 55236).
- Fixed typo in the 32 kHz Crystal (XTAL) oscillator accuracy data section (SAR 59669).
- The "On-Chip Oscillator" section was split, and the Embedded NVM (eNVM) Characteristics, page 104 was added. Table 277, page 107–Table 281, page 109 were revised.(SARs 57898 and 59669).
- PLL VCP Frequency and conditions were added to Table 282, page 110 (SAR 57416).
- Fixed typo for PLL jitter data in the 100-400 MHz range (SAR 60727).
- Updated FCCC information in Table 282, page 110 and Table 283, page 111 (SAR 60799).
- Device 025 specifications were added to Table 283, page 111 (SAR 51625).
- JTAG Table 284, page 112 was replaced (SAR 51188).
- Flash*Freeze Table 293, page 119 was replaced (SAR 57828).
- Added support for HCSL I/O Standard for SERDES reference clocks in Table 300, page 123 and Table 301, page 123 (SAR 50748).
- Tir and Tif parameters were added to Table 303, page 124 (SAR 52203).
- Speed grade consistency was fixed in tables throughout the datasheet (SAR 50722).
- Added jitter attenuation information (SAR 59405).

1.11 Revision 1.0

The following is a summary of the changes in revision 1.0 of this document.

- The IGLOO2 v2 and the SmartFusion2 v5 datasheets are combined into this single product family datasheet.

The following table lists the embedded operating flash limits.

Table 6 • **Embedded Operating Flash Limits**

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Commercial	Embedded flash	Min T_J = 0 °C Max T_J = 85 °C	Min T_J = 0 °C Max T_J = 85 °C	< 1000 cycles per page, up to two million cycles per eNVM array	20 years
			Min T_J = 0 °C Max T_J = 85 °C	< 10000 cycles per page, up to 20 million cycles per eNVM array	10 years
Industrial	Embedded flash	Min T_J = –40 °C Max T_J = 100 °C	Min T_J = –40 °C Max T_J = 100 °C	< 1000 cycles per page, up to two million cycles per eNVM array	20 years
			Min T_J = –40 °C Max T_J = 100 °C	< 10000 cycles per page, up to 20 million cycles per eNVM array	10 years

Note: If your product qualification requires accelerated programming cycles, see *Microsemi SoC Products Quality and Reliability Report* about recommended methodologies.

Table 7 • **Device Storage Temperature and Retention**

Product Grade	Storage Temperature (Tstg)	Retention
Commercial	Min T_J = 0 °C Max T_J = 85 °C	20 years
Industrial	Min T_J = –40 °C Max T_J = 100 °C	20 years

Table 8 • **High Temperature Data Retention (HTR) Lifetime**

T_J (C)	HTR Lifetime[1] (yrs)
90	20.5
95	20.5
100	20.5
105	17.0
110	15.0
115	13.0
120	11.5
125	10.0
130	8.0
135	6.0
140	4.5
145	3.0
150	1.5

1. HTR Lifetime is the period during which a verify failure is not expected due to flash leakage.

Table 9 • **Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices *(continued)***

Device	Still Air θ_{JA}	1.0 m/s θ_{JA}	2.5 m/s θ_{JA}	θ_{JB}	θ_{JC}	Unit
150						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W
FCS536	15.01	12.06	10.76	3.69	1.55	°C/W
FCV484	16.21	13.11	11.84	6.73	0.10	°C/W

2.3.1.2.1 Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in the actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package with another.

The maximum power dissipation allowed is calculated using EQ4.

$$\text{Maximum power allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100 °C. EQ5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where:

θ_{JA} = 14.7 °C/W (taken from Table 9, page 10).

T_A = 85 °C

$$\text{Maximum power allowed} = \frac{100\ °C - 85\ °C}{14.7\ °C/W} = 1.088\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink may be attached to the top of the case, or the airflow inside the system must be increased.

2.3.1.2.2 Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from the junction to the board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

2.3.1.2.3 Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable to packages used with external heat sinks. Constant temperature is applied to the surface, which acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

2.3.1.3 ESD Performance

See *RT0001: Microsemi Corporation - SoC Products Reliability Report* for information about ESD.

2.3.5.5 Detailed I/O Characteristics

Table 24 • **Input Capacitance, Leakage Current, and Ramp Time**

Symbol	Description	Maximum	Unit	Conditions
C_{IN}	Input capacitance	10	pF	
I_{IL} (dc)	Input current low (Applicable to HSTL/SSTL inputs only)	400	µA	V_{DDI} = 2.5 V
		500	µA	V_{DDI} = 1.8 V
		600	µA	V_{DDI} = 1.5 V[1]
	Input current low (Applicable to all other digital inputs)	10	µA	
I_{IH} (dc)	Input current high (Applicable to HSTL/SSTL inputs only)	400	µA	V_{DDI} = 2.5 V
		500	µA	V_{DDI} = 1.8 V
		600	µA	V_{DDI} = 1.5 V[1]
	Input current high (Applicable to all other digital inputs)	10	µA	
T_{RAMPIN}[2]	Input ramp time (Applicable to all digital inputs)	50	ns	

1. Applicable when I/O pair is programmed with an HSTL/SSTL I/O type on IOP and an un-terminated I/O type (LVCMOS, for example) on ION pad.
2. Voltage ramp must be monotonic.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of DDRIO I/O bank at V_{OH}/V_{OL} Level.

Table 25 • **I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank**

	R(WEAK PULL-UP) at V_{OH} (Ω)		R(WEAK PULL-DOWN) at V_{OL} (Ω)	
V_{DDI} Domain	**Min**	**Max**	**Min**	**Max**
2.5 V[1, 2]	10K	17.8K	9.98K	18K
1.8 V[1, 2]	10.3K	19.1K	10.3K	19.5K
1.5 V[1, 2]	10.6K	20.2K	10.6K	21.1K
1.2 V[1, 2]	11.1K	22.7K	11.2K	24.6K

1. R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX).
2. R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN).

Table 34 • **LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.4	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 35 • **LVTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank**

Output Drive Selection	V_{OH} (V)	V_{OL} (V)	IOH (at V_{OH}) mA	IOL (at V_{OL}) mA
2 mA	V_{DDI} – 0.4	0.4	2	2
4 mA	V_{DDI} – 0.4	0.4	4	4
8 mA	V_{DDI} – 0.4	0.4	8	8
12 mA	V_{DDI} – 0.4	0.4	12	12
16 mA	V_{DDI} – 0.4	0.4	16	16
20 mA	V_{DDI} – 0.4	0.4	20	20

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 3.0 V

Table 36 • **LVTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	–1	–Std	–1	–Std	
None	2.262	2.663	2.289	2.695	ns

Table 37 • **LVTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		Unit
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	
2 mA	Slow	3.192	3.755	3.47	4.083	2.969	3.494	1.856	2.183	3.337	3.926	ns
4 mA	Slow	2.331	2.742	2.673	3.145	2.526	2.973	3.034	3.569	4.451	5.236	ns
8 mA	Slow	2.135	2.511	2.33	2.741	2.297	2.703	4.532	5.331	4.825	5.676	ns
12 mA	Slow	2.052	2.414	2.107	2.479	2.162	2.544	5.75	6.764	5.445	6.406	ns
16 mA	Slow	2.062	2.425	2.072	2.438	2.145	2.525	5.993	7.05	5.625	6.618	ns
20 mA	Slow	2.148	2.527	1.999	2.353	2.088	2.458	6.262	7.367	5.876	6.913	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

2.3.5.7 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs that are in compliance with the JEDEC specification JESD8-5A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 38 • **LVCMOS 2.5 V DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V

Table 39 • **LVCMOS 2.5 V DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	V_{IH} (DC)	1.7	2.625	V
DC input logic high (for MSIO I/O bank)	V_{IH} (DC)	1.7	3.45	V
DC input logic low	V_{IL} (DC)	–0.3	0.7	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

1. See Table 24, page 22.

Table 40 • **LVCMOS 2.5 V DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}[1]	V_{DDI} – 0.4	–	V
DC output logic low	V_{OL}[2]		0.4	V

1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

Table 41 • **LVCMOS 2.5 V AC Minimum and Maximum Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	400	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D_{MAX}	410	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	420	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 42 • **LVCMOS 2.5 V AC Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	Rodt_cal	75, 60, 50, 33, 25, 20	Ω

Table 53 • **LVCMOS 1.8 V AC Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	Rodt_cal	75, 60, 50, 33, 25, 20	Ω

Table 54 • **LVCMOS 1.8 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.9	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2k	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 55 • **LVCMOS 1.8 V Transmitter Drive Strength Specifications**

Output Drive Selection			V_{OH} (V)	V_{OL} (V)	IOH (at V_{OH})	IOL (at V_{OL})
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max	mA	mA
2 mA	2 mA	2 mA	V_{DDI} – 0.45	0.45	2	2
4 mA	4 mA	4 mA	V_{DDI} – 0.45	0.45	4	4
6 mA	6 mA	6 mA	V_{DDI} – 0.45	0.45	6	6
8 mA	8 mA	8 mA	V_{DDI} – 0.45	0.45	8	8
10 mA	10 mA	10 mA	V_{DDI} – 0.45	0.45	10	10
12 mA		12 mA	V_{DDI} – 0.45	0.45	12	12
		16 mA[1]	V_{DDI} – 0.45	0.45	16	16

1. 16 mA drive strengths, all slews, meets LPDDR JEDEC electrical compliance.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 1.71 V

Table 56 • **LVCMOS 1.8 V Receiver Characteristics (Input Buffers)**

	On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
		–1	–Std	–1	–Std	
LVCMOS 1.8 V (for DDRIO I/O bank with Fixed Codes)	None	1.968	2.315	2.099	2.47	ns
LVCMOS 1.8 V (for MSIO I/O bank)	None	2.898	3.411	2.883	3.393	ns
	50	3.05	3.59	3.044	3.583	ns
	75	2.999	3.53	2.987	3.516	ns
	150	2.947	3.469	2.933	3.452	ns
LVCMOS 1.8 V (for MSIOD I/O bank)	None	2.611	3.071	2.598	3.057	ns
	50	2.775	3.264	2.775	3.265	ns
	75	2.72	3.2	2.712	3.19	ns
	150	2.666	3.137	2.655	3.123	ns

Table 95 • **HSTL DC Output Voltage Specification Applicable to DDRIO I/O Bank Only**

Parameter	Symbol	Min	Max	Unit
	HSTL Class I			
DC output logic high	V_{OH}	V_{DDI} – 0.4		V
DC output logic low	V_{OL}		0.4	V
Output minimum source DC current (MSIO and DDRIO I/O banks)	I_{OH} at V_{OH}	–8.0		mA
Output minimum sink current (MSIO and DDRIO I/O banks)	I_{OL} at V_{OL}	8.0		mA
	HSTL Class II			
DC output logic high	V_{OH}	V_{DDI} – 0.4		V
DC output logic low	V_{OL}		0.4	V
Output minimum source DC current	I_{OH} at V_{OH}	–16.0		mA
Output minimum sink current	I_{OL} at V_{OL}	16.0		mA

Table 96 • **HSTL DC Differential Voltage Specification**

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID} (DC)	0.2	V

Table 97 • **HSTL AC Differential Voltage Specifications**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF}	0.4		V
AC differential cross point voltage	V_x	0.68	0.9	V

Table 98 • **HSTL Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	400	Mbps	AC loading: per JEDEC specifications

Table 99 • **HSTL Impedance Specification**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	R_{REF}	25.5, 47.8	Ω	Reference resistance = 191 Ω
Effective impedance value (ODT for DDRIO I/O bank only)	R_{TT}	47.8	Ω	Reference resistance = 191 Ω

2.3.6.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 139 • **LPDDR DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max
Supply voltage	V_{DDI}	1.71	1.8	1.89
Termination voltage	V_{TT}	0.838	0.900	0.964
Input reference voltage	V_{REF}	0.838	0.900	0.964

Table 140 • **LPDDR DC Input Voltage Specification**

Parameter	Symbol	Min	Max
DC input logic high	V_{IH} (DC)	0.7 × V_{DDI}	1.89
DC input logic low	V_{IL} (DC)	–0.3	0.3 × V_{DDI}
Input current high[1]	I_{IH} (DC)		
Input current low[1]	I_{IL} (DC)		

1. See Table 24, page 22.

Table 141 • **LPDDR DC Output Voltage Specification Reduced Drive**

Parameter	Symbol	Min	Max
DC output logic high	V_{OH}	0.9 × V_{DDI}	
DC output logic low	V_{OL}		0.1 × V_{DDI}
Output minimum source DC current	I_{OH} at V_{OH}	0.1	
Output minimum sink current	I_{OL} at V_{OL}	–0.1	

Table 142 • **LPDDR DC Output Voltage Specification Full Drive[1]**

Parameter	Symbol	Min	Max
DC output logic high	V_{OH}	0.9 × V_{DDI}	
DC output logic low	V_{OL}		0.1 × V_{DDI}
Output minimum source DC current	I_{OH} at V_{OH}	0.1	
Output minimum sink current	I_{OL} at V_{OL}	–0.1	

1. To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.

Table 143 • **LPDDR DC Differential Voltage Specification**

Parameter	Symbol	Min
DC input differential voltage	V_{ID} (DC)	0.4 × V_{DDI}

Table 150 • **LPDDR Full Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

	T_{DP}		T_{ENZL}		T_{ENZH}		T_{ENHZ}		T_{ENLZ}		
	–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.171	2.555	2.17	2.554	ns
Differential	2.298	2.703	2.288	2.692	2.288	2.692	2.593	3.051	2.593	3.051	ns

Minimum and Maximum DC/AC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode

Table 151 • **LPDDR-LVCMOS 1.8 V Mode Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.710	1.8	1.89	V

Table 152 • **LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	V_{IH} (DC)	0.65 × V_{DDI}	1.89	V
DC input logic high (for MSIO I/O bank)	V_{IH} (DC)	0.65 × V_{DDI}	3.45	V
DC input logic low	V_{IL} (DC)	–0.3	0.35 × V_{DDI}	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

1. See Table 24, page 22.

Table 153 • **LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	V_{DDI} – 0.45		V
DC output logic low	V_{OL}		0.45	V

Table 154 • **LPDDR-LVCMOS 1.8 V Minimum and Maximum AC Switching Speeds**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	400	Mbps	AC loading: 17pf load, 8 ma drive and above/all slew

Table 155 • **LPDDR-LVCMOS 1.8 V Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CAL	75, 60, 50, 33, 25, 20	Ω

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V.

Table 210 • **RSDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.855	3.359	ns
100	2.85	3.353	ns

Table 211 • **RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.602	3.061	ns
100	2.597	3.055	ns

Table 212 • **RSDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
2.097	2.467	2.303	2.709	2.291	2.695	1.961	2.307	1.947	2.29	ns

Table 213 • **RSDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
	–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
No pre-emphasis	1.614	1.899	1.559	1.834	1.55	1.823	1.59	1.87	1.575	1.852	ns
Min pre-emphasis	1.604	1.887	1.742	2.05	1.728	2.032	1.889	2.222	1.858	2.185	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

2.3.7.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

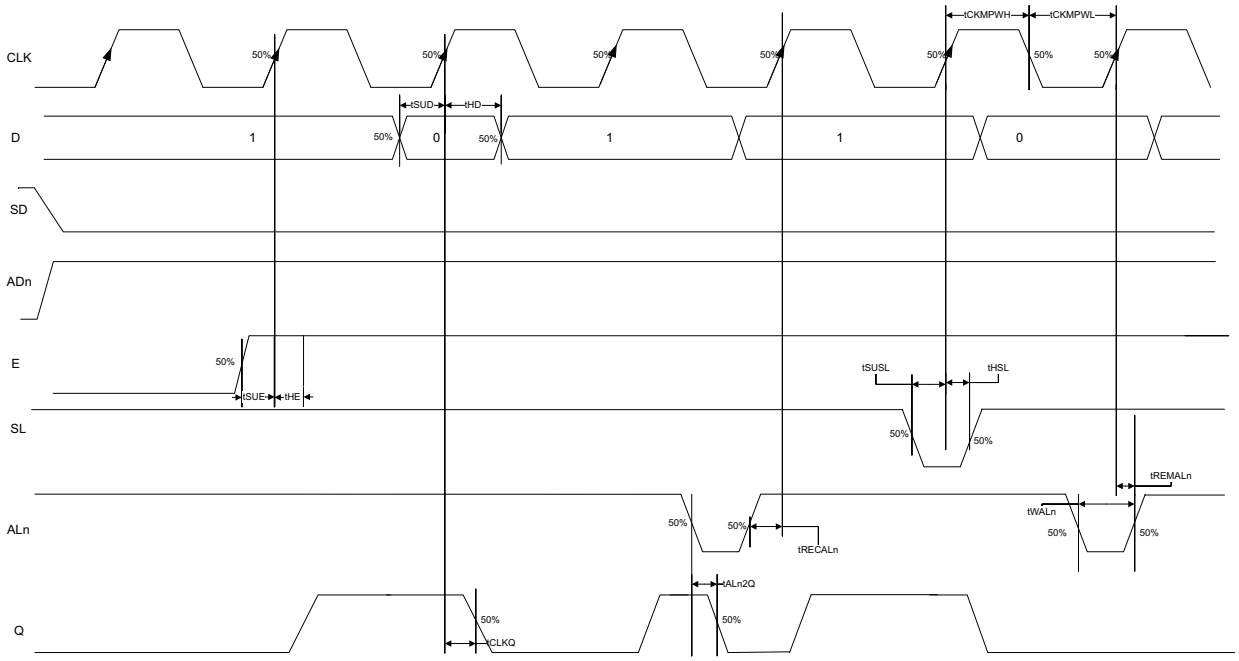
Minimum and Maximum Input and Output Levels (Applicable to MSIO I/O Bank Only)

Table 214 • **LVPECL Recommended DC Operating Conditions**

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

The following figure shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

Figure 16 • **Sequential Module Timing Diagram**



2.3.10.3.1 Timing Characteristics

The following table lists the register delays in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 224 • **Register Delays**

Parameter	Symbol	–1	–Std	Unit
Clock-to-Q of the core register	T_{CLKQ}	0.108	0.127	ns
Data setup time for the core register	T_{SUD}	0.254	0.298	ns
Data hold time for the core register	T_{HD}	0	0	ns
Enable setup time for the core register	T_{SUE}	0.335	0.394	ns
Enable hold time for the core register	T_{HE}	0	0	ns
Synchronous load setup time for the core register	T_{SUSL}	0.335	0.394	ns
Synchronous load hold time for the core register	T_{HSL}	0	0	ns
Asynchronous Clear-to-Q of the core register (ADn = 1)	T_{ALN2Q}	0.473	0.556	ns
Asynchronous preset-to-Q of the core register (ADn = 0)		0.451	0.531	ns
Asynchronous load removal time for the core register	T_{REMALN}	0	0	ns
Asynchronous load recovery time for the core register	T_{RECALN}	0.353	0.415	ns
Asynchronous load minimum pulse width for the core register	T_{WALN}	0.266	0.313	ns
Clock minimum pulse width high for the core register	T_{CKMPWH}	0.065	0.077	ns
Clock minimum pulse width low for the core register	T_{CKMPWL}	0.139	0.164	ns

Table 251 • **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only) *(continued)***

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
150	544496	10	158	15	Sec

Table 252 • **SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	9	61	11	Sec
010	842688	15	107	21	Sec
025	1497408	26	121	35	Sec
050	2695168	43	141	55	Sec
060	2686464	48	143	60	Sec
090	4190208	75	244	91	Sec
150	6682768	117	296	141	Sec

Table 253 • **Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)**

M2S/M2GL Device	Auto Programming 100 kHz	Auto Update 25 MHz	Programming Recovery 12.5 MHz	Unit
005	47	27	28	Sec
010	77	35	35	Sec
025	150	42	41	Sec
050	33[1]	Not Supported	Not Supported	Sec
060	291	83	82	Sec
090	427	109	108	Sec
150	708	157	160	Sec

1. Auto Programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

Table 254 • **Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)**

M2S/M2GL Device	Auto Programming 100 kHz	Auto Update 25 MHz	Programming Recovery 12.5 MHz	Unit
005	41	48	49	Sec
010	86	87	87	Sec
025	87	85	86	Sec
050	85	Not Supported	Not Supported	Sec
060	78	86	86	Sec
090	154	162	162	Sec

2.3.16 SRAM PUF

For more details on static random-access memory (SRAM) physical unclonable functions (PUF) services, see *AC434: Using SRAM PUF System Service in SmartFusion2 Application Note*.

The following table lists the SRAM PUF in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 274 • **SRAM PUF**

	PUF Off		PUF On		
Service	**Typ**	**Max**	**Typ**	**Max**	**Unit**
Create activation code	709.1	746.4	754.4	762.5	ms
Delete activation code	1329.3	1399.3	1414.1	1429.3	ms
Create intrinsic keycode	656.6	691.1	698.5	706.0	ms
Create extrinsic keycode	656.6	691.1	698.5	706.0	ms
Get number of keys	1.3	1.4	1.4	1.4	ms
Export (Kc0, Kc1)	998.0	1050.5	1061.7	1073.1	ms
Export 2 keycodes	2020.2	2126.5	2149.2	2172.3	ms
Export 4 keycodes	3065.7	3227.0	3261.3	3296.4	ms
Export 8 keycodes	5101.0	5369.5	5426.6	5485.0	ms
Export 16 keycodes	9212.1	9697.0	9800.1	9905.5	ms
Import (Kc0, Kc1)	39.7	41.8	42.2	42.7	ms
Import 2 keycodes	50.1	52.7	53.3	53.9	ms
Import 4 keycodes	60.6	63.8	64.5	65.2	ms
Import 8 keycodes	80.9	85.1	86.1	87.0	ms
Import 16 keycodes	123.8	130.4	131.7	133.2	ms
Delete keycode	552.5	581.6	587.8	594.1	ms
Fetch key	31.4	33.0	33.4	33.7	ms
Fetch ecc key	20.0	21.1	21.3	21.5	ms
Get seed	2.0	2.1	2.2	2.2	ms

2.3.20 On-Chip Oscillator

The following tables describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

Table 280 • **Electrical Characteristics of the 50 MHz RC Oscillator**

Parameter	Symbol	Typ	Max	Unit	Condition
Operating frequency	F50RC	50		MHz	
Accuracy	ACC50RC	1	4	%	050 devices
		1	5	%	005, 025, and 060 devices
		1	6.3	%	090 devices
		1	7.1	%	010 and 150 devices
Output duty cycle	CYC50RC	49–51	46.5–53.5	%	
Output jitter (peak to peak)	JIT50RC				Period Jitter
		200	300	ps	005, 010, 050, and 060 devices
		200	400	ps	150 devices
		300	500	ps	025 and 090 devices
					Cycle-to-Cycle Jitter
		200	300	ps	005 and 050 devices
		320	420	ps	010, 060, and 150 devices
		320	850	ps	025 and 090 devices
Operating current	IDYN50RC	6.5		mA	

Table 281 • **Electrical Characteristics of the 1 MHz RC Oscillator**

Parameter	Symbol	Typ	Max	Unit	Condition
Operating frequency	F1RC	1		MHz	
Accuracy	ACC1RC	1	3	%	005, 010, 025, and 050 devices
		1	4.5	%	060, and 150 devices
		1	5.6	%	090 devices
Output duty cycle	CYC1RC	49–51	46.5–53.5	%	005, 010, 025, 050, 090 and 150 devices
		49-51	46.0-54.0	%	060 devices
Output jitter (peak to peak)	JIT1RC				Period Jitter
		10	20	ns	005, 010, 025, and 050 devices
		10	28	ns	060, 090 and 150 devices
					Cycle-to-Cycle Jitter
		10	20	ns	005, 010, and 050 devices
		10	35	ns	025, 060, and 150 devices
		10	45	ns	090 devices
Operating current	IDYN1RC	0.1		mA	
Startup time	SU1RC		17	µs	050, 090, and 150 devices
			18	µs	005, 010, and 025 devices

1. The minimum output clock frequency is limited by the PLL. For more information, see *UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide*.
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance is limited by the CCC output frequency.

The following table lists the CCC/PLL jitter specifications in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 283 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications**

CCC Output Maximum Peak-to-Peak Period Jitter F_{OUT_CCC}						
Parameter	**Conditions/Package Combinations**					**Unit**
10 FG484, 050 FG896/FG484/FCS325 Packages[1]	SSO = 0	0 < SSO <= 2	SSO <= 4	SSO <= 8	SSO <= 16	
20 MHz to 100 MHz	Max(110, ± 1% x ($1/F_{OUT\_CCC}$))	Max(150, ± 1% x ($1/F_{OUT\_CCC}$))				ps
100 MHz to 400 MHz	Max(120, ± 1% x ($1/F_{OUT\_CCC}$))	Max(150, ± 1% x ($1/F_{OUT\_CCC}$))			Max(170, ± 1% x ($1/F_{OUT\_CCC}$))	ps
025 FG484/FCS325 Package[1]	0 < SSO <=16					
20 MHz to 74 MHz	± 1% x ($1/F_{OUT\_CCC}$))					ps
74 MHz to 400 MHz	210					ps
005 FG484 Package[1]	0 < SSO <=16					
20 MHz to 53 MHz	± 1% x ($1/F_{OUT\_CCC}$))					ps
53 MHz to 400 MHz	270					ps
090 FG676 and FC325 Package[1]	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x ($1/F_{OUT\_CCC}$))					ps
100 MHz to 400 MHz	150					ps
060 FG676 Package[1]	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x ($1/F_{OUT\_CCC}$)					ps
100 MHz to 400 MHz	150					
150 FC1152 Package[1]	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x ($1/F_{OUT\_CCC}$))					ps
100 MHz to 400 MHz	120					ps

1. SSO data is based on LVCMOS 2.5 V MSIO and/or MSIOD bank I/Os.

2.3.22 JTAG

Table 284 • **JTAG 1532 for 005, 010, 025, and 050 Devices**

		005		010		025		050		Unit
Parameter	**Symbol**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	
Clock to Q (data out)	T_{TCK2Q}	7.47	8.79	7.73	9.09	7.75	9.12	7.89	9.28	ns
Reset to Q (data out)	T_{RSTB2Q}	7.65	9	6.43	7.56	6.13	7.21	7.40	8.70	ns
Test data input setup time	T_{DISU}	–1.05	–0.89	–0.69	–0.59	–0.67	–0.57	–0.30	–0.25	ns
Test data input hold time	T_{DIHD}	2.38	2.8	2.38	2.8	2.42	2.85	2.09	2.45	ns
Test mode select setup time	T_{TMSSU}	–0.73	–0.62	–1.03	–1.21	–1.1	–0.94	0.28	0.33	ns
Test mode select hold time	T_{TMDHD}	1.36	1.6	1.43	1.68	1.93	2.27	0.16	0.19	ns
ResetB removal time	$T_{TRSTREM}$	–0.77	–0.65	–1.08	–0.92	–1.33	–1.13	–0.45	–0.38	ns
ResetB recovery time	$T_{TRSTREC}$	–0.76	–0.65	–1.07	–0.91	–1.34	–1.14	–0.45	–0.38	ns
TCK maximum frequency	F_{TCKMAX}	25	21.25	25	21.25	25	21.25	25.00	21.25	MHz

Table 285 • **JTAG 1532 for 060, 090, and 150 Devices**

		060		090		150		
Parameter	**Symbol**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
Clock to Q (data out)	T_{TCK2Q}	8.38	9.86	8.96	10.54	8.66	10.19	ns
Reset to Q (data out)	T_{RSTB2Q}	8.54	10.04	7.75	9.12	8.79	10.34	ns
Test data input setup time	T_{DISU}	–1.18	–1	–1.31	–1.11	–0.96	–0.82	ns
Test data input hold time	T_{DIHD}	2.52	2.97	2.68	3.15	2.57	3.02	ns
Test mode select setup time	T_{TMSSU}	–0.97	–0.83	–1.02	–0.87	–0.53	–0.45	ns
Test mode select hold time	T_{TMDHD}	1.7	2	1.67	1.96	1.02	1.2	ns
ResetB removal time	$T_{TRSTREM}$	–1.21	–1.03	–0.76	–0.65	–1.03	–0.88	ns
ResetB recovery time	$T_{TRSTREC}$	–1.21	–1.03	–0.77	–0.65	–1.03	–0.88	ns
TCK maximum frequency	F_{TCKMAX}	25	21.25	25	21.25	25	21.25	MHz

2.3.23 System Controller SPI Characteristics

2.3.31.2 SmartFusion2 Inter-Integrated Circuit (I^2C) Characteristics

This section describes the DC and switching of the I^2C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, see Figure 21, page 125.

The following table lists the I^2C characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V

Table 303 • **I2C Characteristics**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input low voltage	V_{IL}	–0.3		0.8	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive.
Input high voltage	V_{IH}	2		3.45	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive.
Hysteresis of schmitt triggered inputs for V_{DDI} > 2 V	V_{HYS}	0.05 × V_{DDI}			V	See Table 28, page 23 for more information.
Input current high	I_{IL}			10	µA	See Single-Ended I/O Standards, page 24 for more information.
Input current low	I_{IH}			10	µA	See Single-Ended I/O Standards, page 24 for more information.
Input rise time	T_{ir}			1000	ns	Standard mode
				300	ns	Fast mode
Input fall time	T_{if}			300	ns	Standard mode
				300	ns	Fast mode
Maximum output voltage low (open drain) at 3 mA sink current for V_{DDI} > 2 V	V_{OL}			0.4	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive.
Pin capacitance	Cin			10	pF	V_{IN} = 0, f = 1.0 MHz
Output fall time from VIHMin to VILMax[1]	t_{OF}[1]		21.04		ns	V_{IHmin} to V_{ILMax}, CLOAD = 400 pF
			5.556		ns	V_{IHmin} to V_{ILMax}, CLOAD = 100 pF
Output rise time from VILMax to VIHMin[1]	t_{OR} [1]		19.887		ns	V_{ILMax} to V_{IHmin}, CLOAD = 400 pF
			5.218		ns	V_{ILMax} to V_{IHmin}, CLOAD = 100 pF
Output buffer maximum pull-down resistance[2, 3]	$R_{pull\text{-}up}$[2,3]			50	Ω	
Output buffer maximum pull-up resistance[2, 4]	$R_{pull\text{-}down}$[2,4]			131.25	Ω	

Table 305 • **SPI Characteristics for All Devices *(continued)***

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp5	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS fall time (10%–90%)[1]		2.906		ns	IO Configuration: LVCMOS 2.5 V-8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0|1]_DI setup time[2]	12			ns	
sp9m	SPI_[0|1]_DI hold time[2]	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0|1]_DI setup time[2]	2			ns	
sp9s	SPI_[0|1]_DI hold time[2]	7			ns	
SPI master configuration (applicable for 060, 090, and 150 devices)						
sp6m	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 7.0			ns	
sp7m	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) – 9.5			ns	
sp8m	SPI_[0|1]_DI setup time[2]	15			ns	
sp9m	SPI_[0|1]_DI hold time[2]	–2.5			ns	
SPI slave configuration (applicable for 060, 090, and 150 devices)						
sp6s	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 16.0			ns	
sp7s	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) - 3.5			ns	
sp8s	SPI_[0|1]_DI setup time[2]	3			ns	
sp9s	SPI_[0|1]_DI hold time[2]	2.5			ns	

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. For allowable pclk configurations, see Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.