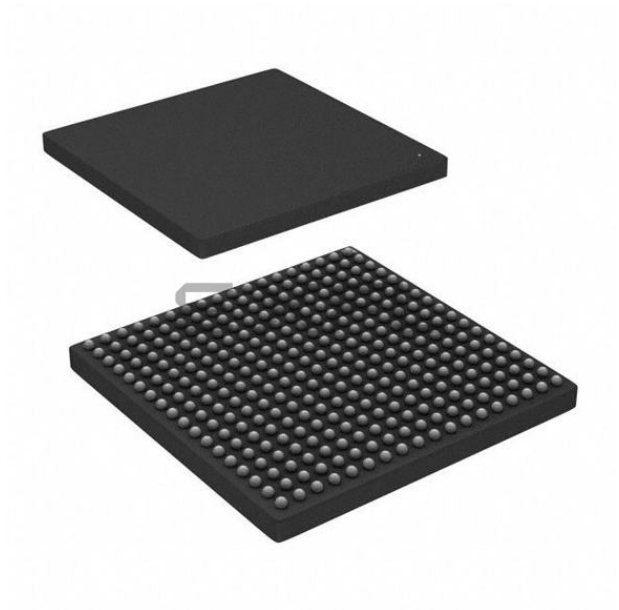

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	86184
Total RAM Bits	2648064
Number of I/O	180
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	325-TFBGA, FCBGA
Supplier Device Package	325-FCBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl090t-fcsg325i

Figure 1 • **High Temperature Data Retention (HTR)**

2.3.1.1 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to –1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to V_{CCI} + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

Note: The above specifications do not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant with the PCI standard including the PCI overshoot/undershoot specifications.

2.3.1.2 Thermal Characteristics

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ1 through EQ3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

Table 11 • **SmartFusion2 and IGLOO2 Quiescent Supply Current (V_{DD} = 1.2 V) – Typical Process**

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC2	Flash*Freeze	1.4	2.6	3.7	5.1	5.0	5.1	8.9	mA	Typical (T_J = 25 °C)
		12.0	20.0	26.6	35.3	35.4	35.7	57.8	mA	Commercial (T_J = 85 °C)
		18.5	30.8	41.0	54.5	54.5	55.0	89.0	mA	Industrial (T_J = 100 °C)

Table 12 • **SmartFusion2 and IGLOO2 Quiescent Supply Current (V_{DD} = 1.26 V) – Worst-Case Process**

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC1	Non-Flash*Freeze	43.8	57.0	84.6	132.3	161.4	163.0	242.5	mA	Commercial (T_J= 85 °C)
		65.3	85.7	127.8	200.9	245.4	247.8	369.0	mA	Industrial (T_J = 100 °C)
IDC2	Flash*Freeze	29.1	45.6	51.7	62.7	69.3	70.0	84.8	mA	Commercial (T_J = 85 °C)
		44.9	70.3	79.7	96.5	106.8	107.8	130.6	mA	Industrial (T_J = 100 °C)

2.3.2.2 Programming Currents

The following tables represent programming, verify and Inrush currents for SmartFusion2 SoC and IGLOO2 FPGA devices.

Table 13 • **Currents During Program Cycle, 0 °C < = T_J <= 85 °C – Typical Process**

Power Supplies	Voltage (V)	005	010	025	050	060	090	150[1]	Unit
V_{DD}	1.26	46	53	55	58	30	42	52	mA
V_{PP}	3.46	8	11	6	10	9	12	12	mA
V_{PPNVM}	3.46	1	2	2	3	3	3		mA
V_{DDI}	2.62	31	16	17	1	12	12	81	mA
	3.46	62	31	36	1	12	17	84	mA
Number of banks		7	8	8	10	10	9	19	

1. V_{PP} and V_{PPNVM} are internally shorted.

Table 14 • **Currents During Verify Cycle, 0 °C <= T_J <= 85 °C – Typical Process**

Power Supplies	Voltage (V)	005	010	025	050	060	090	150[1]	Unit
V_{DD}	1.26	44	53	55	58	33	41	51	mA
V_{PP}	3.46	6	5	3	15	8	11	12	mA
V_{PPNVM}	3.46	1	0	0	1	1	1		mA
V_{DDI}	2.62	31	16	17	1	12	11	81	mA
	3.46	61	32	36	1	12	17	84	mA
Number of banks		7	8	8	10	10	9	19	

1. V_{PP} and V_{PPNVM} are internally shorted.

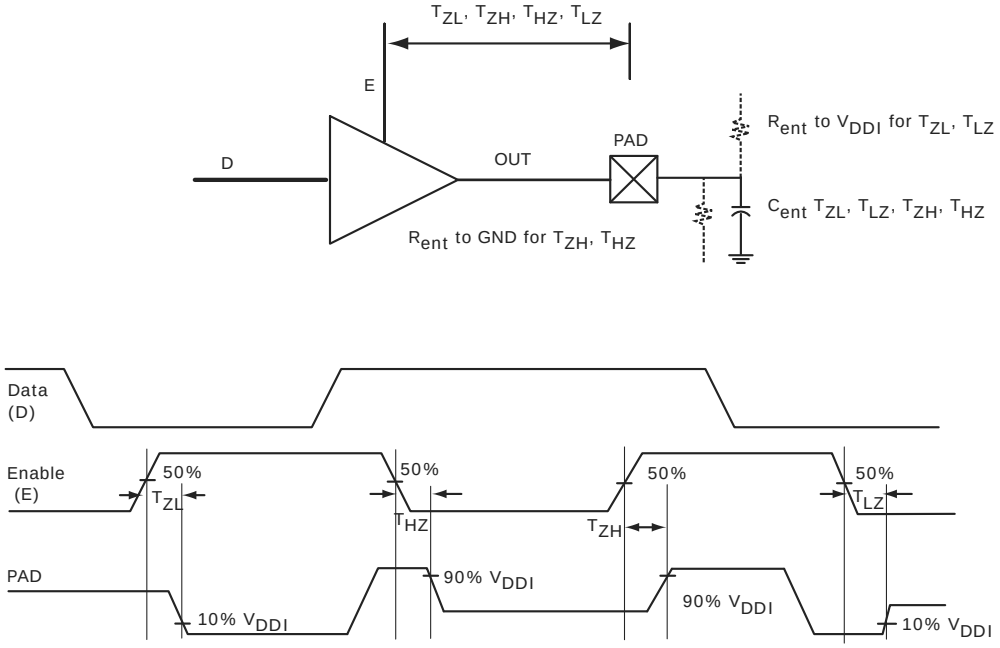
Table 17 • **Timing Model Parameters *(continued)***

Index	Symbol	Description	–1	Unit	For More Information
F	T_{DP}	Propagation delay of an OR gate	0.179	ns	See Table 223, page 76
G	T_{DP}	Propagation delay of an LVDS transmitter	2.136	ns	See Table 169, page 57
H	T_{DP}	Propagation delay of a three-input XOR Gate	0.241	ns	See Table 223, page 76
I	T_{DP}	Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 16 mA on the MSIO bank	2.412	ns	See Table 46, page 27
J	T_{DP}	Propagation delay of a two-input NAND gate	0.179	ns	See Table 223, page 76
K	T_{DP}	Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 8 mA on the MSIO bank	2.309	ns	See Table 46, page 27
L	T_{CLKQ}	Clock-to-Q of the data register	0.108	ns	See Table 224, page 77
	T_{SUD}	Setup time of the data register	0.254	ns	See Table 224, page 77
M	T_{DP}	Propagation delay of a two-input AND gate	0.179	ns	See Table 223, page 76
N	T_{OCLKQ}	Clock-to-Q of the output data register	0.263	ns	See Table 220, page 69
	T_{OSUD}	Setup time of the output data register	0.19	ns	See Table 220, page 69
O	T_{DP}	Propagation delay of SSTL2, Class I transmitter on the MSIO bank	2.055	ns	See Table 114, page 45
P	T_{DP}	Propagation delay of LVCMOS 1.5 V transmitter, drive strength of 12 mA, fast slew on the DDRIO bank	3.316	ns	See Table 70, page 34

2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

Figure 5 • **Tristate Buffer for Enable Path Test Point**



2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

Table 18 • **Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	630			Mbps
LVTTL 3.3 V	600			Mbps
LVCMOS 3.3 V	600			Mbps
LVCMOS 2.5 V	410	420	400	Mbps
LVCMOS 1.8 V	295	400	400	Mbps
LVCMOS 1.5 V	160	220	235	Mbps
LVCMOS 1.2 V	120	160	200	Mbps
LPDDR-LVCMOS 1.8 V mode			400	Mbps

Table 43 • **LVCMOS 2.5 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.2	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ωσ
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 44 • **LVCMOS 2.5 V Transmitter Drive Strength Specifications**

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (With Software Default Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	V_{DDI} – 0.4	0.4	2	2
4 mA	4 mA	4 mA	V_{DDI} – 0.4	0.4	4	4
6 mA	6 mA	6 mA	V_{DDI} – 0.4	0.4	6	6
8 mA	8 mA	8 mA	V_{DDI} – 0.4	0.4	8	8
12 mA	12 mA	12 mA	V_{DDI} – 0.4	0.4	12	12
16 mA		16 mA	V_{DDI} – 0.4	0.4	16	16

Note: For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V

Table 45 • **LVCMOS 2.5 V Receiver Characteristics (Input Buffers)**

	On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
		–1	–Std	–1	–Std	
LVCMOS 2.5 V (for DDRIO I/O bank)	None	1.823	2.145	1.932	2.274	ns
LVCMOS 2.5 V (for MSIO I/O bank)	None	2.486	2.925	2.495	2.935	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	None	2.29	2.694	2.305	2.712	ns

Table 46 • **LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		Unit
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	
2 mA	Slow	3.657	4.302	3.393	3.991	3.675	4.323	3.894	4.582	3.552	4.18	ns
	Medium	3.374	3.97	3.139	3.693	3.396	3.995	3.635	4.277	3.253	3.828	ns
	Medium fast	3.239	3.811	3.036	3.572	3.261	3.836	3.519	4.141	3.128	3.681	ns
	Fast	3.224	3.793	3.029	3.563	3.246	3.818	3.512	4.132	3.119	3.67	ns

Table 131 • **SSTL15 DC Output Voltage Specification (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DDR3/SSTL15 Class I (DDR3 Reduced Drive)				
DC output logic high	V_{OH}	0.8 × V_{DDI}		V
DC output logic low	V_{OL}		0.2 × V_{DDI}	V
Output minimum source DC current	I_{OH} at V_{OH}	6.5		mA
Output minimum sink current	I_{OL} at V_{OL}	–6.5		mA
DDR3/SSTL15 Class II (DDR3 Full Drive)				
DC output logic high	V_{OH}	0.8 × V_{DDI}		V
DC output logic low	V_{OL}		0.2 × V_{DDI}	V
Output minimum source DC current	I_{OH} at V_{OH}	7.6		mA
Output minimum sink current	I_{OL} at V_{OL}	–7.6		mA

Table 132 • **SSTL15 DC Differential Voltage Specification (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID}	0.2	V

Note: To meet JEDEC electrical compliance, use DDR3 full drive transmitter.

Table 133 • **SSTL15 AC SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF} (AC)	0.3		V
AC differential cross point voltage	V_x (AC)	0.5 × V_{DDI} – 0.150	0.5 × V_{DDI} + 0.150	V

Table 134 • **SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	667	Mbps	AC loading: per JEDEC specifications

Table 135 • **SSTL15 AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	R_{REF}	34, 40	Ω	Reference resistor = 240 Ω
Effective impedance value (ODT)	R_{TT}	20, 30, 40, 60, 120	Ω	Reference resistor = 240 Ω

2.3.7.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 173 • **B-LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V

Table 174 • **B-LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	2.925	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

1. See Table 24, page 22.

Table 175 • **B-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 176 • **B-LVDS DC Differential Voltage Specification**

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	V_{OD}	65	460	mV
Output common mode voltage (for MSIO I/O bank only)	V_{OCM}	1.1	1.5	V
Input common mode voltage	V_{ICM}	0.05	2.4	V
Input differential voltage	V_{ID}	0.1	V_{DDI}	V

Table 177 • **B-LVDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	500	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 178 • **B-LVDS AC Impedance Specifications**

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	27	Ω

Table 179 • **B-LVDS AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF

Table 198 • **Mini-LVDS AC Impedance Specifications**

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	100	Ω

Table 199 • **Mini-LVDS AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V.

Table 200 • **Mini-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	–1	–Std	Unit
None	2.855	3.359	ns
100	2.85	3.353	ns
None	2.602	3.061	ns
100	2.597	3.055	ns

Table 201 • **Mini-LVDS AC Switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)**

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	
2.097	2.467	2.308	2.715	2.296	2.701	1.964	2.31	1.949	2.293	ns

Table 202 • **Mini-LVDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	
No pre-emphasis	1.614	1.899	1.562	1.837	1.553	1.826	1.593	1.874	1.578	1.856	ns
Min pre-emphasis	1.604	1.887	1.745	2.053	1.731	2.036	1.892	2.225	1.861	2.189	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

2.3.8.2 Output/Enable Register

Figure 8 • Timing Model for Output/Enable Register

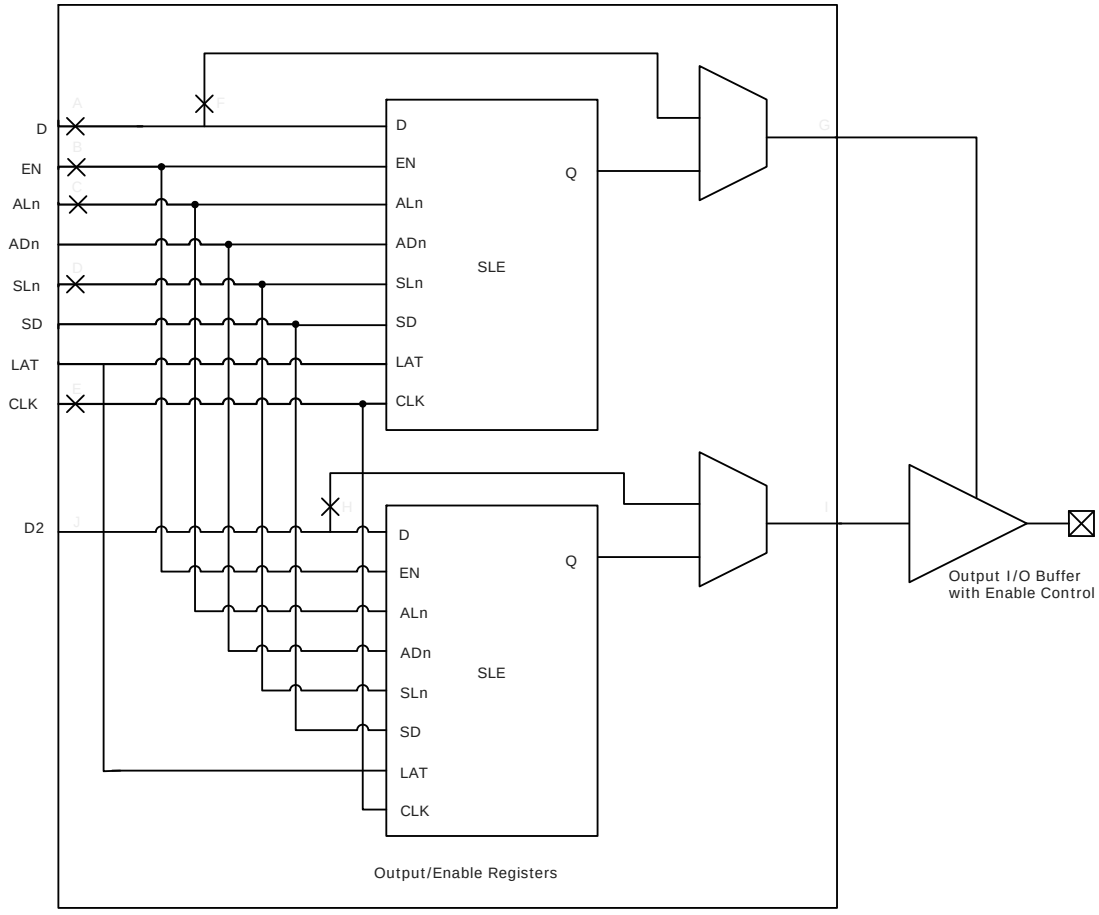
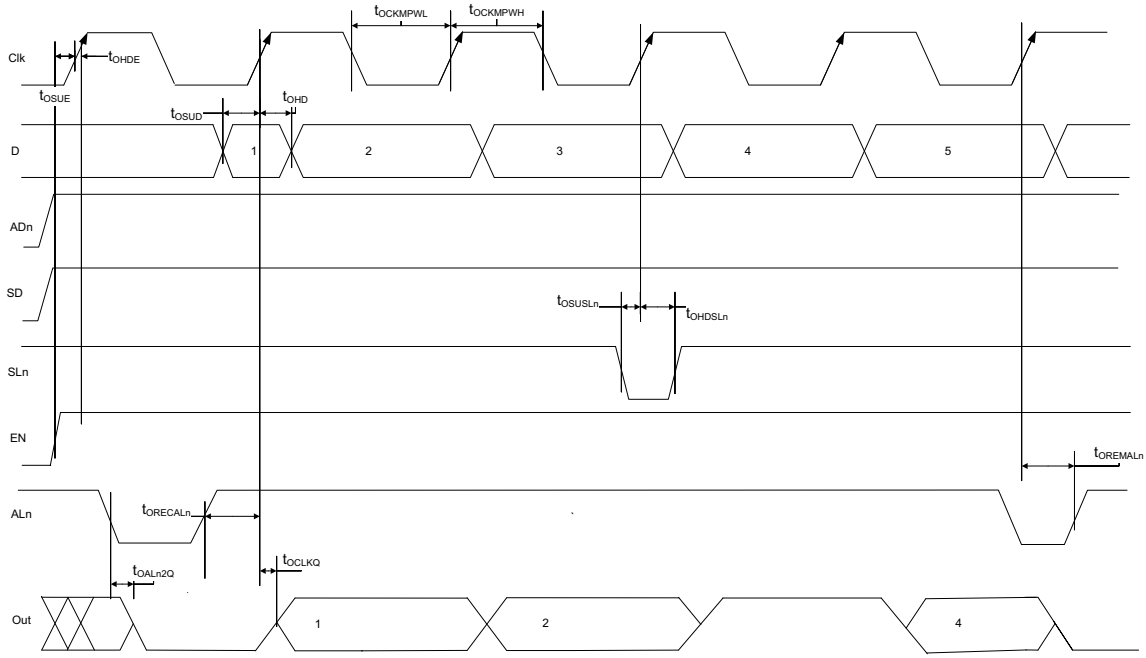


Figure 9 • **I/O Register Output Timing Diagram**



The following table lists the output/enable propagation delays in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 220 • **Output/Enable Data Register Propagation Delays**

Parameter	Symbol	Measuring Nodes (from, to)[1]	–1	–Std	Unit
Bypass delay of the output/enable register	T_{OBYP}	F, G or H, I	0.353	0.415	ns
Clock-to-Q of the output/enable register	T_{OCLKQ}	E, G or E, I	0.263	0.309	ns
Data setup time for the output/enable register	T_{OSUD}	A, E or J, E	0.19	0.223	ns
Data hold time for the output/enable register	T_{OHD}	A, E or J, E	0	0	ns
Enable setup time for the output/enable register	T_{OSUE}	B, E	0.419	0.493	ns
Enable hold time for the output/enable register	T_{OHE}	B, E	0	0	ns
Synchronous load setup time for the output/enable register	T_{OSUSL}	D, E	0.196	0.231	ns
Synchronous load hold time for the output/enable register	T_{OHSL}	D, E	0	0	ns
Asynchronous clear-to-q of the output/enable register (ADn = 1)	T_{OALN2Q}	C, G or C, I	0.505	0.594	ns
Asynchronous preset-to-q of the output/enable register (ADn = 0)		C, G or C, I	0.528	0.621	ns
Asynchronous load removal time for the output/enable register	$T_{OREMALN}$	C, E	0	0	ns
Asynchronous load recovery time for the output/enable register	$T_{ORECALN}$	C, E	0.034	0.04	ns
Asynchronous load minimum pulse width for the output/enable register	T_{OWALN}	C, C	0.304	0.357	ns
Clock minimum pulse width high for the output/enable register	$T_{OCKMPWH}$	E, E	0.075	0.088	ns
Clock minimum pulse width low for the output/enable register	$T_{OCKMPWL}$	E, E	0.159	0.187	ns

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

Table 221 • **Input DDR Propagation Delays *(continued)***

Symbol	Description	Measuring Nodes (from, to)	–1	–Std	Unit
$T_{DDRIWAL}$	Asynchronous load minimum pulse width for input DDR	F, F	0.304	0.357	ns
$T_{DDRICKMPWH}$	Clock minimum pulse width high for input DDR	B, B	0.075	0.088	ns
$T_{DDRICKMPWL}$	Clock minimum pulse width low for input DDR	B, B	0.159	0.187	ns

2.3.9.4 Output DDR Module

Figure 12 • Output DDR Module

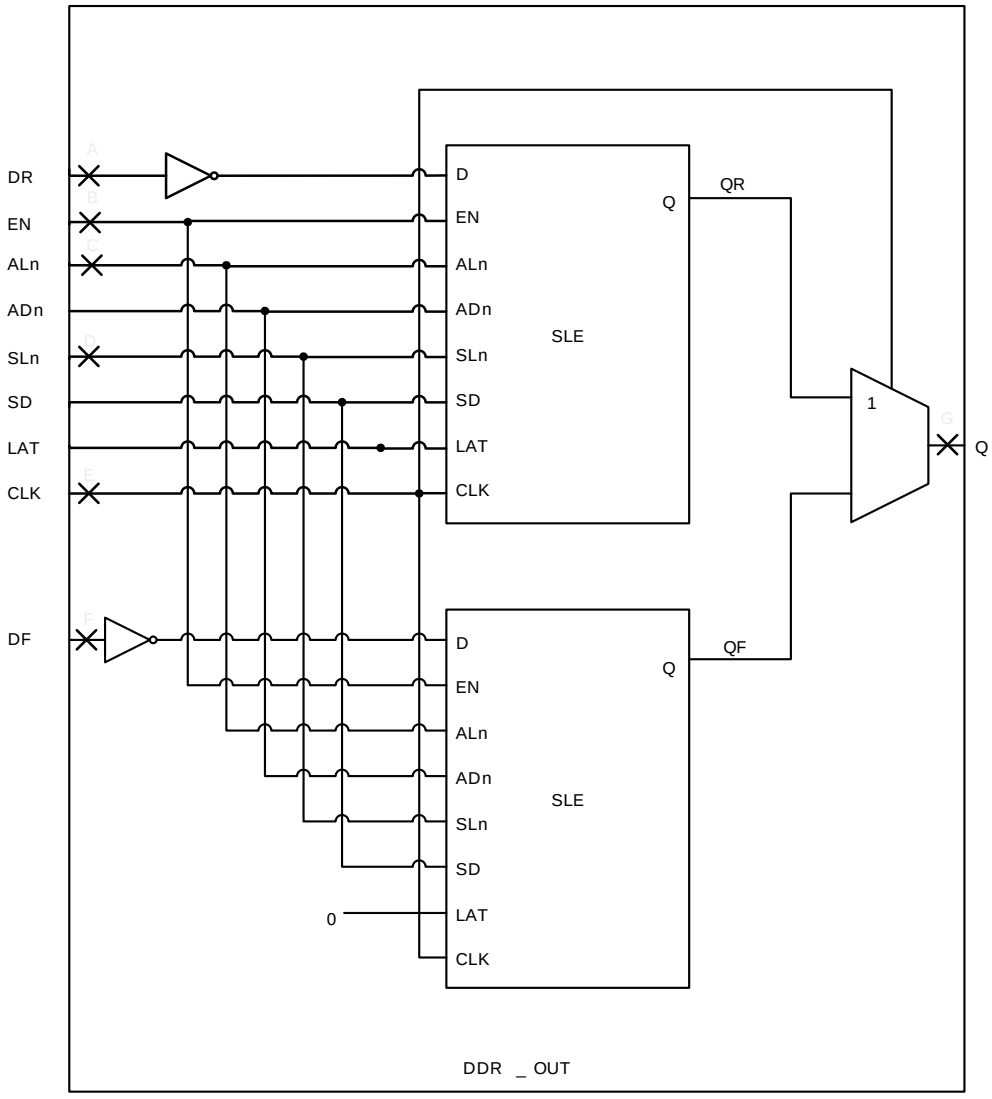


Table 232 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 *(continued)***

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Address setup time	T_{ADDRSU}	0.475		0.559		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.336		0.395		ns
Data hold time	T_{DHD}	0.082		0.096		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		1.529		1.799	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.485		0.57		ns
Read enable hold time	T_{RDEHD}	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}		1.514		1.781	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.415		0.488		ns
Write enable hold time	T_{WEHD}	0.048		0.057		ns
Maximum frequency	F_{MAX}		400		340	MHz

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 233 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns

The following table lists the RAM1K18 – two-port mode for depth × width configuration 512 × 36 in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 236 • **RAM1K18 – Two-Port Mode for Depth × Width Configuration 512 × 36**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register	T_{CLK2Q}		0.334		0.393	ns
Read access time without pipeline register			2.25		2.647	ns
Address setup time	T_{ADDRSU}	0.313		0.368		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.337		0.396		ns
Data hold time	T_{DHD}	0.111		0.13		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.201		0.237		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.25		2.647	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.449		0.528		ns
Read enable hold time	T_{RDEHD}	0.167		0.197		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}		1.506		1.772	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.39		0.458		ns
Write enable hold time	T_{WEHD}	0.242		0.285		ns
Maximum frequency	F_{MAX}		400		340	MHz

2.3.12.2 FPGA Fabric Micro SRAM (µSRAM)

The following table lists the µSRAM in 64 × 18 mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 237 • **µSRAM (RAM64x18) in 64 × 18 Mode**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		–0.778		–0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.839		0.987	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns

Table 237 • **µSRAM (RAM64x18) in 64 × 18 Mode *(continued)***

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the µSRAM in 64 × 16 mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 238 • **µSRAM (RAM64x16) in 64 × 16 Mode**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		–0.778		–0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.983	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 270 • **Math Block with Input Register Used and Output in Bypass Mode**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input register setup time	T_{MISU}	0.149		0.176		ns
Input register hold time	T_{MIHD}	0.185		0.218		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	0.08		0.094		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	–0.012		–0.014		ns
Asynchronous reset removal time	$T_{MARSTREM}$	–0.005		–0.005		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.088		0.104		ns
Input register clock to output delay	T_{MICQ}		2.52		2.964	ns
CDIN to output delay	$T_{MCDIN2Q}$		1.951		2.295	ns

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 271 • **Math Block with Input and Output in Bypass Mode**

		–1	–Std	
Parameter	**Symbol**	**Max**	**Max**	**Unit**
Input to output delay	T_{MIQ}	2.568	3.022	ns
CDIN to output delay	$T_{MCDIN2Q}$	1.951	2.295	ns

2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when V_{DD} = 1.14 V, V_{PPNVM} = V_{PP} = 2.375 V.

Table 272 • **eNVM Read Performance**

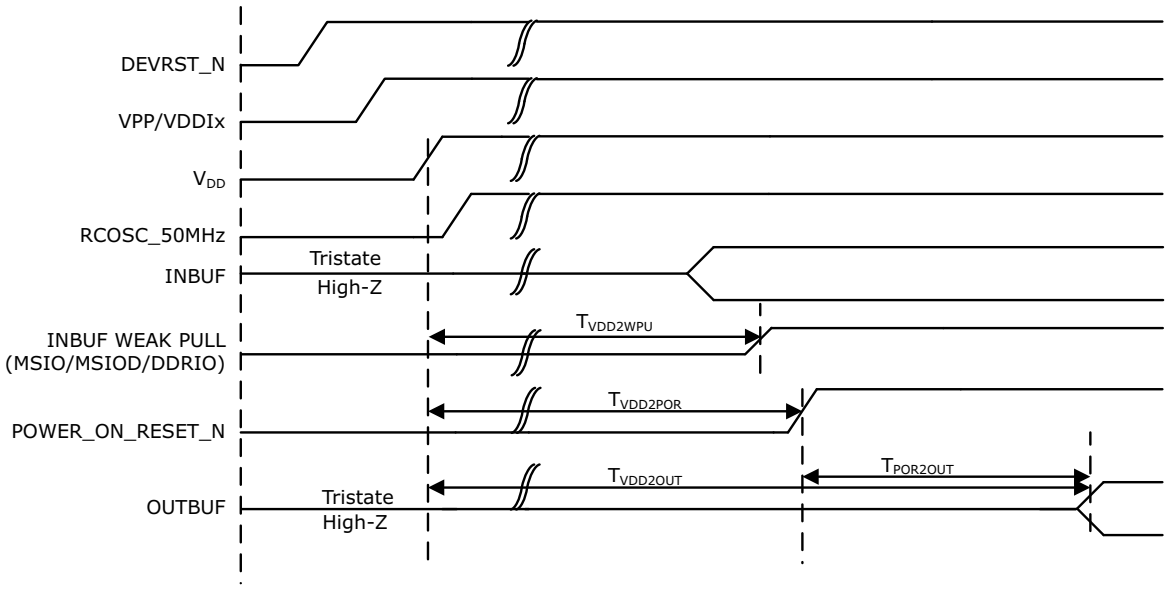
		Operating Temperature Range						
Symbol	**Description**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
T_J	Junction temperature range	–55 °C to 125 °C		–40 °C to 100 °C		0 °C to 85 °C		°C
$F_{MAXREAD}$	eNVM maximum read frequency	25	25	25	25	25	25	MHz

The following table lists the eNVM page programming in worst-case conditions when V_{DD} = 1.14 V, V_{PPNVM} = V_{PP} = 2.375 V.

Table 273 • **eNVM Page Programming**

		Operating Temperature Range						
Symbol	**Description**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
T_J	Junction temperature range	–55 °C to 125 °C		–40 °C to 100 °C		0 °C to 85 °C		°C
$T_{PAGEPGM}$	eNVM page programming time	40	40	40	40	40	40	ms

Figure 18 • **Power-up to Functional Timing Diagram for IGLOO2**



2.3.25 DEVRST_N Characteristics

Table 290 • **DEVRST_N Characteristics for All Devices**

Parameter	Symbol	Max	Unit
DEVRST_N ramp rate	$T_{RAMPDEVRSTN}$	1	us
DEVRST_N cycling rate	$F_{MAXPDEVRSTN}$	100	kHz

2.3.26 DEVRST_N to Functional Times

The following table lists the SmartFusion2 DEVRST_N to functional times in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 291 • **DEVRST_N to Functional Times for SmartFusion2**

				Maximum Power-up to Functional Time for SmartFusion2 (uS)						
Symbol	**From**	**To**	**Description**	**005**	**010**	**025**	**050**	**060**	**090**	**150**
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	518	501	527	521	422	419	694
$T_{POR2MSSRST}$	POWER_ON_RESET_N	MSS_RESET_N_M2F	Fabric to MSS	515	497	524	518	417	414	689
$T_{MSSRST2OUT}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.5	3.5	3.5	3.3	4.8	4.8	4.8
$T_{DEVRST2OUT}$	DEVRST_N	Output available at I/O	V_{DD} at its minimum threshold level to output	706	768	715	691	641	635	871

The following table lists the receiver pa in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 297 • **Receiver Parameters**

Symbol	Description	Min	Typ	Max	Unit
VRX-IN-PP-CC	Differential input peak-to-peak sensitivity (2.5 Gbps)	0.238		1.2	V
	Differential input peak-to-peak sensitivity (2.5 Gbps, de-emphasized)	0.219		1.2	V
	Differential input peak-to-peak sensitivity (5.0 Gbps)	0.300		1.2	V
	Differential input peak-to-peak sensitivity (5.0 Gbps, de-emphasized)	0.300		1.2	V
VRX-CM-AC-P	Input common mode range (AC coupled)			150	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset			15	µs
RLRX-DIFF	Return loss differential mode (2.5 Gbps)	–10			dB
	Return loss differential mode (5.0 Gbps)				
	0.05 GHz to 1.25 GHz	–10			dB
	1.25 GHz to 2.5 GHz	–8			dB
RLRX-CM	Return loss common mode (2.5 Gbps, 5.0 Gbps)	–6			dB
RX-CID[1]	CID limit PCIe Gen1/2			200	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65		175	mV

1. AC-coupled, BER = e^{-12}, using synchronous clock.

Table 298 • **SerDes Protocol Compliance**

Protocol	Maximum Data Rate (Gbps)	–1	–Std
PCIe Gen 1	2.5	Yes	Yes
PCIe Gen 2	5.0	Yes	
XAUI	3.125	Yes	
Generic EPCS	3.2	Yes	
Generic EPCS	2.5	Yes	Yes

2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 308 • **MMUART Characteristics**

Parameter	Description	–1	–Std	Unit
FMMUART_REF_CLK	Internally sourced MMUART reference clock frequency.	166	142	MHz
BAUDMMUARTTx	Maximum transmit baud rate	10.375	8.875	Mbps
BAUDMMUARTRx	Maximum receive baud rate	10.375	8.875	Mbps

2.3.35 IGLOO2 Specifications

2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 309 • **Maximum Frequency for HPMS Main Clock**

Symbol	Description	–1	–Std	Unit
HPMS_CLK	Maximum frequency for the HPMS main clock	166	142	MHz

2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, see Figure 23, page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 310 • **SPI Characteristics for All Devices**

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPIFMAX	Maximum operating frequency of SPI interface			20	MHz	
sp1	SPI_[0|1]_CLK minimum period					
	SPI_[0|1]_CLK = PCLK/2	12			ns	
	SPI_[0|1]_CLK = PCLK/4	24.1			ns	
	SPI_[0|1]_CLK = PCLK/8	48.2			ns	
	SPI_[0|1]_CLK = PCLK/16	0.1			µs	
	SPI_[0|1]_CLK = PCLK/32	0.19			µs	
	SPI_[0|1]_CLK = PCLK/64	0.39			µs	
	SPI_[0|1]_CLK = PCLK/128	0.77			µs	