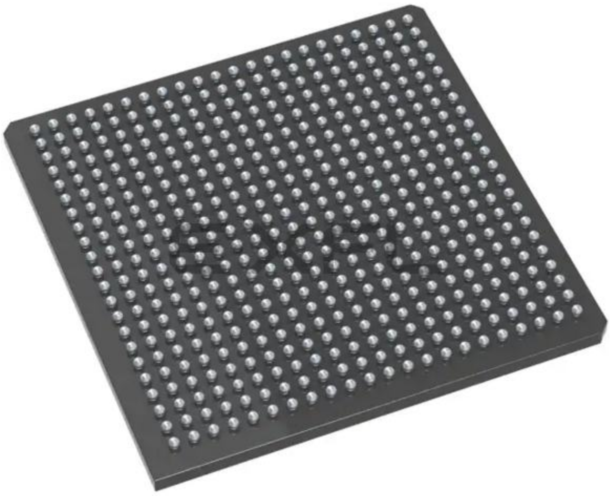

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 86316 |
| Total RAM Bits | 2648064 |
| Number of I/O | 267 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2gl090t-fg484 |

# 1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- Updated Table 24, page 22 with minimum and maximum values for input current low and high (SAR 73114 and 80314).
- Added Non-Deterministic Random Bit Generator (NRBG) Characteristics, page 106 (SAR 73114 and 79517).
- Added 060 device in Table 282, page 110 (SAR 79860).
- Added DEVRST_N to Functional Times, page 116 (SAR 73114).
- Added Cryptographic Block Characteristics, page 106 (SAR 73114 and 79516).
- Update Table 296, page 121 with VTX-AMP details (SAR 81756).
- Update note in Table 297, page 122 (SAR 74570 and 80677).
- Update Table 298, page 122 with generic EPCS details (SAR 75307).
- Added Table 308, page 129 (SAR 50424).

## 1.2 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- The Surge Current on VDD during DEVRST_B Assertion and Surge Current on VDD during Digest Check using System Services tables were deleted and added reference to *AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note*. (SAR 76865 and 76623).
- Added 060 device in Table 4, page 6 (SAR 76383).
- Updated Table 24, page 22 for ramp time input (SAR 72103).
- Added 060 device details in Table 284, page 112 (SAR 74927).
- Updated Table 290, page 116 for name change (SAR 74925).
- Updated Table 283, page 111 for 060 FG676 Package details (SAR 78849).
- Updated Table 305, page 126 for SmartFusion2 and Table 310, page 129 for IGLOO2 for SPI timing and Fmax (SAR 56645, 75331).
- Updated Table 293, page 119 for Flash*Freeze entry and exit times (SAR 75329, 75330).
- Updated Table 297, page 122 for RX-CID information (SAR 78271).
- Added Table 8, page 8 and Figure 1, page 9 (SAR 78932).
- Updated Table 223, page 76 for timing characteristics and Table 224, page 77(SAR 75998).
- Added SRAM PUF, page 105 (SAR 64406).
- Added a footnote on digest cycle in Table 5, page 7 (SAR 79812).

## 1.3 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document.

- Added a note in Table 5, page 7 (SAR 71506).
- Added a note in Table 6, page 8 (SAR 74616).
- Added a note in Figure 3, page 17 (SAR 71506).
- Updated Quiescent Supply Current for 060 in Table 11, page 12 and Table 12, page 13 (SAR 74483).
- Updated programming currents for 060 in Table 13, page 13, Table 14, page 13, and Table 15, page 14.
- Added DEVRST_B assertion tables (SAR 74708).
- Updated I/O speeds for LVDS 3.3 V in Table 18, page 19 and Table 21, page 20 (SAR 69829).
- Updated Table 24, page 22 (SAR 69418).
- Updated Table 25, page 22, Table 26, page 23, Table 27, page 23 (SAR 74570).
- Updated all AC/DC table to link to the Input Capacitance, Leakage Current, and Ramp Time, page 22 for reference (SAR 69418).

***Table 4 •*** **Recommended Operating Conditions *(continued)***

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| 3.3 V DC supply voltage | $V_{DDIx}$ | 3.15 | 3.3 | 3.45 | V | |
| LVDS differential I/O | $V_{DDIx}$ | 2.375 | 2.5 | 3.45 | V | |
| B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O | $V_{DDIx}$ | 2.375 | 2.5 | 2.625 | V | |
| LVPECL differential I/O | $V_{DDIx}$ | 3.15 | 3.3 | 3.45 | V | |
| Reference voltage supply for FDDR (Bank0) and MDDR (Bank5) | $V_{REFx}$ | 0.49 × $V_{DDIx}$ | 0.5 × $V_{DDIx}$ | 0.51 × $V_{DDIx}$ | V | |
| Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to $V_{PP}$. | $V_{PPNVM}$ | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |

1. Programming at Industrial temperature range is available only with $V_{PP}$ = 3.3 V.

**Note:** Power supply ramps must all be strictly monotonic, without plateaus.

***Table 5 •*** **FPGA Operating Limits**

| Product Grade | Element | Programming Temperature | Operating Temperature | Programming Cycles | Digest Temperature | Digest Cycles | Retention (Biased/ Unbiased) |
|---|---|---|---|---|---|---|---|
| Commercial | FPGA | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | 500 | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | 2000 | 20 years |
| Industrial[1] | FPGA | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | 500 | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | 2000 | 20 years |

1. Programming at Industrial temperature range is available only with VPP = 3.3 V.

**Note:** The retention specification is defined as the total number of programing and digest cycles. For example, 20 years of retention after 500 programming cycles.

**Note:** The digest cycle specification is 2000 digest cycles for every program cycle with a maximum of 500 programming cycles.

**Note:** If your product qualification requires accelerated programming cycles, see *Microsemi SoC Products Quality and Reliability Report* about recommended methodologies.

The following table lists the embedded operating flash limits.

***Table 6 •*** **Embedded Operating Flash Limits**

| **Product Grade** | **Element** | **Programming Temperature** | **Maximum Operating Temperature** | **Programming Cycles** | **Retention (Biased/Unbiased)** |
|---|---|---|---|---|---|
| Commercial | Embedded flash | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | < 1000 cycles per page, up to two million cycles per eNVM array | 20 years |
| | | | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | < 10000 cycles per page, up to 20 million cycles per eNVM array | 10 years |
| Industrial | Embedded flash | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | < 1000 cycles per page, up to two million cycles per eNVM array | 20 years |
| | | | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | < 10000 cycles per page, up to 20 million cycles per eNVM array | 10 years |

**Note:** If your product qualification requires accelerated programming cycles, see *Microsemi SoC Products Quality and Reliability Report* about recommended methodologies.

***Table 7 •*** **Device Storage Temperature and Retention**

| **Product Grade** | **Storage Temperature (Tstg)** | **Retention** |
|---|---|---|
| Commercial | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | 20 years |
| Industrial | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | 20 years |

***Table 8 •*** **High Temperature Data Retention (HTR) Lifetime**

| **$T_J$ (C)** | **HTR Lifetime[1] (yrs)** |
|---|---|
| 90 | 20.5 |
| 95 | 20.5 |
| 100 | 20.5 |
| 105 | 17.0 |
| 110 | 15.0 |
| 115 | 13.0 |
| 120 | 11.5 |
| 125 | 10.0 |
| 130 | 8.0 |
| 135 | 6.0 |
| 140 | 4.5 |
| 145 | 3.0 |
| 150 | 1.5 |

1. HTR Lifetime is the period during which a verify failure is not expected due to flash leakage.

where

$\theta_{JA}$ = Junction-to-air thermal resistance

$\theta_{JB}$ = Junction-to-board thermal resistance

$\theta_{JC}$ = Junction-to-case thermal resistance

$T_J$ = Junction temperature

$T_A$ = Ambient temperature

$T_B$ = Board temperature (measured 1.0 mm away from the package edge)

$T_C$ = Case temperature

P = Total power dissipated by the device

***Table 9 •*** **Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices**

| | **Still Air** | **1.0 m/s** | **2.5 m/s** | | | |
|---|---|---|---|---|---|---|
| **Device** | | $\theta_{JA}$ | | $\theta_{JB}$ | $\theta_{JC}$ | **Unit** |
| **005** | | | | | | |
| FG484 | 19.36 | 15.81 | 14.63 | 9.74 | 5.27 | °C/W |
| VF256 | 41.30 | 38.16 | 35.30 | 28.41 | 3.94 | °C/W |
| VF400 | 20.19 | 16.94 | 15.41 | 8.86 | 4.95 | °C/W |
| TQ144 | 42.80 | 36.80 | 34.50 | 37.20 | 10.80 | °C/W |
| **010** | | | | | | |
| FG484 | 18.22 | 14.83 | 13.62 | 8.83 | 4.92 | °C/W |
| VF256 | 37.36 | 34.26 | 31.45 | 24.84 | 7.89 | °C/W |
| VF400 | 19.40 | 15.75 | 14.22 | 8.11 | 4.22 | °C/W |
| TQ144 | 38.60 | 32.60 | 30.30 | 31.80 | 8.60 | °C/W |
| **025** | | | | | | |
| FG484 | 17.03 | 13.66 | 12.45 | 7.66 | 4.18 | °C/W |
| VF256 | 33.85 | 30.59 | 27.85 | 21.63 | 6.13 | °C/W |
| VF400 | 18.36 | 14.89 | 13.36 | 7.12 | 3.41 | °C/W |
| FCS325 | 29.17 | 24.87 | 23.12 | 14.44 | 2.31 | °C/W |
| **050** | | | | | | |
| FG484 | 15.29 | 12.19 | 10.99 | 6.27 | 3.24 | °C/W |
| FG896 | 14.70 | 12.50 | 10.90 | 7.20 | 4.90 | °C/W |
| VF400 | 17.53 | 14.17 | 12.63 | 6.32 | 2.81 | °C/W |
| FCS325 | 27.38 | 23.18 | 21.41 | 12.47 | 1.59 | °C/W |
| **060** | | | | | | |
| FG484 | 15.40 | 12.06 | 10.85 | 6.14 | 3.15 | °C/W |
| FG676 | 15.49 | 12.21 | 11.06 | 7.07 | 3.87 | °C/W |
| VF400 | 17.45 | 14.01 | 12.47 | 6.22 | 2.69 | °C/W |
| FCS325 | 27.03 | 22.91 | 21.25 | 12.33 | 1.54 | °C/W |
| **090** | | | | | | |
| FG484 | 14.64 | 11.37 | 10.16 | 5.43 | 2.77 | °C/W |
| FG676 | 14.52 | 11.19 | 10.37 | 6.17 | 3.24 | °C/W |
| FCS325 | 26.63 | 22.26 | 20.13 | 14.24 | 2.50 | °C/W |

**Table 11 • SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD}$ = 1.2 V) – Typical Process**

| Symbol | Modes | 005 | 010 | 025 | 050 | 060 | 090 | 150 | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| IDC2 | Flash*Freeze | 1.4 | 2.6 | 3.7 | 5.1 | 5.0 | 5.1 | 8.9 | mA | Typical ($T_J$ = 25 °C) |
| | | 12.0 | 20.0 | 26.6 | 35.3 | 35.4 | 35.7 | 57.8 | mA | Commercial ($T_J$ = 85 °C) |
| | | 18.5 | 30.8 | 41.0 | 54.5 | 54.5 | 55.0 | 89.0 | mA | Industrial ($T_J$ = 100 °C) |

**Table 12 • SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD}$ = 1.26 V) – Worst-Case Process**

| Symbol | Modes | 005 | 010 | 025 | 050 | 060 | 090 | 150 | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| IDC1 | Non-Flash*Freeze | 43.8 | 57.0 | 84.6 | 132.3 | 161.4 | 163.0 | 242.5 | mA | Commercial ($T_J$= 85 °C) |
| | | 65.3 | 85.7 | 127.8 | 200.9 | 245.4 | 247.8 | 369.0 | mA | Industrial ($T_J$ = 100 °C) |
| IDC2 | Flash*Freeze | 29.1 | 45.6 | 51.7 | 62.7 | 69.3 | 70.0 | 84.8 | mA | Commercial ($T_J$ = 85 °C) |
| | | 44.9 | 70.3 | 79.7 | 96.5 | 106.8 | 107.8 | 130.6 | mA | Industrial ($T_J$ = 100 °C) |

## 2.3.2.2 Programming Currents

The following tables represent programming, verify and Inrush currents for SmartFusion2 SoC and IGLOO2 FPGA devices.

**Table 13 • Currents During Program Cycle, 0 °C < = $T_J$ <= 85 °C – Typical Process**

| Power Supplies | Voltage (V) | 005 | 010 | 025 | 050 | 060 | 090 | 150[1] | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | 1.26 | 46 | 53 | 55 | 58 | 30 | 42 | 52 | mA |
| $V_{PP}$ | 3.46 | 8 | 11 | 6 | 10 | 9 | 12 | 12 | mA |
| $V_{PPNVM}$ | 3.46 | 1 | 2 | 2 | 3 | 3 | 3 | | mA |
| $V_{DDI}$ | 2.62 | 31 | 16 | 17 | 1 | 12 | 12 | 81 | mA |
| | 3.46 | 62 | 31 | 36 | 1 | 12 | 17 | 84 | mA |
| Number of banks | | 7 | 8 | 8 | 10 | 10 | 9 | 19 | |

1. $V_{PP}$ and $V_{PPNVM}$ are internally shorted.

**Table 14 • Currents During Verify Cycle, 0 °C <= $T_J$ <= 85 °C – Typical Process**

| Power Supplies | Voltage (V) | 005 | 010 | 025 | 050 | 060 | 090 | 150[1] | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | 1.26 | 44 | 53 | 55 | 58 | 33 | 41 | 51 | mA |
| $V_{PP}$ | 3.46 | 6 | 5 | 3 | 15 | 8 | 11 | 12 | mA |
| $V_{PPNVM}$ | 3.46 | 1 | 0 | 0 | 1 | 1 | 1 | | mA |
| $V_{DDI}$ | 2.62 | 31 | 16 | 17 | 1 | 12 | 11 | 81 | mA |
| | 3.46 | 61 | 32 | 36 | 1 | 12 | 17 | 84 | mA |
| Number of banks | | 7 | 8 | 8 | 10 | 10 | 9 | 19 | |

1. $V_{PP}$ and $V_{PPNVM}$ are internally shorted.

### 2.3.5.6 Single-Ended I/O Standards

#### 2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

#### 2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 29 •*** **LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 3.15 | 3.3 | 3.45 | V |

***Table 30 •*** **LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | 2.0 | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.8 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 31 •*** **LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high[1] | $V_{OH}$ | $V_{DDI}$ – 0.4 | | V |
| DC output logic low[1] | $V_{OL}$ | | 0.4 | V |

1. The $V_{OH}$/$V_{OL}$ test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

***Table 32 •*** **LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 2.4 | | V |
| DC output logic low | $V_{OL}$ | | 0.4 | V |

***Table 33 •*** **LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 600 | Mbps | AC loading: 17 pF load, maximum drive/slew |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 3.0 V

***Table 91 •*** **PCI/PCIX AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)**

| | $T_{PY}$ | | $T_{PYS}$ | | |
|---|---|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| None | 2.229 | 2.623 | 2.238 | 2.633 | ns |

***Table 92 •*** **PCI/PCIX AC switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2.146 | 2.525 | 2.043 | 2.404 | 2.084 | 2.452 | 6.095 | 7.171 | 5.558 | 6.539 | ns |

## 2.3.6 Memory Interface and Voltage Referenced I/O Standards

This section describes High-Speed Transceiver Logic (HSTL) memory interface and voltage reference I/O standards.

### 2.3.6.1 High-Speed Transceiver Logic (HSTL)

The HSTL standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO2 FPGA and SmartFusion2 SoC FPGA devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification (Applicable to DDRIO Bank Only)**

***Table 93 •*** **HSTL Recommended DC Operating Conditions**

| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.425 | 1.5 | 1.575 | V |
| Termination voltage | $V_{TT}$ | 0.698 | 0.750 | 0.803 | V |
| Input reference voltage | $V_{REF}$ | 0.698 | 0.750 | 0.803 | V |

***Table 94 •*** **HSTL DC Input Voltage Specification**

| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** |
|---|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | $V_{REF}$ + 0.1 | 1.575 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | $V_{REF}$ – 0.1 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

### 2.3.6.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 103 •*** **DDR1/SSTL2 DC Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |
| Termination voltage | $V_{TT}$ | 1.164 | 1.250 | 1.339 | V |
| Input reference voltage | $V_{REF}$ | 1.164 | 1.250 | 1.339 | V |

***Table 104 •*** **DDR1/SSTL2 DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | $V_{REF}$ + 0.15 | 2.625 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | VREF – 0.15 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 105 •*** **DDR1/SSTL2 DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **SSTL2 Class I (DDR Reduced Drive)** | | | | |
| DC output logic high | $V_{OH}$ | $V_{TT}$ + 0.608 | | V |
| DC output logic low | $V_{OL}$ | | $V_{TT}$ – 0.608 | V |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 8.1 | | mA |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –8.1 | | mA |
| **SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Bank Only** | | | | |
| DC output logic high | $V_{OH}$ | $V_{TT}$ + 0.81 | | V |
| DC output logic low | $V_{OL}$ | | $V_{TT}$ – 0.81 | V |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 16.2 | | mA |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –16.2 | | mA |

***Table 106 •*** **DDR1/SSTL2 DC Differential Voltage Specification**

| Parameter | Symbol | Min | Unit |
|---|---|---|---|
| DC input differential voltage | $V_{ID}$ (DC) | 0.3 | V |

### *2.3.7.5 RSDS*

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

**Minimum and Maximum Input and Output Levels**

***Table 203 •*** **RSDS Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

***Table 204 •*** **RSDS DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input voltage | $V_I$ | 0 | 2.925 | V |

***Table 205 •*** **RSDS DC Output Voltage Specification**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

***Table 206 •*** **RSDS Differential Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Differential output voltage swing | $V_{OD}$ | 100 | 600 | mV |
| Output common mode voltage | $V_{OCM}$ | 0.5 | 1.5 | V |
| Input common mode voltage | $V_{ICM}$ | 0.3 | 1.5 | V |
| Input differential voltage | $V_{ID}$ | 100 | 600 | mV |

***Table 207 •*** **RSDS Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 520 | Mbps | AC loading: 2 pF / 100 Ω differential load |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 700 | Mbps | AC loading: 2 pF / 100 Ω differential load |

***Table 208 •*** **RSDS AC Impedance Specifications**

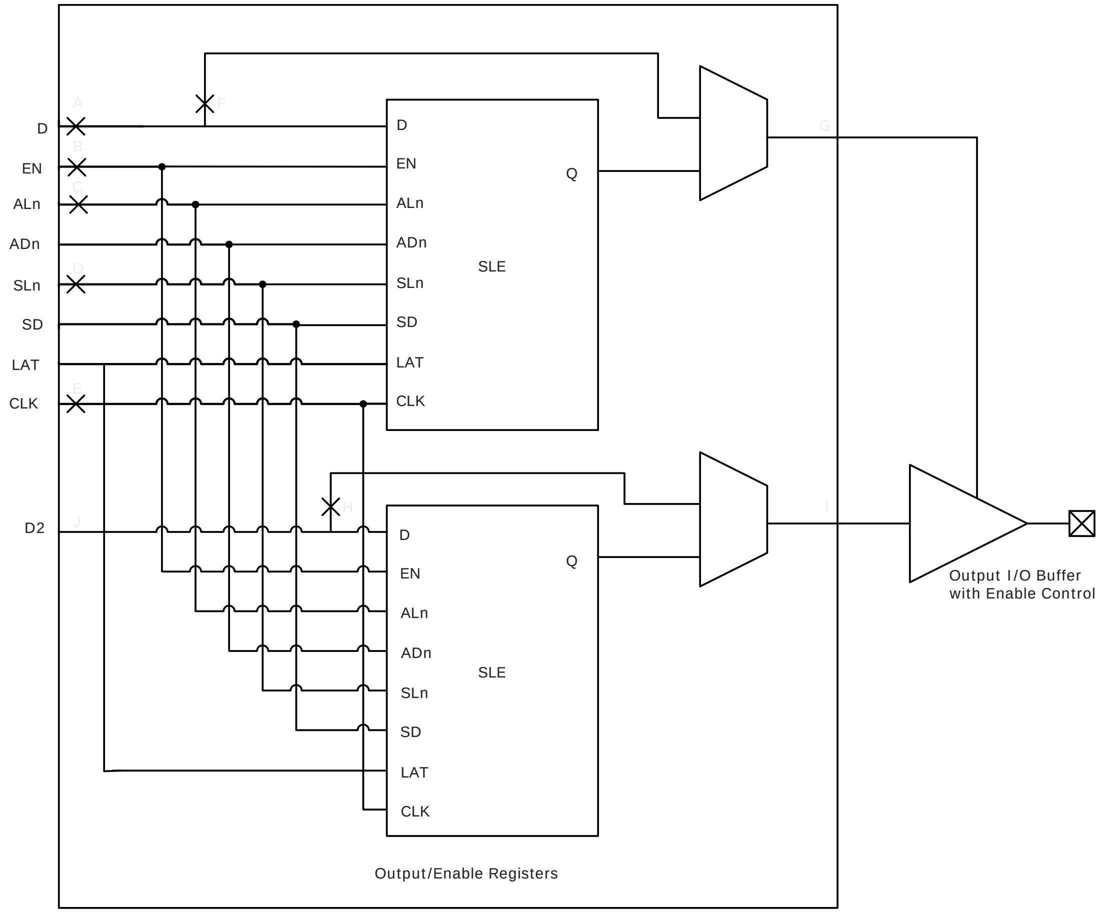
| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Termination resistance | RT | 100 | Ω |

***Table 209 •*** **RSDS AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | Cross point | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |

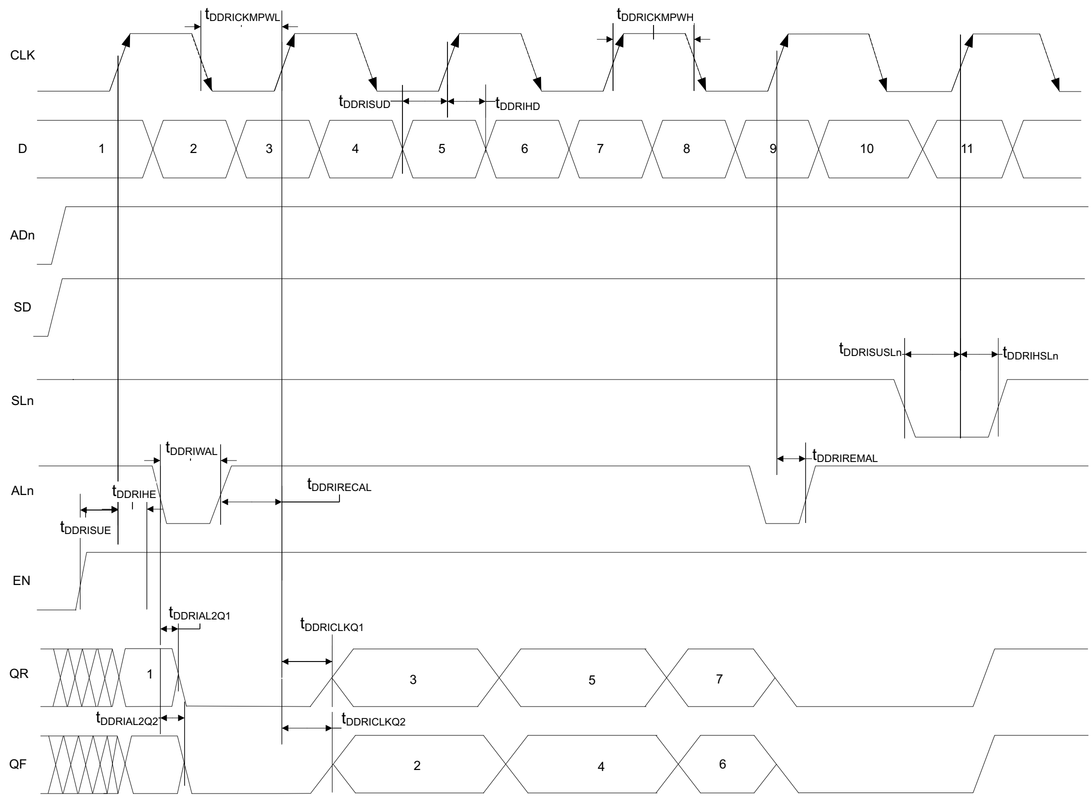
### 2.3.8.2 Output/Enable Register

**Figure 8 • Timing Model for Output/Enable Register**



### *2.3.9.2 Input DDR Timing Diagram*

***Figure 11 •*** **Input DDR Timing Diagram**



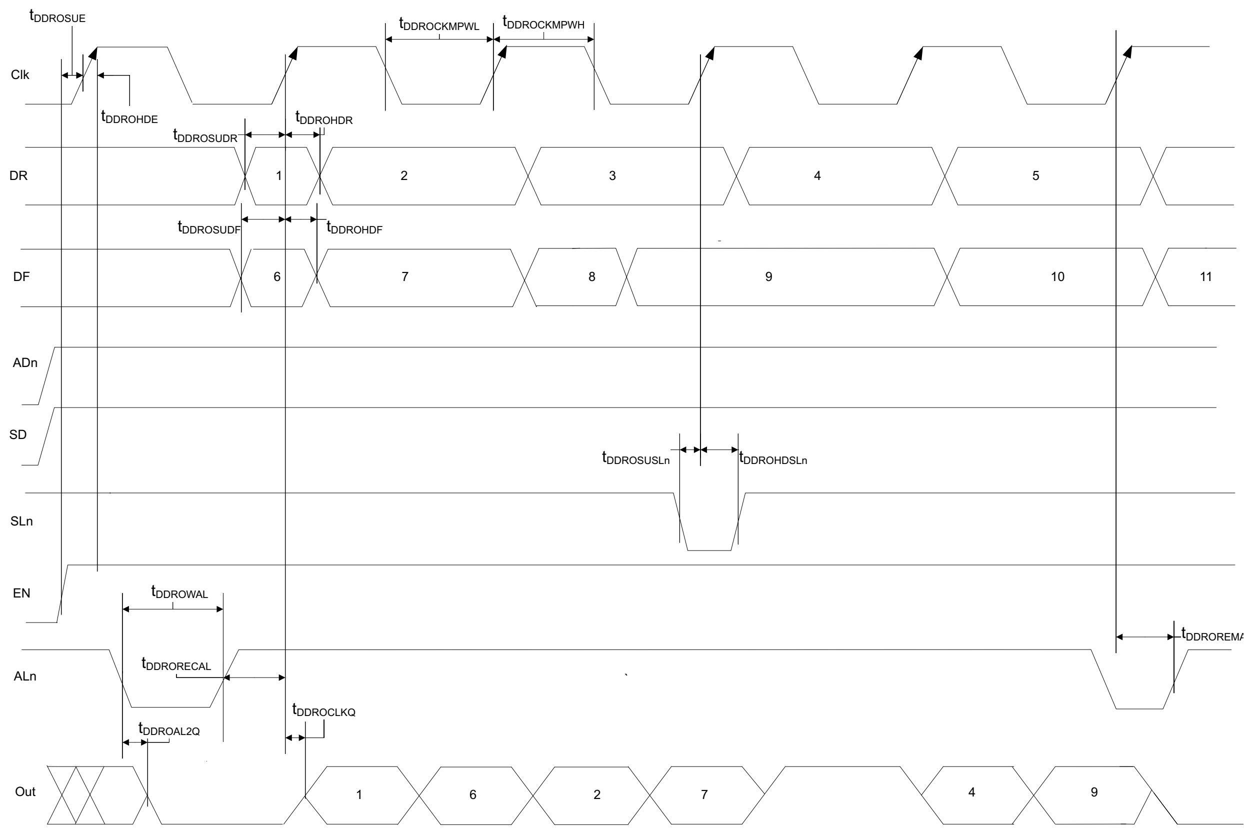

### *2.3.9.3 Timing Characteristics*

The following table lists the input DDR propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 221 •*** **Input DDR Propagation Delays**

| Symbol | Description | Measuring Nodes (from, to) | –1 | –Std | Unit |
|---|---|---|---|---|---|
| $T_{DDRICLKQ1}$ | Clock-to-Out Out_QR for input DDR | B, C | 0.16 | 0.188 | ns |
| $T_{DDRICLKQ2}$ | Clock-to-Out Out_QF for input DDR | B, D | 0.166 | 0.195 | ns |
| $T_{DDRISUD}$ | Data setup for input DDR | A, B | 0.357 | 0.421 | ns |
| $T_{DDRIHD}$ | Data hold for input DDR | A, B | 0 | 0 | ns |
| $T_{DDRISUE}$ | Enable setup for input DDR | E, B | 0.46 | 0.542 | ns |
| $T_{DDRIHE}$ | Enable hold for input DDR | E, B | 0 | 0 | ns |
| $T_{DDRISUSLN}$ | Synchronous load setup for input DDR | G, B | 0.46 | 0.542 | ns |
| $T_{DDRIHSLN}$ | Synchronous load hold for input DDR | G, B | 0 | 0 | ns |
| $T_{DDRIAL2Q1}$ | Asynchronous load-to-out QR for input DDR | F, C | 0.587 | 0.69 | ns |
| $T_{DDRIAL2Q2}$ | Asynchronous load-to-out QF for input DDR | F, D | 0.541 | 0.636 | ns |
| $T_{DDRIREMAL}$ | Asynchronous load removal time for input DDR | F, B | 0 | 0 | ns |
| $T_{DDRIRECAL}$ | Asynchronous load recovery time for input DDR | F, B | 0.074 | 0.087 | ns |

**Figure 13 •** **Output DDR Timing Diagram**




### *2.3.9.5 Timing Characteristics*

The following table lists the output DDR propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

**Table 222 •** **Output DDR Propagation Delays**

| Symbol | Description | Measuring Nodes (from, to) | –1 | –Std | Unit |
|---|---|---|---|---|---|
| $T_{DDROCLKQ}$ | Clock-to-out of DDR for output DDR | E, G | 0.263 | 0.309 | ns |
| $T_{DDROSUDF}$ | Data_F data setup for output DDR | F, E | 0.143 | 0.168 | ns |
| $T_{DDROSUDR}$ | Data_R data setup for output DDR | A, E | 0.19 | 0.223 | ns |
| $T_{DDROHDF}$ | Data_F data hold for output DDR | F, E | 0 | 0 | ns |
| $T_{DDROHDR}$ | Data_R data hold for output DDR | A, E | 0 | 0 | ns |
| $T_{DDROSUE}$ | Enable setup for input DDR | B, E | 0.419 | 0.493 | ns |
| $T_{DDROHE}$ | Enable hold for input DDR | B, E | 0 | 0 | ns |
| $T_{DDROSUSLN}$ | Synchronous load setup for input DDR | D, E | 0.196 | 0.231 | ns |
| $T_{DDROHSLN}$ | Synchronous load hold for input DDR | D, E | 0 | 0 | ns |
| $T_{DDROAL2Q}$ | Asynchronous load-to-out for output DDR | C, G | 0.528 | 0.621 | ns |
| $T_{DDROREMAL}$ | Asynchronous load removal time for output DDR | C, E | 0 | 0 | ns |
| $T_{DDRORECAL}$ | Asynchronous load recovery time for output DDR | C, E | 0.034 | 0.04 | ns |

### 2.3.10.2 Timing Characteristics

The following table lists the combinatorial cell propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 223 •*** **Combinatorial Cell Propagation Delays**

| Combinatorial Cell | Equation | Symbol | –1 | –Std | Unit |
|---|---|---|---|---|---|
| INV | Y = !A | $T_{PD}$ | 0.1 | 0.118 | ns |
| AND2 | Y = A · B | $T_{PD}$ | 0.164 | 0.193 | ns |
| NAND2 | Y = !(A · B) | $T_{PD}$ | 0.147 | 0.173 | ns |
| OR2 | Y = A + B | $T_{PD}$ | 0.164 | 0.193 | ns |
| NOR2 | Y = !(A + B) | $T_{PD}$ | 0.147 | 0.173 | ns |
| XOR2 | $Y = A \oplus B$ | $T_{PD}$ | 0.164 | 0.193 | ns |
| XOR3 | $Y = A \oplus B \oplus C$ | $T_{PD}$ | 0.225 | 0.265 | ns |
| AND3 | Y = A · B · C | $T_{PD}$ | 0.209 | 0.246 | ns |
| AND4 | Y = A · B · C · D | $T_{PD}$ | 0.287 | 0.338 | ns |

### 2.3.10.3 Sequential Module

IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

***Figure 15 •*** **Sequential Module**

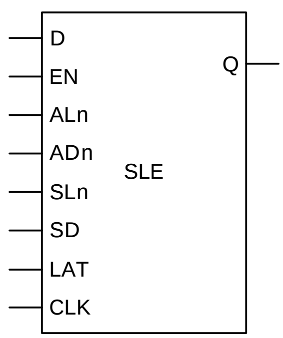


***Table 242 •*** **µSRAM (RAM512x2) in 512 × 2 Mode *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.101 | | 0.118 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.137 | | 0.161 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.247 | | 0.29 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.03 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 1024 × 1 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 243 •*** **µSRAM (RAM1024x1) in 1024 × 1 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.27 | | 0.31 | ns |
| Read access time without pipeline register | | | 1.78 | | 2.1 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.978 | | 2.327 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.137 | | 0.161 | | ns |
| Read address hold time in asynchronous mode | | –0.6 | | –0.71 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.77 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.16 | | 2.54 | ns |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.02 | | –0.03 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |

*Table 248 •* **2 Step IAP Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 137536 | 2 | 37 | 5 | Sec |
| 010 | 274816 | 4 | 76 | 11 | Sec |
| 025 | 274816 | 4 | 78 | 10 | Sec |
| 050 | 278528 | 3 | 85 | 9 | Sec |
| 060 | 268480 | 5 | 76 | 22 | Sec |
| 090 | 544496 | 10 | 152 | 43 | Sec |
| 150 | 544496 | 10 | 153 | 44 | Sec |

*Table 249 •* **2 Step IAP Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 439296 | 6 | 56 | 11 | Sec |
| 010 | 842688 | 11 | 100 | 21 | Sec |
| 025 | 1497408 | 19 | 113 | 32 | Sec |
| 050 | 2695168 | 32 | 136 | 48 | Sec |
| 060 | 2686464 | 43 | 137 | 70 | Sec |
| 090 | 4190208 | 68 | 236 | 115 | Sec |
| 150 | 6682768 | 109 | 286 | 162 | Sec |

*Table 250 •* **SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 302672 | 6 | 19 | 8 | Sec |
| 010 | 568784 | 10 | 26 | 14 | Sec |
| 025 | 1223504 | 21 | 39 | 29 | Sec |
| 050 | 2424832 | 39 | 60 | 50 | Sec |
| 060 | 2418896 | 44 | 65 | 54 | Sec |
| 090 | 3645968 | 66 | 90 | 79 | Sec |
| 150 | 6139184 | 108 | 140 | 128 | Sec |

*Table 251 •* **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 137536 | 3 | 42 | 4 | Sec |
| 010 | 274816 | 4 | 82 | 7 | Sec |
| 025 | 274816 | 4 | 82 | 8 | Sec |
| 050 | 278528 | 4 | 80 | 8 | Sec |
| 060 | 268480 | 6 | 80 | 8 | Sec |
| 090 | 544496 | 10 | 157 | 15 | Sec |

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 270 •*** **Math Block with Input Register Used and Output in Bypass Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input register setup time | $T_{MISU}$ | 0.149 | | 0.176 | | ns |
| Input register hold time | $T_{MIHD}$ | 0.185 | | 0.218 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | 0.08 | | 0.094 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | –0.012 | | –0.014 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | –0.005 | | –0.005 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.088 | | 0.104 | | ns |
| Input register clock to output delay | $T_{MICQ}$ | | 2.52 | | 2.964 | ns |
| CDIN to output delay | $T_{MCDIN2Q}$ | | 1.951 | | 2.295 | ns |

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 271 •*** **Math Block with Input and Output in Bypass Mode**

| | | –1 | –Std | |
|---|---|---|---|---|
| **Parameter** | **Symbol** | **Max** | **Max** | **Unit** |
| Input to output delay | $T_{MIQ}$ | 2.568 | 3.022 | ns |
| CDIN to output delay | $T_{MCDIN2Q}$ | 1.951 | 2.295 | ns |

## 2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when $V_{DD}$ = 1.14 V, $V_{PPNVM}$ = $V_{PP}$ = 2.375 V.

***Table 272 •*** **eNVM Read Performance**

| | | Operating Temperature Range | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Description** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| $T_J$ | Junction temperature range | –55 °C to 125 °C | | –40 °C to 100 °C | | 0 °C to 85 °C | | °C |
| $F_{MAXREAD}$ | eNVM maximum read frequency | 25 | 25 | 25 | 25 | 25 | 25 | MHz |

The following table lists the eNVM page programming in worst-case conditions when $V_{DD}$ = 1.14 V, $V_{PPNVM}$ = $V_{PP}$ = 2.375 V.

***Table 273 •*** **eNVM Page Programming**

| | | Operating Temperature Range | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Description** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| $T_J$ | Junction temperature range | –55 °C to 125 °C | | –40 °C to 100 °C | | 0 °C to 85 °C | | °C |
| $T_{PAGEPGM}$ | eNVM page programming time | 40 | 40 | 40 | 40 | 40 | 40 | ms |

## 2.3.16 SRAM PUF

For more details on static random-access memory (SRAM) physical unclonable functions (PUF) services, see *AC434: Using SRAM PUF System Service in SmartFusion2 Application Note*.

The following table lists the SRAM PUF in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 274 •*** **SRAM PUF**

| | PUF Off | | PUF On | | |
|---|---|---|---|---|---|
| **Service** | **Typ** | **Max** | **Typ** | **Max** | **Unit** |
| Create activation code | 709.1 | 746.4 | 754.4 | 762.5 | ms |
| Delete activation code | 1329.3 | 1399.3 | 1414.1 | 1429.3 | ms |
| Create intrinsic keycode | 656.6 | 691.1 | 698.5 | 706.0 | ms |
| Create extrinsic keycode | 656.6 | 691.1 | 698.5 | 706.0 | ms |
| Get number of keys | 1.3 | 1.4 | 1.4 | 1.4 | ms |
| Export (Kc0, Kc1) | 998.0 | 1050.5 | 1061.7 | 1073.1 | ms |
| Export 2 keycodes | 2020.2 | 2126.5 | 2149.2 | 2172.3 | ms |
| Export 4 keycodes | 3065.7 | 3227.0 | 3261.3 | 3296.4 | ms |
| Export 8 keycodes | 5101.0 | 5369.5 | 5426.6 | 5485.0 | ms |
| Export 16 keycodes | 9212.1 | 9697.0 | 9800.1 | 9905.5 | ms |
| Import (Kc0, Kc1) | 39.7 | 41.8 | 42.2 | 42.7 | ms |
| Import 2 keycodes | 50.1 | 52.7 | 53.3 | 53.9 | ms |
| Import 4 keycodes | 60.6 | 63.8 | 64.5 | 65.2 | ms |
| Import 8 keycodes | 80.9 | 85.1 | 86.1 | 87.0 | ms |
| Import 16 keycodes | 123.8 | 130.4 | 131.7 | 133.2 | ms |
| Delete keycode | 552.5 | 581.6 | 587.8 | 594.1 | ms |
| Fetch key | 31.4 | 33.0 | 33.4 | 33.7 | ms |
| Fetch ecc key | 20.0 | 21.1 | 21.3 | 21.5 | ms |
| Get seed | 2.0 | 2.1 | 2.2 | 2.2 | ms |

The following table lists the IGLOO2 DEVRST_N to functional times in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 292 •*** **DEVRST_N to Functional Times for IGLOO2**

| | | | | Maximum Power-up to Functional Time for IGLOO2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **From** | **To** | **Description** | **005** | **010** | **025** | **050** | **060** | **090** | **150** |
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 114 | 116 | 113 | 113 | 115 | 115 | 114 |
| $T_{DEVRST2OUT}$ | DEVRST_N | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 314 | 353 | 314 | 307 | 343 | 341 | 341 |
| $T_{DEVRST2POR}$ | DEVRST_N | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 200 | 238 | 201 | 195 | 230 | 229 | 227 |
| $T_{DEVRST2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |

The following table lists the SerDes reference clock AC specifications in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 299 •*** **SerDes Reference Clock AC Specifications**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Reference clock frequency | $F_{REFCLK}$ | 100 | 160 | MHz |
| Reference clock rise time | $T_{RISE}$ | 0.6 | 4 | V/ns |
| Reference clock fall time | $T_{FALL}$ | 0.6 | 4 | V/ns |
| Reference clock duty cycle | $T_{CYC}$ | 40 | 60 | % |
| Reference clock mismatch | $M_{MREFCLK}$ | –300 | 300 | ppm |
| Reference spread spectrum clock | SSCref | 0 | 5000 | ppm |

***Table 300 •*** **HCSL Minimum and Maximum DC Input Levels (Applicable to SerDes REFCLK Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | |
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |
| **HCSL DC Input Voltage Specification** | | | | | |
| DC Input voltage | $V_I$ | 0 | | 2.625 | V |
| **HCSL Differential Voltage Specification** | | | | | |
| Input common mode voltage | $V_{ICM}$ | 0.05 | | 2.4 | V |
| Input differential voltage | $V_{IDIFF}$ | 100 | | 1100 | mV |

***Table 301 •*** **HCSL Minimum and Maximum AC Switching Speeds (Applicable to SerDes REFCLK Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **HCSL AC Specifications** | | | | | |
| Maximum data rate (for MSIO I/O bank) | $F_{MAX}$ | | | 350 | Mbps |
| **HCSL Impedance Specifications** | | | | | |
| Termination resistance | Rt | | 100 | | Ω |

## 2.3.31 SmartFusion2 Specifications

### 2.3.31.1 MSS Clock Frequency

The following table lists the maximum frequency for MSS main clock in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 302 •*** **Maximum Frequency for MSS Main Clock**

| Symbol | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| M3_CLK | Maximum frequency for the MSS main clock | 166 | 142 | MHz |

***Table 310 •*** **SPI Characteristics for All Devices *(continued)***

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| sp2 | SPI_[0\|1]_CLK minimum pulse width high | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.05 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.095 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.195 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.385 | | | µs | |
| sp3 | SPI_[0\|1]_CLK minimum pulse width low | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.05 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.095 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.195 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.385 | | | µs | |
| sp4 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS rise time (10%–90%)[1] | | 2.77 | | ns | I/O Configuration: LVCMOS 2.5 V - 8 mA<br>AC loading: 35 pF<br>test conditions: Typical voltage, 25 °C |
| sp5 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS fall time (10%–90%)[1] | | 2.906 | | ns | I/O Configuration: LVCMOS 2.5 V - 8 mA<br>AC loading: 35 pF<br>test conditions: Typical voltage, 25 °C |
| SPI master configuration (applicable for 005, 010, 025, and 050 devices) | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 8.0 | | | ns | |
| sp7m | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) – 2.5 | | | ns | |
| sp8m | SPI_[0\|1]_DI setup time[2] | 12 | | | ns | |
| sp9m | SPI_[0\|1]_DI hold time[2] | 2.5 | | | ns | |
| SPI slave configuration (applicable for 005, 010, 025, and 050 devices) | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 17.0 | | | ns | |
| sp7s | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) + 3.0 | | | ns | |
| sp8s | SPI_[0\|1]_DI setup time[2] | 2 | | | ns | |
| sp9s | SPI_[0\|1]_DI hold time[2] | 7 | | | ns | |