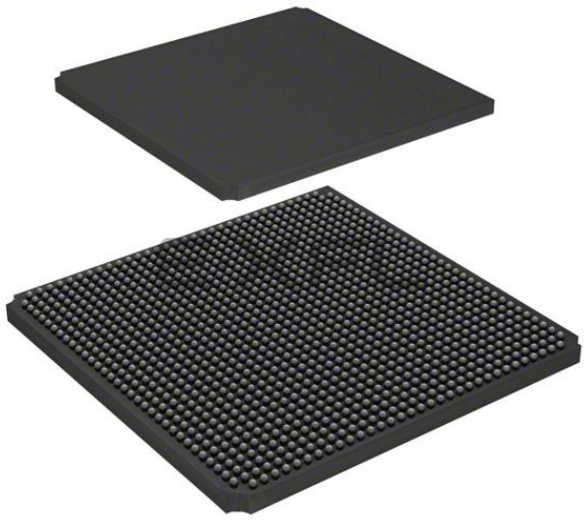
Microchip Technology - M2GL150T-1FC1152 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	146124
Total RAM Bits	5120000
Number of I/O	574
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl150t-1fc1152

2 IGLOO2 FPGA and SmartFusion2 SoC FPGA

Microsemi's mainstream SmartFusion®2 SoC and IGLOO®2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated math blocks, multiple embedded memory blocks, and high-performance SerDes communication interfaces on a single chip. Both families benefit from low-power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to 5 MBs of embedded RAM, up to 16 SerDes lanes, and up to four PCI Express Gen 2 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 devices integrate an entire low-power, real-time microcontroller subsystem (MSS) with a rich set of industry-standard peripherals including Ethernet, USB, and CAN, while IGLOO2 devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

2.1 Device Status

The following table shows the design security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

Table 1 • **IGLOO2 and SmartFusion2 Design Security Densities**

Design Security Device Densities	Status
005	Production
010, 010T	Production
025, 025T	Production
050, 050T	Production
060, 060T	Production
090, 090T	Production
150, 150T	Production

The following table shows the data security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

Table 2 • **IGLOO2 and SmartFusion2 Data Security Densities**

Data Security Device Densities	Status
005S	Production
010TS	Production
025TS	Production
050TS	Production
060TS	Production
090TS	Production
150TS	Production

where

θ_{JA} = Junction-to-air thermal resistance

θ_{JB} = Junction-to-board thermal resistance

θ_{JC} = Junction-to-case thermal resistance

T_J = Junction temperature

T_A = Ambient temperature

T_B = Board temperature (measured 1.0 mm away from the package edge)

T_C = Case temperature

P = Total power dissipated by the device

Table 9 • **Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices**

	Still Air	1.0 m/s	2.5 m/s			
Device		**θ_{JA}**		**θ_{JB}**	**θ_{JC}**	**Unit**
005						
FG484	19.36	15.81	14.63	9.74	5.27	°C/W
VF256	41.30	38.16	35.30	28.41	3.94	°C/W
VF400	20.19	16.94	15.41	8.86	4.95	°C/W
TQ144	42.80	36.80	34.50	37.20	10.80	°C/W
010						
FG484	18.22	14.83	13.62	8.83	4.92	°C/W
VF256	37.36	34.26	31.45	24.84	7.89	°C/W
VF400	19.40	15.75	14.22	8.11	4.22	°C/W
TQ144	38.60	32.60	30.30	31.80	8.60	°C/W
025						
FG484	17.03	13.66	12.45	7.66	4.18	°C/W
VF256	33.85	30.59	27.85	21.63	6.13	°C/W
VF400	18.36	14.89	13.36	7.12	3.41	°C/W
FCS325	29.17	24.87	23.12	14.44	2.31	°C/W
050						
FG484	15.29	12.19	10.99	6.27	3.24	°C/W
FG896	14.70	12.50	10.90	7.20	4.90	°C/W
VF400	17.53	14.17	12.63	6.32	2.81	°C/W
FCS325	27.38	23.18	21.41	12.47	1.59	°C/W
060						
FG484	15.40	12.06	10.85	6.14	3.15	°C/W
FG676	15.49	12.21	11.06	7.07	3.87	°C/W
VF400	17.45	14.01	12.47	6.22	2.69	°C/W
FCS325	27.03	22.91	21.25	12.33	1.54	°C/W
090						
FG484	14.64	11.37	10.16	5.43	2.77	°C/W
FG676	14.52	11.19	10.37	6.17	3.24	°C/W
FCS325	26.63	22.26	20.13	14.24	2.50	°C/W

Table 9 • **Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices *(continued)***

Device	Still Air θ_{JA}	1.0 m/s θ_{JA}	2.5 m/s θ_{JA}	θ_{JB}	θ_{JC}	Unit
150						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W
FCS536	15.01	12.06	10.76	3.69	1.55	°C/W
FCV484	16.21	13.11	11.84	6.73	0.10	°C/W

2.3.1.2.1 Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in the actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package with another.

The maximum power dissipation allowed is calculated using EQ4.

$$\text{Maximum power allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100 °C. EQ5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where:

θ_{JA} = 14.7 °C/W (taken from Table 9, page 10).

T_A = 85 °C

$$\text{Maximum power allowed} = \frac{100\ °C - 85\ °C}{14.7\ °C/W} = 1.088\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink may be attached to the top of the case, or the airflow inside the system must be increased.

2.3.1.2.2 Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from the junction to the board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

2.3.1.2.3 Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable to packages used with external heat sinks. Constant temperature is applied to the surface, which acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

2.3.1.3 ESD Performance

See *RT0001: Microsemi Corporation - SoC Products Reliability Report* for information about ESD.

Table 17 • **Timing Model Parameters *(continued)***

Index	Symbol	Description	–1	Unit	For More Information
F	T_{DP}	Propagation delay of an OR gate	0.179	ns	See Table 223, page 76
G	T_{DP}	Propagation delay of an LVDS transmitter	2.136	ns	See Table 169, page 57
H	T_{DP}	Propagation delay of a three-input XOR Gate	0.241	ns	See Table 223, page 76
I	T_{DP}	Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 16 mA on the MSIO bank	2.412	ns	See Table 46, page 27
J	T_{DP}	Propagation delay of a two-input NAND gate	0.179	ns	See Table 223, page 76
K	T_{DP}	Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 8 mA on the MSIO bank	2.309	ns	See Table 46, page 27
L	T_{CLKQ}	Clock-to-Q of the data register	0.108	ns	See Table 224, page 77
	T_{SUD}	Setup time of the data register	0.254	ns	See Table 224, page 77
M	T_{DP}	Propagation delay of a two-input AND gate	0.179	ns	See Table 223, page 76
N	T_{OCLKQ}	Clock-to-Q of the output data register	0.263	ns	See Table 220, page 69
	T_{OSUD}	Setup time of the output data register	0.19	ns	See Table 220, page 69
O	T_{DP}	Propagation delay of SSTL2, Class I transmitter on the MSIO bank	2.055	ns	See Table 114, page 45
P	T_{DP}	Propagation delay of LVCMOS 1.5 V transmitter, drive strength of 12 mA, fast slew on the DDRIO bank	3.316	ns	See Table 70, page 34

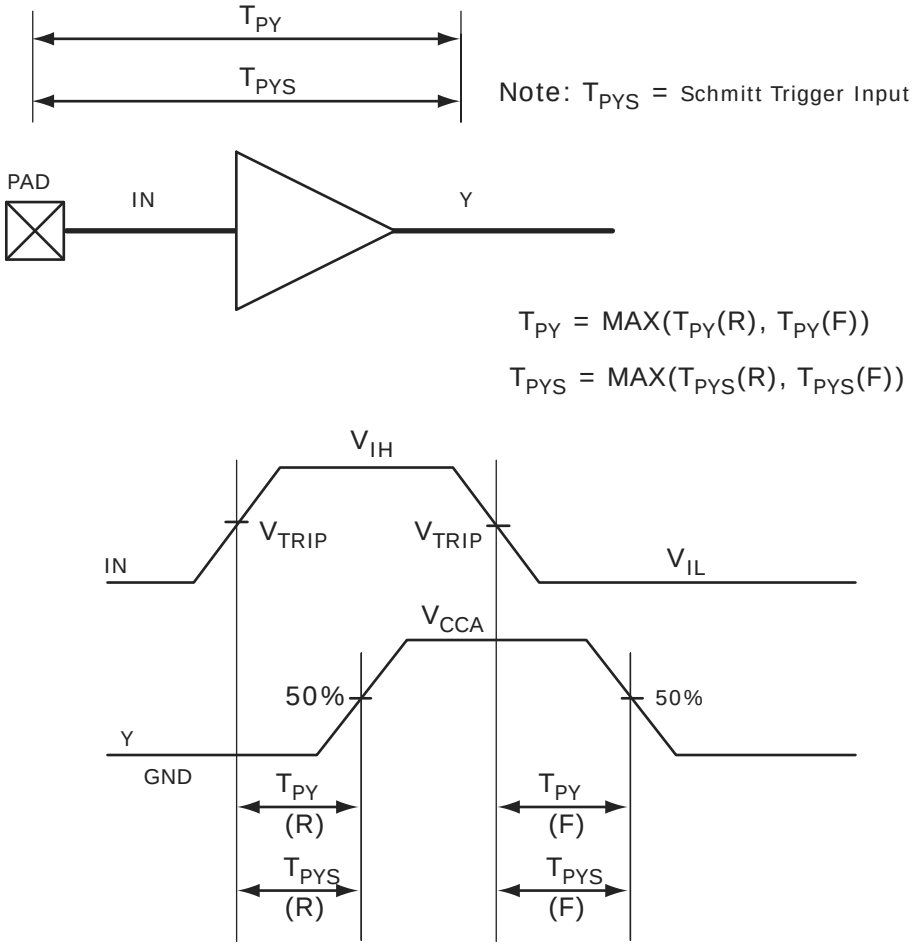
2.3.5 User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the I/Os section of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

2.3.5.1 Input Buffer and AC Loading

The following figure shows the input buffer and AC loading.

Figure 3 • **Input Buffer AC Loading**



2.3.5.2 Output Buffer and AC Loading

The following figure shows the output buffer and AC loading.

Figure 4 • **Output Buffer AC Loading**

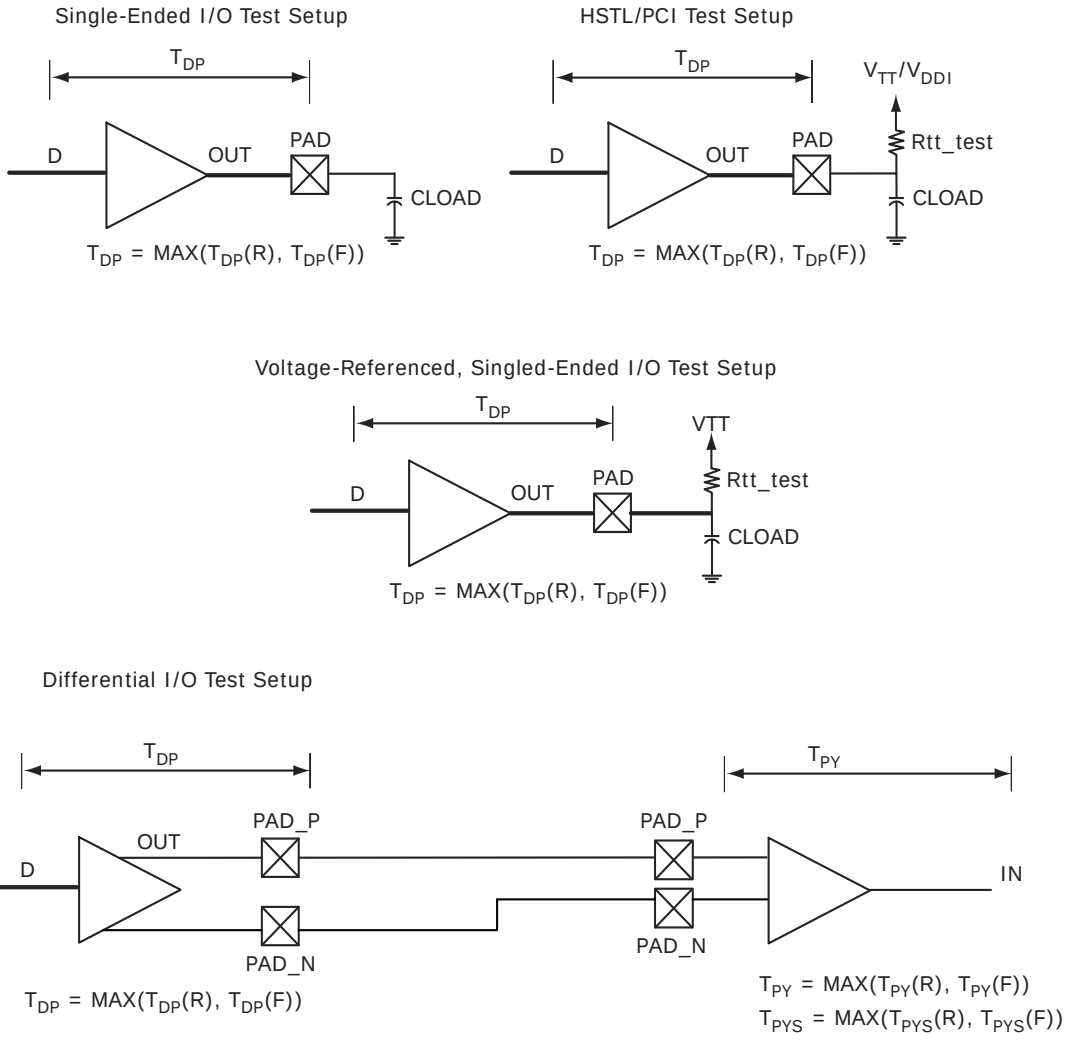


Table 48 • **LVCMOS 2.5 V Transmitter Characteristics for MSIOD Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	Unit
2 mA	Slow	2.206	2.596	2.678	3.15	2.64	3.106	4.935	5.805	4.74	5.576	ns
4 mA	Slow	1.835	2.159	2.242	2.637	2.256	2.654	5.413	6.368	5.15	6.059	ns
6 mA	Slow	1.709	2.01	2.132	2.508	2.167	2.549	5.813	6.838	5.499	6.469	ns
8 mA	Slow	1.63	1.918	1.958	2.303	2.012	2.367	6.226	7.324	5.816	6.842	ns
12 mA	Slow	1.648	1.939	1.86	2.187	1.921	2.259	6.519	7.669	6.027	7.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

2.3.5.8 1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 49 • **LVCMOS 1.8 V DC Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
LVCMOS 1.8 V DC Recommended Operating Conditions					
Supply voltage	V_{DDI}	1.710	1.8	1.89	V

Table 50 • **LVCMOS 1.8 V DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	V_{IH} (DC)	0.65 × V_{DDI}	1.89	V
DC input logic high (for MSIO I/O bank)	V_{IH} (DC)	0.65 × V_{DDI}	3.45	V
DC input logic low	V_{IL} (DC)	–0.3	0.35 × V_{DDI}	V
Input current high[1]	I_{IH} (DC)			–
Input current low[1]	I_{IL} (DC)			–

1. See Table 24, page 22.

Table 51 • **LVCMOS 1.8 V DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	V_{DDI} – 0.45		V
DC output logic low	V_{OL}		0.45	V

Table 52 • **LVCMOS 1.8 V Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)[1]	D_{MAX}	400	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D_{MAX}	295	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)[1]	D_{MAX}	400	Mbps	AC loading: 17 pF load, maximum drive/slew

1. Maximum Data Rate applies for Drive Strength 8 mA and above, All Slews.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V.

Table 180 • **B-LVDS AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.738	3.221	ns
100	2.735	3.218	ns

Table 181 • **B-LVDS AC Switching Characteristics for Receiver for MSIOD I/O Bank (Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.495	2.934	ns
100	2.495	2.935	ns

Table 182 • **B-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
2.258	2.656	2.343	2.756	2.329	2.74	2.12	2.494	2.123	2.497	ns

2.3.7.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum Input and Output Levels

Table 183 • **M-LVDS Recommended DC Operating Conditions**

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply voltage[1]	V_{DDI}	2.375	2.5	2.625	V

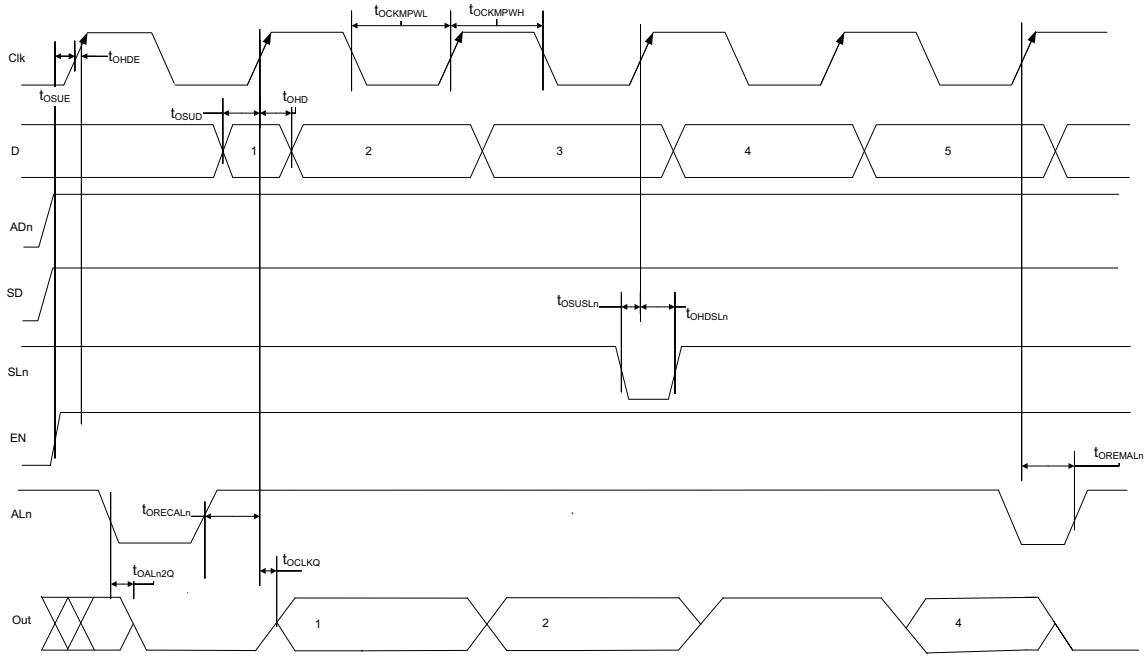
1. Only M-LVDS TYPE I is supported.

Table 184 • **M-LVDS DC Input Voltage Specification**

Parameter	**Symbol**	**Min**	**Max**	**Unit**
DC input voltage	V_I	0	2.925	V
Input current high[1]	I_{IH} (DC)			
Input current low[2]	I_{IL} (DC)			

1. See Table 24, page 22.

Figure 9 • **I/O Register Output Timing Diagram**



The following table lists the output/enable propagation delays in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 220 • **Output/Enable Data Register Propagation Delays**

Parameter	Symbol	Measuring Nodes (from, to)[1]	–1	–Std	Unit
Bypass delay of the output/enable register	T_{OBYP}	F, G or H, I	0.353	0.415	ns
Clock-to-Q of the output/enable register	T_{OCLKQ}	E, G or E, I	0.263	0.309	ns
Data setup time for the output/enable register	T_{OSUD}	A, E or J, E	0.19	0.223	ns
Data hold time for the output/enable register	T_{OHD}	A, E or J, E	0	0	ns
Enable setup time for the output/enable register	T_{OSUE}	B, E	0.419	0.493	ns
Enable hold time for the output/enable register	T_{OHE}	B, E	0	0	ns
Synchronous load setup time for the output/enable register	T_{OSUSL}	D, E	0.196	0.231	ns
Synchronous load hold time for the output/enable register	T_{OHSL}	D, E	0	0	ns
Asynchronous clear-to-q of the output/enable register (ADn = 1)	T_{OALN2Q}	C, G or C, I	0.505	0.594	ns
Asynchronous preset-to-q of the output/enable register (ADn = 0)		C, G or C, I	0.528	0.621	ns
Asynchronous load removal time for the output/enable register	$T_{OREMALN}$	C, E	0	0	ns
Asynchronous load recovery time for the output/enable register	$T_{ORECALN}$	C, E	0.034	0.04	ns
Asynchronous load minimum pulse width for the output/enable register	T_{OWALN}	C, C	0.304	0.357	ns
Clock minimum pulse width high for the output/enable register	$T_{OCKMPWH}$	E, E	0.075	0.088	ns
Clock minimum pulse width low for the output/enable register	$T_{OCKMPWL}$	E, E	0.159	0.187	ns

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

2.3.9.4 Output DDR Module

Figure 12 • Output DDR Module

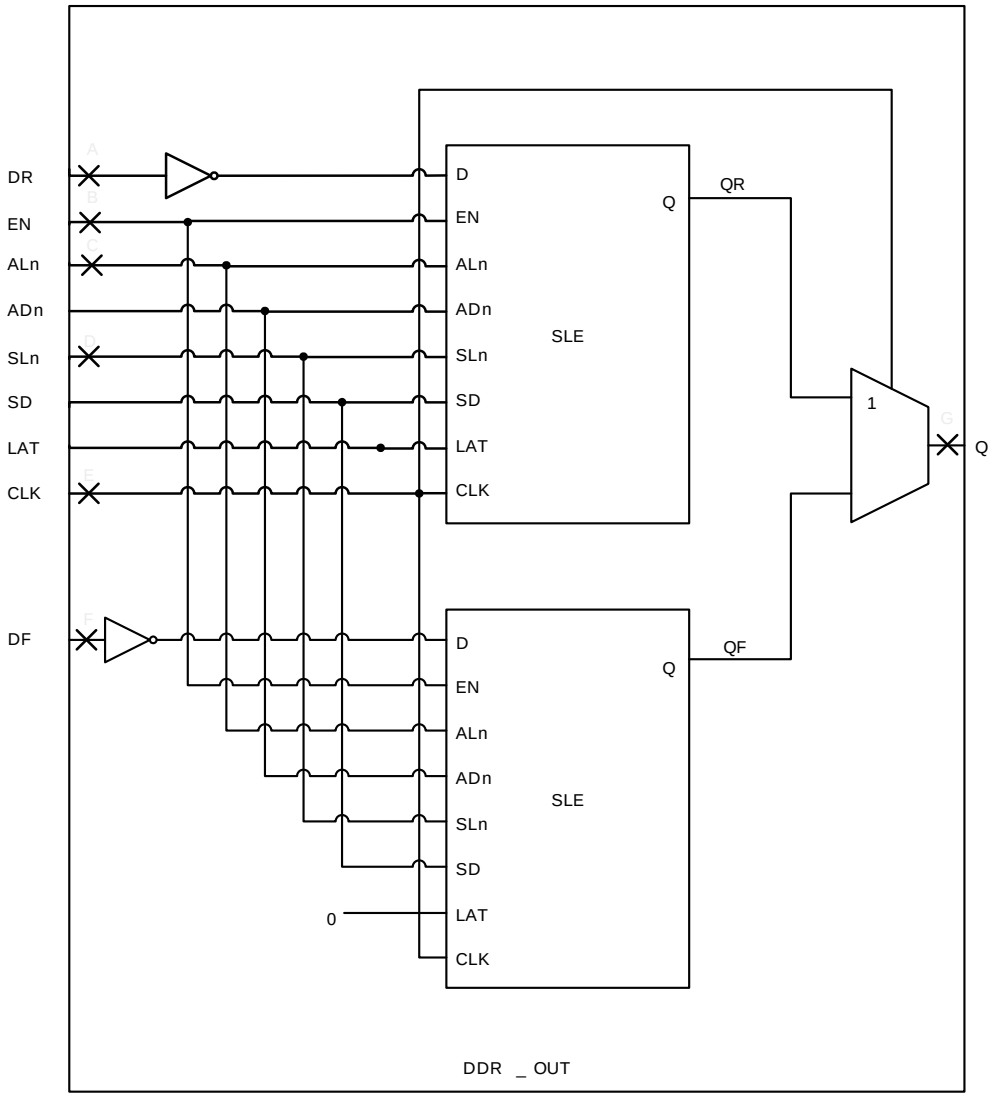


Table 222 • **Output DDR Propagation Delays *(continued)***

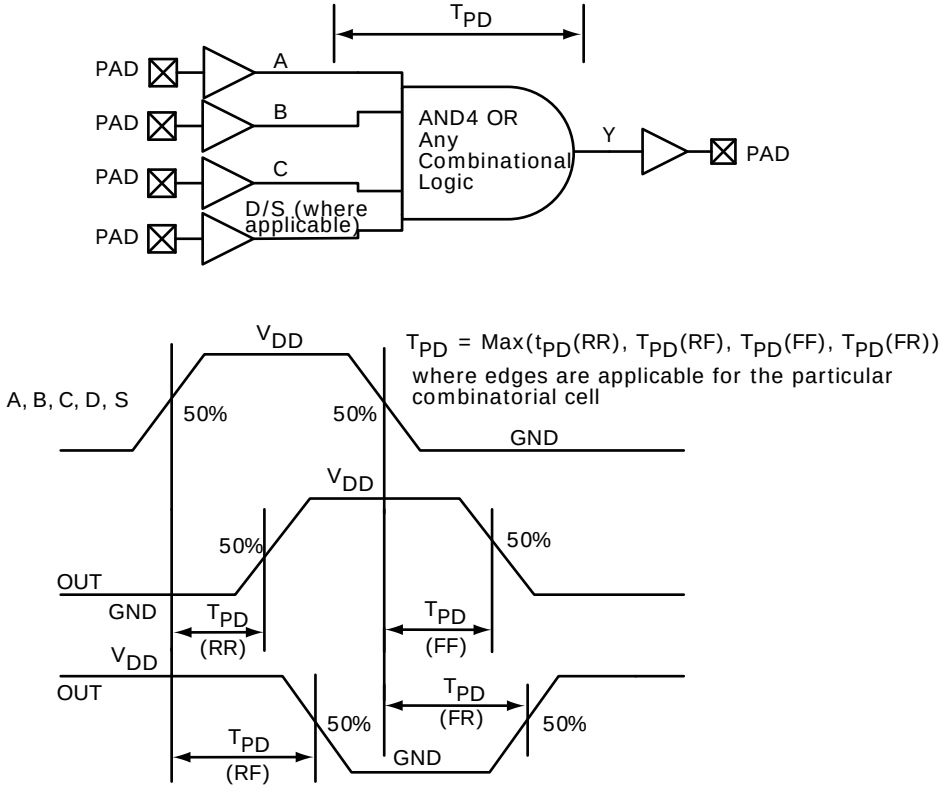
Symbol	Description	Measuring Nodes (from, to)	–1	–Std	Unit
$T_{DDROWAL}$	Asynchronous load minimum pulse width for output DDR	C, C	0.304	0.357	ns
$T_{DDROCKMPWH}$	Clock minimum pulse width high for the output DDR	E, E	0.075	0.088	ns
$T_{DDROCKMPWL}$	Clock minimum pulse width low for the output DDR	E, E	0.159	0.187	ns

2.3.10 Logic Element Specifications

2.3.10.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, see *SmartFusion2 and IGLOO2 Macro Library Guide*.

Figure 14 • **LUT-4**



2.3.11 Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for the positions of various global routing resources.

The following table lists the 150 device global resources in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 225 • **150 Device Global Resource**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input low delay for global clock	T_{RCKL}	0.83	0.911	0.831	0.913	ns
Input high delay for global clock	T_{RCKH}	1.457	1.588	1.715	1.869	ns
Maximum skew for global clock	T_{RCKSW}		0.131		0.154	ns

The following table lists the 090 device global resources in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 226 • **090 Device Global Resource**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input low delay for global clock	T_{RCKL}	0.835	0.888	0.833	0.886	ns
Input high delay for global clock	T_{RCKH}	1.405	1.489	1.654	1.752	ns
Maximum skew for global clock	T_{RCKSW}		0.084		0.098	ns

The following table lists the 050 device global resources in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 227 • **050 Device Global Resource**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input low delay for global clock	T_{RCKL}	0.827	0.897	0.826	0.896	ns
Input high delay for global clock	T_{RCKH}	1.419	1.53	1.671	1.8	ns
Maximum skew for global clock	T_{RCKSW}		0.111		0.129	ns

The following table lists the 025 device global resources in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 228 • **025 Device Global Resource**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input low delay for global clock	T_{RCKL}	0.747	0.799	0.745	0.797	ns
Input high delay for global clock	T_{RCKH}	1.294	1.378	1.522	1.621	ns
Maximum skew for global clock	T_{RCKSW}		0.084		0.099	ns

Table 248 • **2 Step IAP Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	137536	2	37	5	Sec
010	274816	4	76	11	Sec
025	274816	4	78	10	Sec
050	278528	3	85	9	Sec
060	268480	5	76	22	Sec
090	544496	10	152	43	Sec
150	544496	10	153	44	Sec

Table 249 • **2 Step IAP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	6	56	11	Sec
010	842688	11	100	21	Sec
025	1497408	19	113	32	Sec
050	2695168	32	136	48	Sec
060	2686464	43	137	70	Sec
090	4190208	68	236	115	Sec
150	6682768	109	286	162	Sec

Table 250 • **SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	302672	6	19	8	Sec
010	568784	10	26	14	Sec
025	1223504	21	39	29	Sec
050	2424832	39	60	50	Sec
060	2418896	44	65	54	Sec
090	3645968	66	90	79	Sec
150	6139184	108	140	128	Sec

Table 251 • **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	137536	3	42	4	Sec
010	274816	4	82	7	Sec
025	274816	4	82	8	Sec
050	278528	4	80	8	Sec
060	268480	6	80	8	Sec
090	544496	10	157	15	Sec

Table 262 • **SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	302672	6	41	8	Sec
010	568784	10	48	14	Sec
025	1223504	21	61	29	Sec
050	2424832	39	82	50	Sec
060	2418896	44	87	54	Sec
090	3645968	66	112	79	Sec
150	6139184	108	162	128	Sec

Table 263 • **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	137536	3	64	4	Sec
010	274816	4	104	7	Sec
025	274816	4	104	8	Sec
050	2,78,528	4	102	8	Sec
060	268480	6	102	8	Sec
090	544496	10	179	15	Sec
150	544496	10	180	15	Sec

Table 264 • **SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	9	83	11	Sec
010	842688	15	129	21	Sec
025	1497408	26	143	35	Sec
050	2695168	43	163	55	Sec
060	2686464	48	165	60	Sec
090	4190208	75	266	91	Sec
150	6682768	117	318	141	Sec

2.3.16 SRAM PUF

For more details on static random-access memory (SRAM) physical unclonable functions (PUF) services, see *AC434: Using SRAM PUF System Service in SmartFusion2 Application Note*.

The following table lists the SRAM PUF in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 274 • **SRAM PUF**

	PUF Off		PUF On		
Service	**Typ**	**Max**	**Typ**	**Max**	**Unit**
Create activation code	709.1	746.4	754.4	762.5	ms
Delete activation code	1329.3	1399.3	1414.1	1429.3	ms
Create intrinsic keycode	656.6	691.1	698.5	706.0	ms
Create extrinsic keycode	656.6	691.1	698.5	706.0	ms
Get number of keys	1.3	1.4	1.4	1.4	ms
Export (Kc0, Kc1)	998.0	1050.5	1061.7	1073.1	ms
Export 2 keycodes	2020.2	2126.5	2149.2	2172.3	ms
Export 4 keycodes	3065.7	3227.0	3261.3	3296.4	ms
Export 8 keycodes	5101.0	5369.5	5426.6	5485.0	ms
Export 16 keycodes	9212.1	9697.0	9800.1	9905.5	ms
Import (Kc0, Kc1)	39.7	41.8	42.2	42.7	ms
Import 2 keycodes	50.1	52.7	53.3	53.9	ms
Import 4 keycodes	60.6	63.8	64.5	65.2	ms
Import 8 keycodes	80.9	85.1	86.1	87.0	ms
Import 16 keycodes	123.8	130.4	131.7	133.2	ms
Delete keycode	552.5	581.6	587.8	594.1	ms
Fetch key	31.4	33.0	33.4	33.7	ms
Fetch ecc key	20.0	21.1	21.3	21.5	ms
Get seed	2.0	2.1	2.2	2.2	ms

2.3.21 Clock Conditioning Circuits (CCC)

The following table lists the CCC/PLL specifications in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 282 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**

Parameter	Min	Typ	Max	Unit	Conditions
Clock conditioning circuitry input frequency F_{IN_CCC}	1		200	MHz	All CCC
	0.032		200	MHz	32 kHz capable CCC
Clock conditioning circuitry output frequency F_{OUT_CCC}[1]	0.078		400	MHz	
PLL VCO frequency[2]	500		1000	MHz	
Delay increments in programmable delay blocks		75	100	ps	
Number of programmable values in each programmable delay block			64		
Acquisition time		70	100	µs	F_{IN} >= 1 MHz
		1	16	ms	F_{IN} = 32 kHz
Input duty cycle (reference clock)					Internal Feedback
	10		90	%	1 MHz ≤ F_{IN_CCC} ≤ 25 MHz
	25		75	%	25 MHz ≤ F_{IN_CCC}≤ 100 MHz
	35		65	%	100 MHz ≤ F_{IN_CCC} ≤ 150 MHz
	45		55	%	150 MHz ≤ F_{IN_CCC} ≤ 200 MHz
					External Feedback (CCC, FPGA, Off-chip)
	25		75	%	1 MHz ≤ F_{IN_CCC} ≤ 25 MHz
	35		65	%	25 MHz ≤ F_{IN_CCC} ≤ 35 MHz
	45		55	%	35 MHz ≤ F_{IN_CCC} ≤ 50 MHz
Output duty cycle	48		52	%	050 devices F_{OUT} ≤ 400 MHz
	48		52	%	005, 010, and 025 devices F_{OUT} < 350 MHz
	46		54	%	005, 010, and 025 devices 350 MHz ≤ F_{out} ≤ 400 MHz
	48		52	%	060 and 090 devices F_{OUT} ≤ 100 MHz
	44		52	%	060 and 090 devices 100 MHz ≤ F_{OUT} ≤ 400 MHz
	48		52	%	150 devices F_{OUT} ≤ 120 MHz
	45		52	%	150 devices 120 MHz ≤ F_{OUT} ≤ 400 MHz
Spread Spectrum Characteristics					
Modulation frequency range	25	35	50	k	
Modulation depth range	0		1.5	%	
Modulation depth control		0.5		%	

The following table lists the system controller characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 286 • **System Controller SPI Characteristics for All Devices**

Symbol	Description	Conditions	Min	Typ	Unit
sp1	SC_SPI_SCK minimum period		20		ns
sp2	SC_SPI_SCK minimum pulse width high		10		ns
sp3	SC_SPI_SCK minimum pulse width low		10		ns
sp4[1]	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%–90%) 1	I/O configuration: LVTTL 3.3 V– 20 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C		1.239	ns
sp5[1]	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%–90%) 1	I/O configuration: LVTTL 3.3 V– 20 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C		1.245	ns
sp6	Data from master (SC_SPI_SDO) setup time		160		ns
sp7	Data from master (SC_SPI_SDO) hold time		160		ns
sp8	SC_SPI_SDI setup time		20		ns
sp9	SC_SPI_SDI hold time		20		ns

1. For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx. Use the supported I/O Configurations for the System Controller SPI in the following table.

Table 287 • **Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)**

Voltage Supply	I/O Drive Configuration	Unit
3.3 V	20	mA
2.5 V	16	mA
1.8 V	12	mA
1.5 V	8	mA
1.2 V	4	mA

2.3.24 Power-up to Functional Times

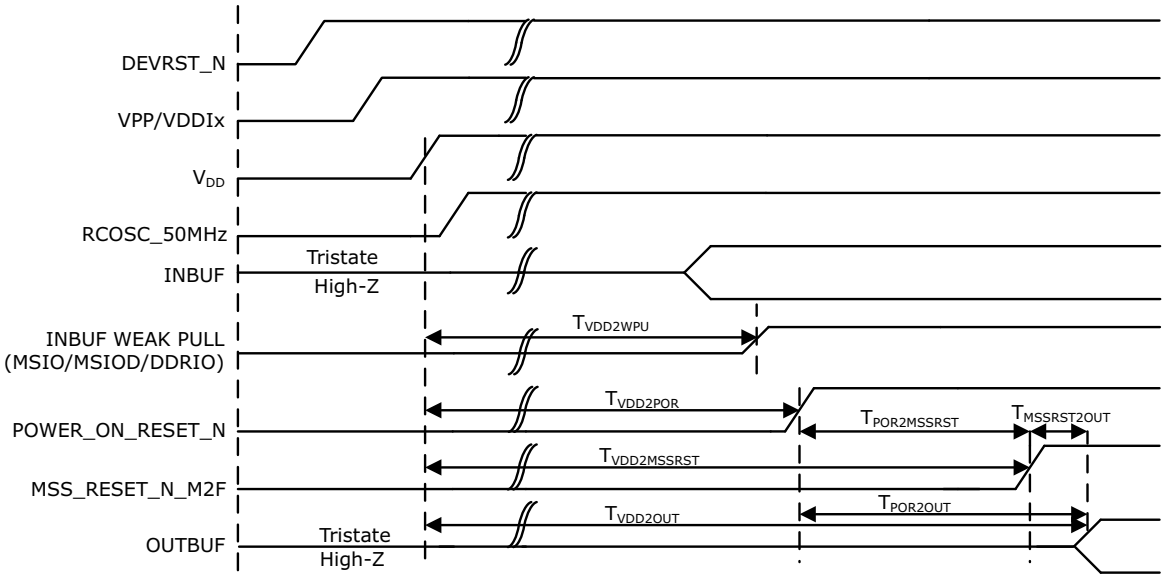
The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 288 • **Power-up to Functional Times for SmartFusion2**

				Maximum Power-up to Functional Time for SmartFusion2 (uS)						
Symbol	**From**	**To**	**Description**	**005**	**010**	**025**	**050**	**060**	**090**	**150**
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	647	500	531	483	474	524	647
$T_{POR2MSSRST}$	POWER_ON_RESET_N	MSS_RESET_N_M2F	Fabric to MSS	644	497	528	480	468	518	641
$T_{MSSRST2OUT}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.6	3.6	3.6	3.4	4.9	4.8	4.8
$T_{VDD2OUT}$	V_{DD}	Output available at I/O	V_{DD} at its minimum threshold level to output	3096	2975	3012	2959	2869	2992	3225
$T_{VDD2POR}$	V_{DD}	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	2476	2487	2496	2486	2406	2563	2602
$T_{VDD2MSSRST}$	V_{DD}	MSS_RESET_N_M2F	V_{DD} at its minimum threshold level to MSS	3093	2972	3008	2956	2864	2987	3220
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

Figure 17 • **Power-up to Functional Timing Diagram for SmartFusion2**



The following table lists the IGLOO2 power-up to functional times in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 289 • **Power-up to Functional Times for IGLOO2**

				Maximum Power-up to Functional Time for IGLOO2 (uS)						
Symbol	**From**	**To**	**Description**	**005**	**010**	**025**	**050**	**060**	**090**	**150**
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	114	114	113	114	114	114
$T_{VDD2OUT}$	V_{DD}	Output available at I/O	V_{DD} at its minimum threshold level to output	2587	2600	2607	2558	2591	2600	2699
$T_{VDD2POR}$	V_{DD}	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	2474	2486	2493	2445	2477	2486	2585
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide*.