**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 146124 |
| Total RAM Bits | 5120000 |
| Number of I/O | 293 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 536-LFBGA, CSPBGA |
| Supplier Device Package | 536-CSPBGA (16x16) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2gl150t-1fcsg536 |

***Table 17 •*** **Timing Model Parameters *(continued)***

| Index | Symbol | Description | –1 | Unit | For More Information |
|---|---|---|---|---|---|
| F | $T_{DP}$ | Propagation delay of an OR gate | 0.179 | ns | See Table 223, page 76 |
| G | $T_{DP}$ | Propagation delay of an LVDS transmitter | 2.136 | ns | See Table 169, page 57 |
| H | $T_{DP}$ | Propagation delay of a three-input XOR Gate | 0.241 | ns | See Table 223, page 76 |
| I | $T_{DP}$ | Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 16 mA on the MSIO bank | 2.412 | ns | See Table 46, page 27 |
| J | $T_{DP}$ | Propagation delay of a two-input NAND gate | 0.179 | ns | See Table 223, page 76 |
| K | $T_{DP}$ | Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 8 mA on the MSIO bank | 2.309 | ns | See Table 46, page 27 |
| L | $T_{CLKQ}$ | Clock-to-Q of the data register | 0.108 | ns | See Table 224, page 77 |
| | $T_{SUD}$ | Setup time of the data register | 0.254 | ns | See Table 224, page 77 |
| M | $T_{DP}$ | Propagation delay of a two-input AND gate | 0.179 | ns | See Table 223, page 76 |
| N | $T_{OCLKQ}$ | Clock-to-Q of the output data register | 0.263 | ns | See Table 220, page 69 |
| | $T_{OSUD}$ | Setup time of the output data register | 0.19 | ns | See Table 220, page 69 |
| O | $T_{DP}$ | Propagation delay of SSTL2, Class I transmitter on the MSIO bank | 2.055 | ns | See Table 114, page 45 |
| P | $T_{DP}$ | Propagation delay of LVCMOS 1.5 V transmitter, drive strength of 12 mA, fast slew on the DDRIO bank | 3.316 | ns | See Table 70, page 34 |

***Table 22 •*** **Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---|---|---|---|---|
| LPDDR | | | 200 | MHz |
| HSTL1.5 V | | | 200 | MHz |
| SSTL 2.5 V | 255 | 350 | 200 | MHz |
| SSTL 1.8 V | | | 334 | MHz |
| SSTL 1.5 V | | | 334 | MHz |

***Table 23 •*** **Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | Unit |
|---|---|---|---|
| LVPECL (input only) | 450 | | MHz |
| LVDS 3.3 V | 267.5 | | MHz |
| LVDS 2.5 V | 267.5 | 350 | MHz |
| RSDS | 260 | 350 | MHz |
| BLVDS | 250 | | MHz |
| MLVDS | 250 | | MHz |
| Mini-LVDS | 260 | 350 | MHz |

### 2.3.5.7 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs that are in compliance with the JEDEC specification JESD8-5A.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 38 •*** **LVCMOS 2.5 V DC Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

***Table 39 •*** **LVCMOS 2.5 V DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high (for MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 1.7 | 2.625 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 1.7 | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.7 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 40 •*** **LVCMOS 2.5 V DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$[1] | $V_{DDI}$ – 0.4 | – | V |
| DC output logic low | $V_{OL}$[2] | | 0.4 | V |

1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

***Table 41 •*** **LVCMOS 2.5 V AC Minimum and Maximum Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 400 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 410 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 420 | Mbps | AC loading: 17 pF load, maximum drive/slew |

***Table 42 •*** **LVCMOS 2.5 V AC Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | Rodt_cal | 75, 60, 50, 33, 25, 20 | Ω |

***Table 58 •*** **LVCMOS 1.8 V Transmitter Characteristics for MSIO I/O Bank**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 3.441 | 4.047 | 4.165 | 4.9 | 4.413 | 5.192 | 4.891 | 5.755 | 5.138 | 6.044 | ns |
| 4 mA | Slow | 3.218 | 3.786 | 3.642 | 4.284 | 3.941 | 4.636 | 5.665 | 6.665 | 5.568 | 6.551 | ns |
| 6 mA | Slow | 3.141 | 3.694 | 3.501 | 4.118 | 3.823 | 4.498 | 6.587 | 7.75 | 6.032 | 7.096 | ns |
| 8 mA | Slow | 3.165 | 3.723 | 3.319 | 3.904 | 3.654 | 4.298 | 6.898 | 8.115 | 6.216 | 7.313 | ns |
| 10 mA | Slow | 3.202 | 3.767 | 3.278 | 3.857 | 3.616 | 4.254 | 7.25 | 8.529 | 6.435 | 7.571 | ns |
| 12 mA | Slow | 3.277 | 3.855 | 3.175 | 3.736 | 3.519 | 4.139 | 7.392 | 8.697 | 6.538 | 7.692 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 59 •*** **LVCMOS 1.8 V Transmitter Characteristics for MSIOD I/O Bank**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 2.725 | 3.206 | 3.316 | 3.901 | 3.484 | 4.099 | 5.204 | 6.123 | 4.997 | 5.88 | ns |
| 4 mA | Slow | 2.242 | 2.638 | 2.777 | 3.267 | 2.947 | 3.466 | 5.729 | 6.74 | 5.448 | 6.41 | ns |
| 6 mA | Slow | 1.995 | 2.347 | 2.466 | 2.901 | 2.63 | 3.094 | 6.372 | 7.496 | 5.987 | 7.043 | ns |
| 8 mA | Slow | 2.001 | 2.354 | 2.44 | 2.87 | 2.6 | 3.058 | 6.633 | 7.804 | 6.193 | 7.286 | ns |
| 10 mA | Slow | 2.025 | 2.382 | 2.312 | 2.719 | 2.47 | 2.906 | 6.94 | 8.165 | 6.412 | 7.544 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### *2.3.5.9 1.5 V LVCMOS*

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 60 •*** **LVCMOS 1.5 V DC Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.425 | 1.5 | 1.575 | V |

***Table 61 •*** **LVCMOS 1.5 V DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high for (MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 1.575 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.35 × $V_{DDI}$ | V |
| Input current high[1] | $I_{IH}$ (DC) | | | – |
| Input current low[1] | $I_{IL}$ (DC | | | – |

1. See Table 24, page 22.

**Table 185 • M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

**Table 186 • M-LVDS Differential Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Differential output voltage swing (for MSIO I/O bank only) | $V_{OD}$ | 300 | 650 | mV |
| Output common mode voltage (for MSIO I/O bank only) | $V_{OCM}$ | 0.3 | 2.1 | V |
| Input common mode voltage | $V_{ICM}$ | 0.3 | 1.2 | V |
| Input differential voltage | $V_{ID}$ | 50 | 2400 | mV |

**Table 187 • M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | 500 | Mbps | AC loading: 2 pF / 100 Ω differential load |

**Table 188 • M-LVDS AC Impedance Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Termination resistance | $R_T$ | 50 | Ω |

**Table 189 • M-LVDS AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | Cross point | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V

**Table 190 • M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| On-Die Termination (ODT) | –1 | –Std | Unit |
| None | 2.738 | 3.221 | ns |
| 100 | 2.735 | 3.218 | ns |

***Figure 7 •*** **I/O Register Input Timing Diagram**

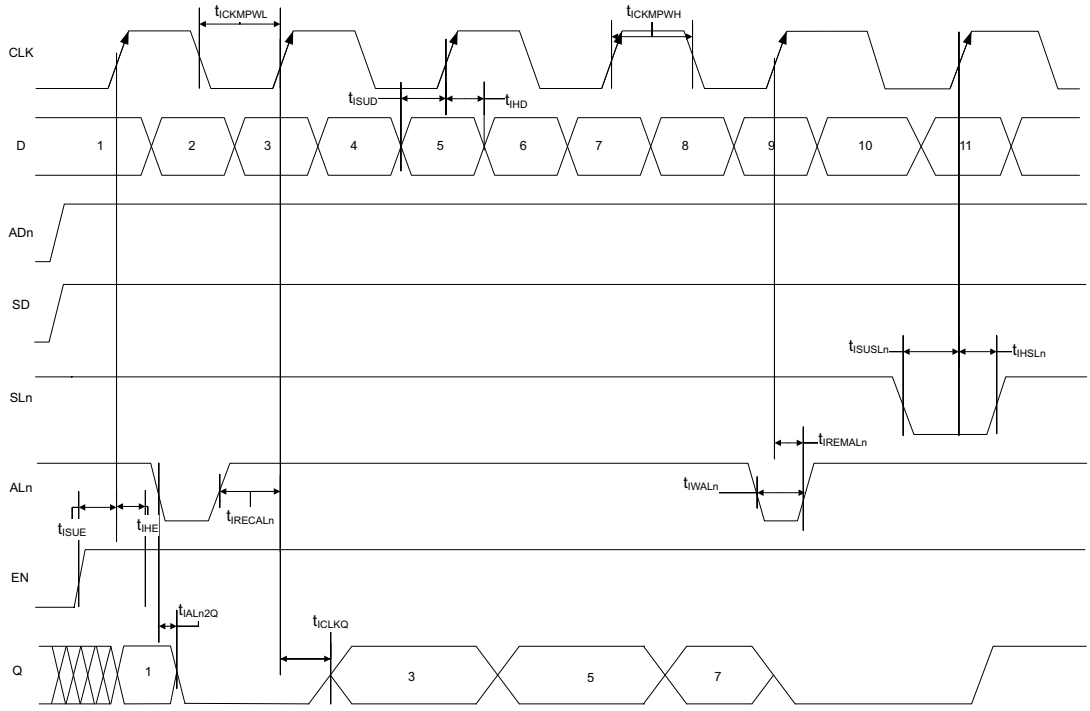
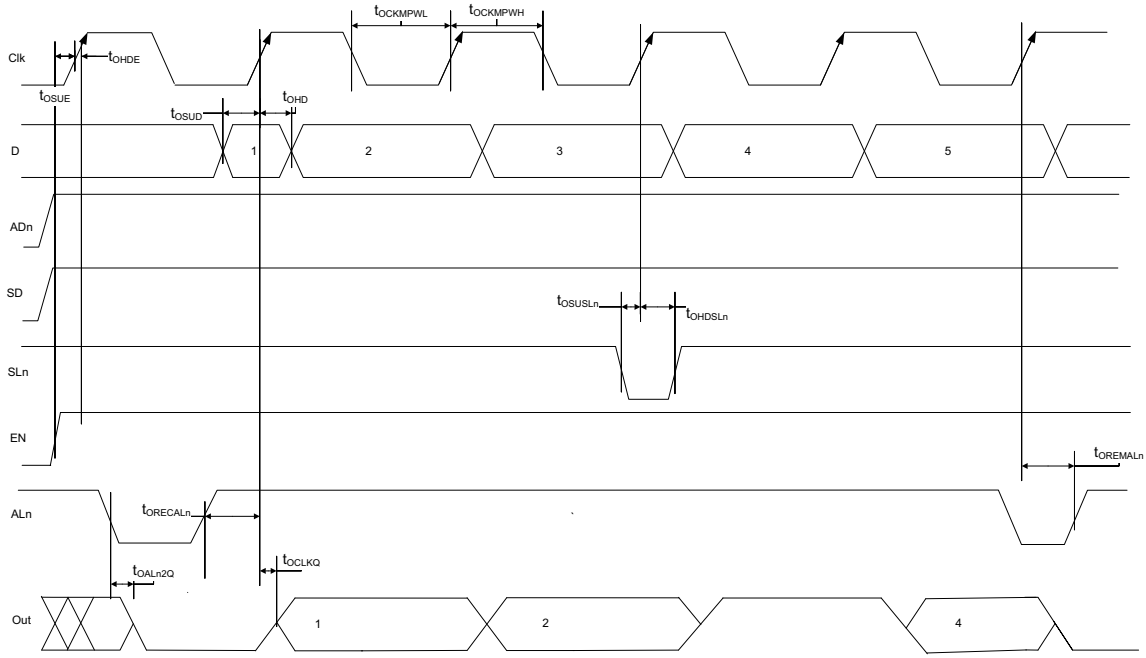


***Figure 9 •*** **I/O Register Output Timing Diagram**




The following table lists the output/enable propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 220 •*** **Output/Enable Data Register Propagation Delays**

| Parameter | Symbol | Measuring Nodes (from, to)[1] | –1 | –Std | Unit |
|---|---|---|---|---|---|
| Bypass delay of the output/enable register | $T_{OBYP}$ | F, G or H, I | 0.353 | 0.415 | ns |
| Clock-to-Q of the output/enable register | $T_{OCLKQ}$ | E, G or E, I | 0.263 | 0.309 | ns |
| Data setup time for the output/enable register | $T_{OSUD}$ | A, E or J, E | 0.19 | 0.223 | ns |
| Data hold time for the output/enable register | $T_{OHD}$ | A, E or J, E | 0 | 0 | ns |
| Enable setup time for the output/enable register | $T_{OSUE}$ | B, E | 0.419 | 0.493 | ns |
| Enable hold time for the output/enable register | $T_{OHE}$ | B, E | 0 | 0 | ns |
| Synchronous load setup time for the output/enable register | $T_{OSUSL}$ | D, E | 0.196 | 0.231 | ns |
| Synchronous load hold time for the output/enable register | $T_{OHSL}$ | D, E | 0 | 0 | ns |
| Asynchronous clear-to-q of the output/enable register (ADn = 1) | $T_{OALN2Q}$ | C, G or C, I | 0.505 | 0.594 | ns |
| Asynchronous preset-to-q of the output/enable register (ADn = 0) | | C, G or C, I | 0.528 | 0.621 | ns |
| Asynchronous load removal time for the output/enable register | $T_{OREMALN}$ | C, E | 0 | 0 | ns |
| Asynchronous load recovery time for the output/enable register | $T_{ORECALN}$ | C, E | 0.034 | 0.04 | ns |
| Asynchronous load minimum pulse width for the output/enable register | $T_{OWALN}$ | C, C | 0.304 | 0.357 | ns |
| Clock minimum pulse width high for the output/enable register | $T_{OCKMPWH}$ | E, E | 0.075 | 0.088 | ns |
| Clock minimum pulse width low for the output/enable register | $T_{OCKMPWL}$ | E, E | 0.159 | 0.187 | ns |

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

***Table 232 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Address setup time | $T_{ADDRSU}$ | 0.475 | | 0.559 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.336 | | 0.395 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.529 | | 1.799 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.485 | | 0.57 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.514 | | 1.781 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.415 | | 0.488 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 233 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 16K × 1 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 235 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.32 | | 0.377 | ns |
| Read access time without pipeline register | | | 2.269 | | 2.669 | ns |
| Access time with feed-through write timing | | | 1.51 | | 1.777 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.626 | | 0.737 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.322 | | 0.378 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.51 | | 1.777 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.53 | | 0.624 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.547 | | 1.82 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.454 | | 0.534 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

### 2.3.12.2 FPGA Fabric Micro SRAM (µSRAM)

The following table lists the µSRAM in 64 × 18 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 237 •*** **µSRAM (RAM64x18) in 64 × 18 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.266 | | 0.313 | ns |
| Read access time without pipeline register | | | 1.677 | | 1.973 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.856 | | 2.184 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.091 | | 0.107 | | ns |
| Read address hold time in asynchronous mode | | –0.778 | | –0.915 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.765 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.036 | | 2.396 | ns |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.023 | | –0.027 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.839 | | 0.987 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.115 | | 0.135 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.15 | | 0.177 | | ns |

***Table 239 •*** **µSRAM (RAM128x9) in 128 × 9 Mode *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.023 | | –0.027 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.835 | | 0.982 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.115 | | 0.135 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.15 | | 0.177 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.128 | | 0.15 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.026 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 128 × 8 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 240 •*** **µSRAM (RAM128x8) in 128 × 8 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.266 | | 0.313 | ns |
| Read access time without pipeline register | | | 1.677 | | 1.973 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.856 | | 2.184 | | ns |

## 2.3.14 Math Block Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC math block supports 18×18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently. The following table lists the math blocks with all registers used in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 268 •*** **Math Blocks with all Registers Used**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input, control register setup time | $T_{MISU}$ | 0.149 | | 0.176 | | ns |
| Input, control register hold time | $T_{MIHD}$ | 1.68 | | 1.976 | | ns |
| CDIN input setup time | $T_{MOCDINSU}$ | 0.185 | | 0.218 | | ns |
| CDIN input hold time | $T_{MOCDINHD}$ | 0.08 | | 0.094 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | –0.419 | | –0.493 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | 0.011 | | 0.013 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | 0 | | 0 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.088 | | 0.104 | | ns |
| Output register clock to out delay | $T_{MOCQ}$ | | 0.232 | | 0.273 | ns |
| CLK minimum period | $T_{MCLKMP}$ | 2.245 | | 2.641 | | ns |

The following table lists the math blocks with input bypassed and output registers used in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 269 •*** **Math Block with Input Bypassed and Output Registers Used**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Output register setup time | $T_{MOSU}$ | 2.294 | | 2.699 | | ns |
| Output register hold time | $T_{MOHD}$ | 1.68 | | 1.976 | | ns |
| CDIN input setup time | $T_{MOCDINSU}$ | 0.115 | | 0.136 | | ns |
| CDIN input hold time | $T_{MOCDINHD}$ | –0.444 | | –0.522 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | –0.419 | | –0.493 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | 0.011 | | 0.013 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | 0 | | 0 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.014 | | 0.017 | | ns |
| Output register clock to out delay | $T_{MOCQ}$ | | 0.232 | | 0.273 | ns |
| CLK minimum period | $T_{MCLKMP}$ | 2.179 | | 2.563 | | ns |

***Table 276 •*** **Cryptographic Block Characteristics *(continued)***

| Service | Conditions | Timing | Unit |
|---|---|---|---|
| SHA256 | 512 bits | 540 | kbps |
| | 1024 bits | 780 | kbps |
| | 2048 bits | 950 | kbps |
| | 24 kbits | 1140 | kbps |
| HMAC | 512 bytes | 820 | kbps |
| | 1024 bytes | 890 | kbps |
| | 2048 bytes | 930 | kbps |
| | 24 kbytes | 980 | kbps |
| KeyTree | | 1.8 | ms |
| Challenge-response | PUF = OFF | 25 | ms |
| | PUF = ON | 7 | ms |
| ECC point multiplication | | 590 | ms |
| ECC point addition | | 8 | ms |

1. Using cypher block chaining (CBC) mode.

## 2.3.19 Crystal Oscillator

The following table describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

***Table 277 •*** **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 20 | | MHz | |
| Accuracy | ACCXTAL | | | 0.0047 | % | 005, 010, 025, 050, 060, and 090 devices |
| | | | | 0.0058 | % | 150 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 200 | 300 | ps | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 200 | 300 | ps | 010, 025, 050, and 060 devices |
| | | | 250 | 410 | ps | 150 devices |
| | | | 250 | 550 | ps | 005 and 090 devices |
| Operating current | IDYNXTAL | | 1.5 | | mA | 010, 050, and 060 devices |
| | | | 1.65 | | mA | 005, 025, 090, and 150 devices |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |

1. The minimum output clock frequency is limited by the PLL. For more information, see *UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide*.
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance is limited by the CCC output frequency.

The following table lists the CCC/PLL jitter specifications in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 283 •*** **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications**

| **CCC Output Maximum Peak-to-Peak Period Jitter $F_{OUT\_CCC}$** | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Conditions/Package Combinations** | | | | | **Unit** |
| **10 FG484, 050 FG896/FG484/FCS325 Packages[1]** | SSO = 0 | 0 < SSO <= 2 | SSO <= 4 | SSO <= 8 | SSO <= 16 | |
| 20 MHz to 100 MHz | Max(110, ± 1% x ($1/F_{OUT\_CCC}$)) | Max(150, ± 1% x ($1/F_{OUT\_CCC}$)) | | | | ps |
| 100 MHz to 400 MHz | Max(120, ± 1% x ($1/F_{OUT\_CCC}$)) | Max(150, ± 1% x ($1/F_{OUT\_CCC}$)) | | | Max(170, ± 1% x ($1/F_{OUT\_CCC}$)) | ps |
| **025 FG484/FCS325 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 74 MHz | ± 1% x ($1/F_{OUT\_CCC}$)) | | | | | ps |
| 74 MHz to 400 MHz | 210 | | | | | ps |
| **005 FG484 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 53 MHz | ± 1% x ($1/F_{OUT\_CCC}$)) | | | | | ps |
| 53 MHz to 400 MHz | 270 | | | | | ps |
| **090 FG676 and FC325 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 100 MHz | ± 1% x ($1/F_{OUT\_CCC}$)) | | | | | ps |
| 100 MHz to 400 MHz | 150 | | | | | ps |
| **060 FG676 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 100 MHz | ± 1% x ($1/F_{OUT\_CCC}$) | | | | | ps |
| 100 MHz to 400 MHz | 150 | | | | | |
| **150 FC1152 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 100 MHz | ± 1% x ($1/F_{OUT\_CCC}$)) | | | | | ps |
| 100 MHz to 400 MHz | 120 | | | | | ps |

1. SSO data is based on LVCMOS 2.5 V MSIO and/or MSIOD bank I/Os.

## 2.3.22 JTAG

***Table 284 •*** **JTAG 1532 for 005, 010, 025, and 050 Devices**

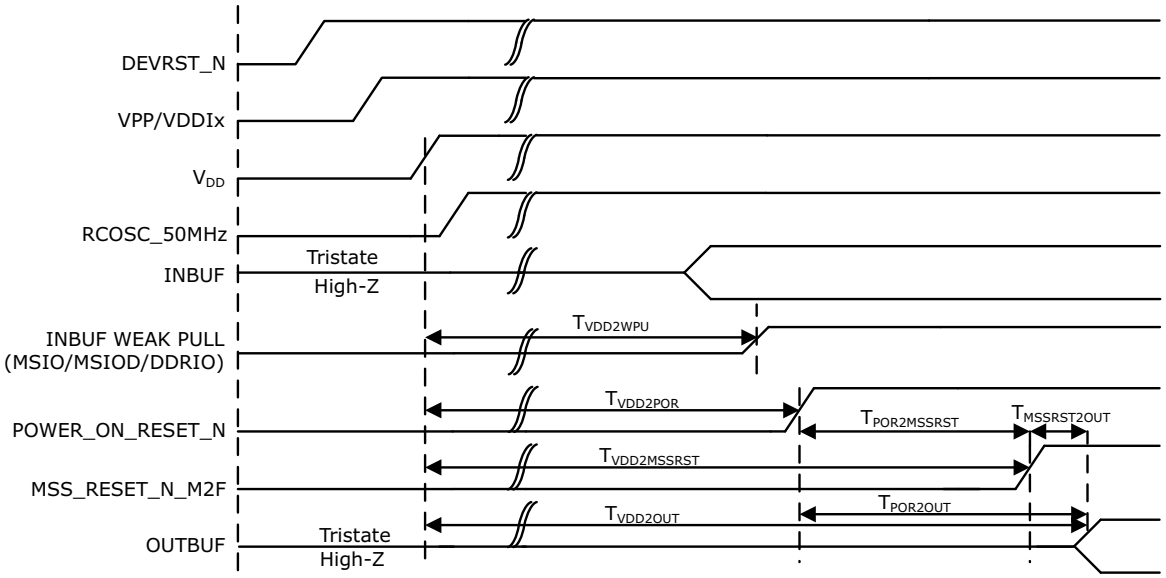
| | | 005 | | 010 | | 025 | | 050 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | |
| Clock to Q (data out) | $T_{TCK2Q}$ | 7.47 | 8.79 | 7.73 | 9.09 | 7.75 | 9.12 | 7.89 | 9.28 | ns |
| Reset to Q (data out) | $T_{RSTB2Q}$ | 7.65 | 9 | 6.43 | 7.56 | 6.13 | 7.21 | 7.40 | 8.70 | ns |
| Test data input setup time | $T_{DISU}$ | –1.05 | –0.89 | –0.69 | –0.59 | –0.67 | –0.57 | –0.30 | –0.25 | ns |
| Test data input hold time | $T_{DIHD}$ | 2.38 | 2.8 | 2.38 | 2.8 | 2.42 | 2.85 | 2.09 | 2.45 | ns |
| Test mode select setup time | $T_{TMSSU}$ | –0.73 | –0.62 | –1.03 | –1.21 | –1.1 | –0.94 | 0.28 | 0.33 | ns |
| Test mode select hold time | $T_{TMDHD}$ | 1.36 | 1.6 | 1.43 | 1.68 | 1.93 | 2.27 | 0.16 | 0.19 | ns |
| ResetB removal time | $T_{TRSTREM}$ | –0.77 | –0.65 | –1.08 | –0.92 | –1.33 | –1.13 | –0.45 | –0.38 | ns |
| ResetB recovery time | $T_{TRSTREC}$ | –0.76 | –0.65 | –1.07 | –0.91 | –1.34 | –1.14 | –0.45 | –0.38 | ns |
| TCK maximum frequency | $F_{TCKMAX}$ | 25 | 21.25 | 25 | 21.25 | 25 | 21.25 | 25.00 | 21.25 | MHz |

***Table 285 •*** **JTAG 1532 for 060, 090, and 150 Devices**

| | | 060 | | 090 | | 150 | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| Clock to Q (data out) | $T_{TCK2Q}$ | 8.38 | 9.86 | 8.96 | 10.54 | 8.66 | 10.19 | ns |
| Reset to Q (data out) | $T_{RSTB2Q}$ | 8.54 | 10.04 | 7.75 | 9.12 | 8.79 | 10.34 | ns |
| Test data input setup time | $T_{DISU}$ | –1.18 | –1 | –1.31 | –1.11 | –0.96 | –0.82 | ns |
| Test data input hold time | $T_{DIHD}$ | 2.52 | 2.97 | 2.68 | 3.15 | 2.57 | 3.02 | ns |
| Test mode select setup time | $T_{TMSSU}$ | –0.97 | –0.83 | –1.02 | –0.87 | –0.53 | –0.45 | ns |
| Test mode select hold time | $T_{TMDHD}$ | 1.7 | 2 | 1.67 | 1.96 | 1.02 | 1.2 | ns |
| ResetB removal time | $T_{TRSTREM}$ | –1.21 | –1.03 | –0.76 | –0.65 | –1.03 | –0.88 | ns |
| ResetB recovery time | $T_{TRSTREC}$ | –1.21 | –1.03 | –0.77 | –0.65 | –1.03 | –0.88 | ns |
| TCK maximum frequency | $F_{TCKMAX}$ | 25 | 21.25 | 25 | 21.25 | 25 | 21.25 | MHz |

## 2.3.23 System Controller SPI Characteristics

***Figure 17 •*** **Power-up to Functional Timing Diagram for SmartFusion2**




The following table lists the IGLOO2 power-up to functional times in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 289 •*** **Power-up to Functional Times for IGLOO2**

| | | | | Maximum Power-up to Functional Time for IGLOO2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **From** | **To** | **Description** | **005** | **010** | **025** | **050** | **060** | **090** | **150** |
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 114 | 114 | 114 | 113 | 114 | 114 | 114 |
| $T_{VDD2OUT}$ | $V_{DD}$ | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 2587 | 2600 | 2607 | 2558 | 2591 | 2600 | 2699 |
| $T_{VDD2POR}$ | $V_{DD}$ | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 2474 | 2486 | 2493 | 2445 | 2477 | 2486 | 2585 |
| $T_{VDD2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2500 | 2487 | 2509 | 2475 | 2507 | 2519 | 2617 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2504 | 2491 | 2510 | 2478 | 2517 | 2525 | 2620 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2479 | 2468 | 2493 | 2458 | 2486 | 2499 | 2595 |

**Note:** For more information about power-up times, see *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide*.

The following table lists the SerDes reference clock AC specifications in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 299 •*** **SerDes Reference Clock AC Specifications**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Reference clock frequency | $F_{REFCLK}$ | 100 | 160 | MHz |
| Reference clock rise time | $T_{RISE}$ | 0.6 | 4 | V/ns |
| Reference clock fall time | $T_{FALL}$ | 0.6 | 4 | V/ns |
| Reference clock duty cycle | $T_{CYC}$ | 40 | 60 | % |
| Reference clock mismatch | $M_{MREFCLK}$ | –300 | 300 | ppm |
| Reference spread spectrum clock | SSCref | 0 | 5000 | ppm |

***Table 300 •*** **HCSL Minimum and Maximum DC Input Levels (Applicable to SerDes REFCLK Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | |
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |
| **HCSL DC Input Voltage Specification** | | | | | |
| DC Input voltage | $V_I$ | 0 | | 2.625 | V |
| **HCSL Differential Voltage Specification** | | | | | |
| Input common mode voltage | $V_{ICM}$ | 0.05 | | 2.4 | V |
| Input differential voltage | $V_{IDIFF}$ | 100 | | 1100 | mV |

***Table 301 •*** **HCSL Minimum and Maximum AC Switching Speeds (Applicable to SerDes REFCLK Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **HCSL AC Specifications** | | | | | |
| Maximum data rate (for MSIO I/O bank) | $F_{MAX}$ | | | 350 | Mbps |
| **HCSL Impedance Specifications** | | | | | |
| Termination resistance | Rt | | 100 | | Ω |

# 2.3.31 SmartFusion2 Specifications

## 2.3.31.1 MSS Clock Frequency

The following table lists the maximum frequency for MSS main clock in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 302 •*** **Maximum Frequency for MSS Main Clock**

| Symbol | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| M3_CLK | Maximum frequency for the MSS main clock | 166 | 142 | MHz |

### 2.3.31.3 Serial Peripheral Interface (SPI) Characteristics

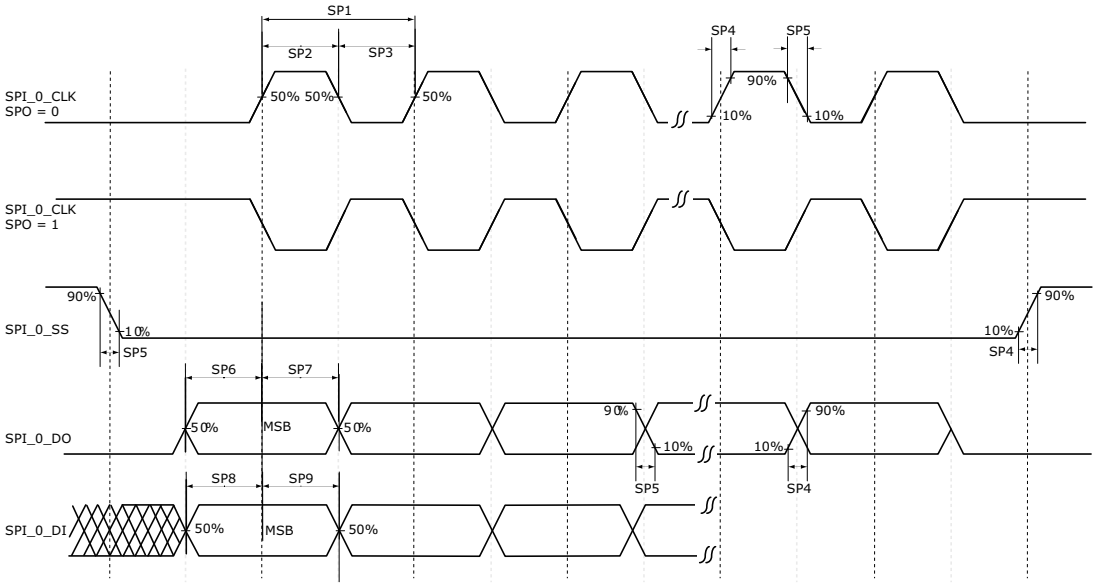
This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, see Figure 22, page 128.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V

***Table 305 •*** **SPI Characteristics for All Devices**

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| SPIFMAX | Maximum operating frequency of SPI interface | | | 20 | MHz | |
| sp1 | SPI_[0\|1]_CLK minimum period | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 12 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 48.2 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.1 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.19 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.39 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.77 | | | µs | |
| sp2 | SPI_[0\|1]_CLK minimum pulse width high | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.05 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.095 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.195 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.385 | | | µs | |
| sp3 | SPI_[0\|1]_CLK minimum pulse width low | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.05 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.095 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.195 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.385 | | | µs | |
| sp4 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS rise time (10%–90%)[1] | | 2.77 | | ns | I/O Configuration: LVCMOS 2.5 V– 8 mA<br>AC loading: 35 pF<br>Test conditions: Typical voltage, 25 °C |

***Figure 22 •*** **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**




## 2.3.32 CAN Controller Characteristics

The following table lists the CAN controller characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 306 •*** **CAN Controller Characteristics**

| Parameter | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| FCANREFCLK[1] | Internally sourced CAN reference clock frequency | 160 | 136 | MHz |
| BAUDCANMAX | Maximum CAN performance baud rate | 1 | 1 | Mbps |
| BAUDCANMIN | Minimum CAN performance baud rate | 0.05 | 0.05 | Mbps |

1. PCLK to CAN controller must be a multiple of 8 MHz.

## 2.3.33 USB Characteristics

The following table lists the USB characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 307 •*** **USB Characteristics**

| Parameter | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| FUSBREFCLK | Internally sourced USB reference clock frequency | 166 | 142 | MHz |
| TUSBCLK | USB clock period | 16.66 | 16.66 | ns |
| TUSBPD | Clock to USB data propagation delay | 9.0 | 9.0 | ns |
| TUSBSU | Setup time for USB data | 6.0 | 6.0 | ns |
| TUSBHD | Hold time for USB data | 0 | 0 | ns |

## 2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 308 •*** **MMUART Characteristics**

| Parameter | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| FMMUART_REF_CLK | Internally sourced MMUART reference clock frequency. | 166 | 142 | MHz |
| BAUDMMUARTTx | Maximum transmit baud rate | 10.375 | 8.875 | Mbps |
| BAUDMMUARTRx | Maximum receive baud rate | 10.375 | 8.875 | Mbps |

## 2.3.35 IGLOO2 Specifications

### 2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 309 •*** **Maximum Frequency for HPMS Main Clock**

| Symbol | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| HPMS_CLK | Maximum frequency for the HPMS main clock | 166 | 142 | MHz |

### 2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, see Figure 23, page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 310 •*** **SPI Characteristics for All Devices**

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| SPIFMAX | Maximum operating frequency of SPI interface | | | 20 | MHz | |
| sp1 | SPI_[0\|1]_CLK minimum period | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 12 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 48.2 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.1 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.19 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.39 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.77 | | | µs | |