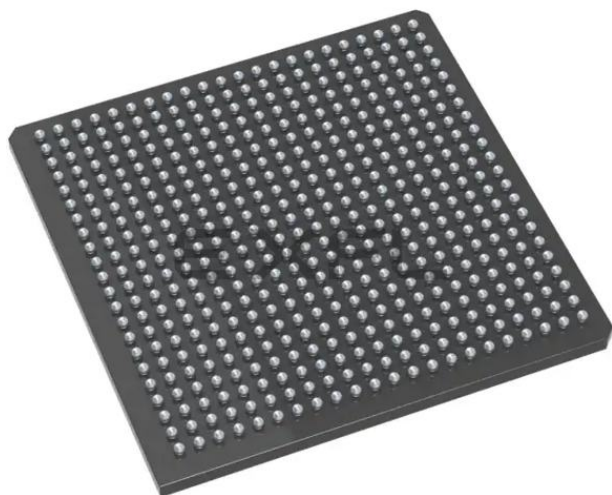




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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                                                     |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Active                                                                                                                                                              |
| Number of LABs/CLBs            | -                                                                                                                                                                   |
| Number of Logic Elements/Cells | 146124                                                                                                                                                              |
| Total RAM Bits                 | 5120000                                                                                                                                                             |
| Number of I/O                  | 248                                                                                                                                                                 |
| Number of Gates                | -                                                                                                                                                                   |
| Voltage - Supply               | 1.14V ~ 2.625V                                                                                                                                                      |
| Mounting Type                  | Surface Mount                                                                                                                                                       |
| Operating Temperature          | 0°C ~ 85°C (TJ)                                                                                                                                                     |
| Package / Case                 | 484-BFBGA                                                                                                                                                           |
| Supplier Device Package        | 484-FBGA (19x19)                                                                                                                                                    |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/microchip-technology/m2gl150t-1fcv484">https://www.e-xfl.com/product-detail/microchip-technology/m2gl150t-1fcv484</a> |



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- Added [Table 244](#), page 94 and [Table 256](#), page 99 (SAR 73971).
- Updated the [SerDes Electrical and Timing AC and DC Characteristics](#), page 121 (SAR 71171).
- Added the [DEVRST\\_N Characteristics](#), page 116 (SAR 64100, 72103).
- Added [Table 298](#), page 122 (SAR 71897).
- Updated [Table 25](#), page 22, [Table 26](#), page 23, and [Table 27](#), page 23 (SAR 74570).
- Added 060 devices in [Table 277](#), page 107, [Table 278](#), page 108, and [Table 279](#), page 108 (SAR 57898).
- Updated duty cycle parameter of crystal in [Table 280](#), page 109 and [Table 281](#), page 109 (SAR 57898).
- Added 32 KHz mode PLL acquisition time in [Table 282](#), page 110 (SAR 68281).
- Updated [Table 293](#), page 119 for 060 devices (SAR 57828).
- Updated [Table 297](#), page 122 for CID value (SAR 70878).

## 1.4 Revision 8.0

The following is a summary of the changes in revision 8.0 of this document.

- Updated [Table 11](#), page 12 (SAR 69218).
- Updated [Table 12](#), page 13 (SAR 69218).
- Updated [Table 283](#), page 111 (SAR 69000).

## 1.5 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Updated [Table 1](#), page 4 (SAR 68620).

## 1.6 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- Updated [Table 5](#), page 7 (SAR 65949).
- Updated [Table 9](#), page 10 (SAR 62995).
- Updated [Table 123](#), page 47 and [Table 133](#), page 49 (SAR 67210).
- Added [Embedded NVM \(eNVM\) Characteristics](#), page 104 (SAR 52509).
- Updated [Table 277](#), page 107 (SAR 64855).
- Updated [Table 282](#), page 110 (SAR 65958 and SAR 56666).
- Added [DDR Memory Interface Characteristics](#), page 120 (SAR 66223).
- Added [SFP Transceiver Characteristics](#), page 120 (SAR 63105).
- Updated [Table 302](#), page 123 and [Table 309](#), page 129 (SAR 66314).

## 1.7 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Updated [Table 1](#), page 4.
- Updated [Table 4](#), page 6 for  $T_J$  symbol information.
- Updated [Table 5](#), page 7 (SAR 63109).
- Updated [Table 9](#), page 10.
- Updated [Table 282](#), page 110 (SAR 62012).
- Added [Table 290](#), page 116 (SAR 64100).
- Added [Table 306](#), page 128, [Table 307](#), page 128 (SAR 50424).

## 1.8 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document.

- Updated [Table 1](#), page 4. Changed the Status of 090 devices to "Production" (SAR 62750).
- Updated [Figure 10](#), page 70. Removed inverter bubble from DDR\_IN latch (SAR 61418).
- Updated [SerDes Electrical and Timing AC and DC Characteristics](#), page 121 (SAR 62836).

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIO I/O bank at  $V_{OH}/V_{OL}$  Level.

**Table 26 • I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank**

| $V_{DDI}$ Domain      | R(WEAK PULL-UP) at $V_{OH}$ ( $\Omega$ ) |       | R(WEAK PULL-DOWN) at $V_{OL}$ ( $\Omega$ ) |       |
|-----------------------|------------------------------------------|-------|--------------------------------------------|-------|
|                       | Min                                      | Max   | Min                                        | Max   |
| 3.3 V                 | 9.9K                                     | 17.1K | 9.98K                                      | 17.5K |
| 2.5 V <sup>1, 2</sup> | 10K                                      | 17.6K | 10.1K                                      | 18.4K |
| 1.8 V <sup>1, 2</sup> | 10.4K                                    | 19.1K | 10.4K                                      | 20.4K |
| 1.5 V <sup>1, 2</sup> | 10.7K                                    | 20.4K | 10.8K                                      | 22.2K |
| 1.2 V <sup>1, 2</sup> | 11.3K                                    | 23.2K | 11.5K                                      | 26.7K |

1.  $R(\text{WEAK PULL-DOWN}) = (V_{OLspec})/I(\text{WEAK PULL-DOWN MAX})$ .
2.  $R(\text{WEAK PULL-UP}) = (V_{DDImax} - V_{OHspec})/I(\text{WEAK PULL-UP MIN})$ .

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIOD I/O bank at  $V_{OH}/V_{OL}$  Level.

**Table 27 • I/O Weak Pull-up/Pull-down Resistances for MSIOD I/O Bank**

| $V_{DDI}$ Domain      | R(WEAK PULL-UP) at $V_{OH}$ ( $\Omega$ ) |       | R(WEAK PULL-DOWN) at $V_{OL}$ ( $\Omega$ ) |       |
|-----------------------|------------------------------------------|-------|--------------------------------------------|-------|
|                       | Min                                      | Max   | Min                                        | Max   |
| 2.5 V <sup>1, 2</sup> | 9.6K                                     | 16.6K | 9.5K                                       | 16.4K |
| 1.8 V <sup>1, 2</sup> | 9.7K                                     | 17.3K | 9.7K                                       | 17.1K |
| 1.5 V <sup>1, 2</sup> | 9.9K                                     | 18K   | 9.8K                                       | 17.6K |
| 1.2 V <sup>1, 2</sup> | 10.3K                                    | 19.6K | 10K                                        | 19.1K |

1.  $R(\text{WEAK PULL-DOWN}) = (V_{OLspec})/I(\text{WEAK PULL-DOWN MAX})$ .
2.  $R(\text{WEAK PULL-UP}) = (V_{DDImax} - V_{OHspec})/I(\text{WEAK PULL-UP MIN})$ .

The following table lists the hysteresis voltage value for schmitt trigger mode input buffers.

**Table 28 • Schmitt Trigger Input Hysteresis**

| Input Buffer Configuration        | Hysteresis Value (Typical, unless otherwise noted) |
|-----------------------------------|----------------------------------------------------|
| 3.3 V LVTTTL/LVCMOS/<br>PCI/PCI-X | $0.05 \times V_{DDI}$ (worst-case)                 |
| 2.5 V LVCMOS                      | $0.05 \times V_{DDI}$ (worst-case)                 |
| 1.8 V LVCMOS                      | $0.1 \times V_{DDI}$ (worst-case)                  |
| 1.5 V LVCMOS                      | 60 mV                                              |
| 1.2 V LVCMOS                      | 20 mV                                              |

**Table 118 • DDR1/SSTL2 Class II Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

|              | $T_{DP}$ |       | $T_{ZL}$ |       | $T_{ZH}$ |       | $T_{HZ}$ |       | $T_{LZ}$ |       | Unit |
|--------------|----------|-------|----------|-------|----------|-------|----------|-------|----------|-------|------|
|              | -1       | -Std  | -1       | -Std  | -1       | -Std  | -1       | -Std  | -1       | -Std  |      |
| Single-ended | 2.29     | 2.693 | 1.988    | 2.338 | 1.978    | 2.326 | 1.989    | 2.34  | 1.979    | 2.328 | ns   |
| Differential | 2.418    | 2.846 | 2.304    | 2.711 | 2.297    | 2.702 | 2.131    | 2.506 | 2.124    | 2.499 | ns   |

**2.3.6.4 Stub-Series Terminated Logic 1.8 V (SSTL18)**

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification****Table 119 • SSTL18 DC Recommended DC Operating Conditions**

| Parameter               | Symbol    | Min   | Typ   | Max   | Unit |
|-------------------------|-----------|-------|-------|-------|------|
| Supply voltage          | $V_{DDI}$ | 1.71  | 1.8   | 1.89  | V    |
| Termination voltage     | $V_{TT}$  | 0.838 | 0.900 | 0.964 | V    |
| Input reference voltage | $V_{REF}$ | 0.838 | 0.900 | 0.964 | V    |

**Table 120 • SSTL18 DC Input Voltage Specification**

| Parameter                       | Symbol        | Min               | Max               | Unit |
|---------------------------------|---------------|-------------------|-------------------|------|
| DC input logic high             | $V_{IH}$ (DC) | $V_{REF} + 0.125$ | 1.89              | V    |
| DC input logic low              | $V_{IL}$ (DC) | -0.3              | $V_{REF} - 0.125$ | V    |
| Input current high <sup>1</sup> | $I_{IH}$ (DC) |                   |                   |      |
| Input current low <sup>1</sup>  | $I_{IL}$ (DC) |                   |                   |      |

1. See Table 24, page 22.

**Table 121 • SSTL18 DC Output Voltage Specification**

| Parameter                                              | Symbol               | Min              | Max              | Unit |
|--------------------------------------------------------|----------------------|------------------|------------------|------|
| <b>SSTL18 Class I (DDR2 Reduced Drive)</b>             |                      |                  |                  |      |
| DC output logic high                                   | $V_{OH}$             | $V_{TT} + 0.603$ |                  | V    |
| DC output logic low                                    | $V_{OL}$             |                  | $V_{TT} - 0.603$ | V    |
| Output minimum source DC current (DDRIO I/O bank only) | $I_{OH}$ at $V_{OH}$ | 6.5              |                  | mA   |
| Output minimum sink current (DDRIO I/O bank only)      | $I_{OL}$ at $V_{OL}$ | -6.5             |                  | mA   |
| <b>SSTL18 Class II (DDR2 Full Drive)<sup>1</sup></b>   |                      |                  |                  |      |
| DC output logic high                                   | $V_{OH}$             | $V_{TT} + 0.603$ |                  | V    |
| DC output logic low                                    | $V_{OL}$             |                  | $V_{TT} - 0.603$ | V    |
| Output minimum source DC current (DDRIO I/O bank only) | $I_{OH}$ at $V_{OH}$ | 13.4             |                  | mA   |
| Output minimum sink current (DDRIO I/O bank only)      | $I_{OL}$ at $V_{OL}$ | -13.4            |                  | mA   |

1. To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.



**Table 144 • LPDDR AC Differential Voltage Specifications (for DDRIO I/O Bank Only)**

| Parameter                           | Symbol     | Min                  | Max                  | Unit |
|-------------------------------------|------------|----------------------|----------------------|------|
| AC input differential voltage       | $V_{DIFF}$ | $0.6 \times V_{DDI}$ |                      | V    |
| AC differential cross point voltage | $V_x$      | $0.4 \times V_{DDI}$ | $0.6 \times V_{DDI}$ | V    |

**Table 145 • LPDDR AC Specifications (for DDRIO I/O Bank Only)**

| Parameter         | Symbol    | Max | Unit | Conditions                           |
|-------------------|-----------|-----|------|--------------------------------------|
| Maximum data rate | $D_{MAX}$ | 400 | Mbps | AC loading: per JEDEC specifications |

**Table 146 • LPDDR AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

| Parameter                                    | Symbol    | Typ         | Unit     | Conditions                        |
|----------------------------------------------|-----------|-------------|----------|-----------------------------------|
| Supported output driver calibrated impedance | $R_{REF}$ | 20, 42      | $\Omega$ | Reference resistor = 150 $\Omega$ |
| Effective impedance value (ODT)              | $R_{TT}$  | 50, 70, 150 | $\Omega$ | Reference resistor = 150 $\Omega$ |

**Table 147 • LPDDR AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

| Parameter                                                                        | Symbol         | Typ | Unit     |
|----------------------------------------------------------------------------------|----------------|-----|----------|
| Measuring/trip point for data path                                               | $V_{TRIP}$     | 0.9 | V        |
| Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )         | $R_{ENT}$      | 2K  | $\Omega$ |
| Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ ) | $C_{ENT}$      | 5   | pF       |
| Reference resistance for data test path for LPDDR ( $T_{DP}$ )                   | $R_{TT\_TEST}$ | 50  | $\Omega$ |
| Capacitive loading for data path ( $T_{DP}$ )                                    | $C_{LOAD}$     | 5   | $\Omega$ |

**AC Switching Characteristics**

Worst-case commercial conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ , worst-case  $V_{DDI}$ .

**Table 148 • LPDDR Receiver Characteristics for DDRIO I/O Bank with Fixed Codes**

|                          |      | $T_{PY}$ |       | Unit |
|--------------------------|------|----------|-------|------|
| On-Die Termination (ODT) |      | -1       | -Std  |      |
| Pseudo differential      | None | 1.568    | 1.845 | ns   |
| True differential        | None | 1.588    | 1.869 | ns   |

**Table 149 • LPDDR Reduced Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

|              | $T_{DP}$ |       | $T_{ENZL}$ |       | $T_{ENZH}$ |       | $T_{ENHZ}$ |       | $T_{ENLZ}$ |       | Unit |
|--------------|----------|-------|------------|-------|------------|-------|------------|-------|------------|-------|------|
|              | -1       | -Std  | -1         | -Std  | -1         | -Std  | -1         | -Std  | -1         | -Std  |      |
| Single-ended | 2.383    | 2.804 | 2.23       | 2.623 | 2.229      | 2.622 | 2.202      | 2.591 | 2.201      | 2.59  | ns   |
| Differential | 2.396    | 2.819 | 2.764      | 3.252 | 2.764      | 3.252 | 2.255      | 2.653 | 2.255      | 2.653 | ns   |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 16K × 1 in worst commercial-case conditions when  $T_J = 85\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 235 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1**

| Parameter                                                              | Symbol          | –1     |       | –Std   |       | Unit |
|------------------------------------------------------------------------|-----------------|--------|-------|--------|-------|------|
|                                                                        |                 | Min    | Max   | Min    | Max   |      |
| Clock period                                                           | $T_{CY}$        | 2.5    |       | 2.941  |       | ns   |
| Clock minimum pulse width high                                         | $T_{CLKMPWH}$   | 1.125  |       | 1.323  |       | ns   |
| Clock minimum pulse width low                                          | $T_{CLKMPWL}$   | 1.125  |       | 1.323  |       | ns   |
| Pipelined clock period                                                 | $T_{PLCY}$      | 2.5    |       | 2.941  |       | ns   |
| Pipelined clock minimum pulse width high                               | $T_{PLCLKMPWH}$ | 1.125  |       | 1.323  |       | ns   |
| Pipelined clock minimum pulse width low                                | $T_{PLCLKMPWL}$ | 1.125  |       | 1.323  |       | ns   |
| Read access time with pipeline register                                |                 |        | 0.32  |        | 0.377 | ns   |
| Read access time without pipeline register                             | $T_{CLK2Q}$     |        | 2.269 |        | 2.669 | ns   |
| Access time with feed-through write timing                             |                 |        | 1.51  |        | 1.777 | ns   |
| Address setup time                                                     | $T_{ADDRSU}$    | 0.626  |       | 0.737  |       | ns   |
| Address hold time                                                      | $T_{ADDRHD}$    | 0.274  |       | 0.322  |       | ns   |
| Data setup time                                                        | $T_{DSU}$       | 0.322  |       | 0.378  |       | ns   |
| Data hold time                                                         | $T_{DHD}$       | 0.082  |       | 0.096  |       | ns   |
| Block select setup time                                                | $T_{BLKSU}$     | 0.207  |       | 0.244  |       | ns   |
| Block select hold time                                                 | $T_{BLKHD}$     | 0.216  |       | 0.254  |       | ns   |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$     |        | 1.51  |        | 1.777 | ns   |
| Block select minimum pulse width                                       | $T_{BLKMPW}$    | 0.186  |       | 0.219  |       | ns   |
| Read enable setup time                                                 | $T_{RDESU}$     | 0.53   |       | 0.624  |       | ns   |
| Read enable hold time                                                  | $T_{RDEHD}$     | 0.071  |       | 0.083  |       | ns   |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)                | $T_{RDPLESU}$   | 0.248  |       | 0.291  |       | ns   |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)                 | $T_{RDPLEHD}$   | 0.102  |       | 0.12   |       | ns   |
| Asynchronous reset to output propagation delay                         | $T_{R2Q}$       |        | 1.547 |        | 1.82  | ns   |
| Asynchronous reset removal time                                        | $T_{RSTREM}$    | 0.506  |       | 0.595  |       | ns   |
| Asynchronous reset recovery time                                       | $T_{RSTREC}$    | 0.004  |       | 0.005  |       | ns   |
| Asynchronous reset minimum pulse width                                 | $T_{RSTMPW}$    | 0.301  |       | 0.354  |       | ns   |
| Pipelined register asynchronous reset removal time                     | $T_{PLRSTREM}$  | –0.279 |       | –0.328 |       | ns   |
| Pipelined register asynchronous reset recovery time                    | $T_{PLRSTREC}$  | 0.327  |       | 0.385  |       | ns   |
| Pipelined register asynchronous reset minimum pulse width              | $T_{PLRSTMPW}$  | 0.282  |       | 0.332  |       | ns   |
| Synchronous reset setup time                                           | $T_{SRSTSU}$    | 0.226  |       | 0.265  |       | ns   |
| Synchronous reset hold time                                            | $T_{SRSTHD}$    | 0.036  |       | 0.043  |       | ns   |
| Write enable setup time                                                | $T_{WESU}$      | 0.454  |       | 0.534  |       | ns   |
| Write enable hold time                                                 | $T_{WEHD}$      | 0.048  |       | 0.057  |       | ns   |
| Maximum frequency                                                      | $F_{MAX}$       |        | 400   |        | 340   | MHz  |

### 2.3.12.2 FPGA Fabric Micro SRAM ( $\mu$ SRAM)

The following table lists the  $\mu$ SRAM in  $64 \times 18$  mode in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 237 •  $\mu$ SRAM (RAM64x18) in  $64 \times 18$  Mode**

| Parameter                                                                             | Symbol          | –1     |     | –Std   |     | Unit |
|---------------------------------------------------------------------------------------|-----------------|--------|-----|--------|-----|------|
|                                                                                       |                 | Min    | Max | Min    | Max |      |
| Read clock period                                                                     | $T_{CY}$        | 4      |     | 4      |     | ns   |
| Read clock minimum pulse width high                                                   | $T_{CLKMPWH}$   | 1.8    |     | 1.8    |     | ns   |
| Read clock minimum pulse width low                                                    | $T_{CLKMPWL}$   | 1.8    |     | 1.8    |     | ns   |
| Read pipeline clock period                                                            | $T_{PLCY}$      | 4      |     | 4      |     | ns   |
| Read pipeline clock minimum pulse width high                                          | $T_{PLCLKMPWH}$ | 1.8    |     | 1.8    |     | ns   |
| Read pipeline clock minimum pulse width low                                           | $T_{PLCLKMPWL}$ | 1.8    |     | 1.8    |     | ns   |
| Read access time with pipeline register                                               | $T_{CLK2Q}$     | 0.266  |     | 0.313  |     | ns   |
| Read access time without pipeline register                                            |                 | 1.677  |     | 1.973  |     | ns   |
| Read address setup time in synchronous mode                                           | $T_{ADDRSU}$    | 0.301  |     | 0.354  |     | ns   |
| Read address setup time in asynchronous mode                                          |                 | 1.856  |     | 2.184  |     | ns   |
| Read address hold time in synchronous mode                                            | $T_{ADDRHD}$    | 0.091  |     | 0.107  |     | ns   |
| Read address hold time in asynchronous mode                                           |                 | –0.778 |     | –0.915 |     | ns   |
| Read enable setup time                                                                | $T_{RDENSU}$    | 0.278  |     | 0.327  |     | ns   |
| Read enable hold time                                                                 | $T_{RDENHD}$    | 0.057  |     | 0.067  |     | ns   |
| Read block select setup time                                                          | $T_{BLKSU}$     | 1.839  |     | 2.163  |     | ns   |
| Read block select hold time                                                           | $T_{BLKHD}$     | –0.65  |     | –0.765 |     | ns   |
| Read block select to out disable time (when pipelined register is disabled)           | $T_{BLK2Q}$     | 2.036  |     | 2.396  |     | ns   |
| Read asynchronous reset removal time (pipelined clock)                                | $T_{RSTREM}$    | –0.023 |     | –0.027 |     | ns   |
| Read asynchronous reset removal time (non-pipelined clock)                            |                 | 0.046  |     | 0.054  |     | ns   |
| Read asynchronous reset recovery time (pipelined clock)                               | $T_{RSTREC}$    | 0.507  |     | 0.597  |     | ns   |
| Read asynchronous reset recovery time (non-pipelined clock)                           |                 | 0.236  |     | 0.278  |     | ns   |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$       | 0.839  |     | 0.987  |     | ns   |
| Read synchronous reset setup time                                                     | $T_{SRSTSU}$    | 0.271  |     | 0.319  |     | ns   |
| Read synchronous reset hold time                                                      | $T_{SRSTHD}$    | 0.061  |     | 0.071  |     | ns   |
| Write clock period                                                                    | $T_{CCY}$       | 4      |     | 4      |     | ns   |
| Write clock minimum pulse width high                                                  | $T_{CCLKMPWH}$  | 1.8    |     | 1.8    |     | ns   |
| Write clock minimum pulse width low                                                   | $T_{CCLKMPWL}$  | 1.8    |     | 1.8    |     | ns   |
| Write block setup time                                                                | $T_{BLKCSU}$    | 0.404  |     | 0.476  |     | ns   |
| Write block hold time                                                                 | $T_{BLKCHD}$    | 0.007  |     | 0.008  |     | ns   |
| Write input data setup time                                                           | $T_{DINCSU}$    | 0.115  |     | 0.135  |     | ns   |
| Write input data hold time                                                            | $T_{DINCHD}$    | 0.15   |     | 0.177  |     | ns   |

**Table 237 •  $\mu$ SRAM (RAM64x18) in  $64 \times 18$  Mode (continued)**

| Parameter                | Symbol        | -1     |     | -Std  |     | Unit |
|--------------------------|---------------|--------|-----|-------|-----|------|
|                          |               | Min    | Max | Min   | Max |      |
| Write address setup time | $T_{ADDRCSU}$ | 0.088  |     | 0.104 |     | ns   |
| Write address hold time  | $T_{ADDRCHD}$ | 0.128  |     | 0.15  |     | ns   |
| Write enable setup time  | $T_{WECSU}$   | 0.397  |     | 0.467 |     | ns   |
| Write enable hold time   | $T_{WECHD}$   | -0.026 |     | -0.03 |     | ns   |
| Maximum frequency        | $F_{MAX}$     |        | 250 |       | 250 | MHz  |

The following table lists the  $\mu$ SRAM in  $64 \times 16$  mode in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 238 •  $\mu$ SRAM (RAM64x16) in  $64 \times 16$  Mode**

| Parameter                                                                             | Symbol          | -1     |       | -Std   |       | Unit |
|---------------------------------------------------------------------------------------|-----------------|--------|-------|--------|-------|------|
|                                                                                       |                 | Min    | Max   | Min    | Max   |      |
| Read clock period                                                                     | $T_{CY}$        | 4      |       | 4      |       | ns   |
| Read clock minimum pulse width high                                                   | $T_{CLKMPWH}$   | 1.8    |       | 1.8    |       | ns   |
| Read clock minimum pulse width low                                                    | $T_{CLKMPWL}$   | 1.8    |       | 1.8    |       | ns   |
| Read pipeline clock period                                                            | $T_{PLCY}$      | 4      |       | 4      |       | ns   |
| Read pipeline clock minimum pulse width high                                          | $T_{PLCLKMPWH}$ | 1.8    |       | 1.8    |       | ns   |
| Read pipeline clock minimum pulse width low                                           | $T_{PLCLKMPWL}$ | 1.8    |       | 1.8    |       | ns   |
| Read access time with pipeline register                                               | $T_{CLK2Q}$     |        | 0.266 |        | 0.313 | ns   |
| Read access time without pipeline register                                            |                 |        | 1.677 |        | 1.973 | ns   |
| Read address setup time in synchronous mode                                           | $T_{ADDRSU}$    | 0.301  |       | 0.354  |       | ns   |
| Read address setup time in asynchronous mode                                          |                 | 1.856  |       | 2.184  |       | ns   |
| Read address hold time in synchronous mode                                            | $T_{ADDRHD}$    | 0.091  |       | 0.107  |       | ns   |
| Read address hold time in asynchronous mode                                           |                 | -0.778 |       | -0.915 |       | ns   |
| Read enable setup time                                                                | $T_{RDENSU}$    | 0.278  |       | 0.327  |       | ns   |
| Read enable hold time                                                                 | $T_{RDENHD}$    | 0.057  |       | 0.067  |       | ns   |
| Read block select setup time                                                          | $T_{BLKSU}$     | 1.839  |       | 2.163  |       | ns   |
| Read block select hold time                                                           | $T_{BLKHD}$     | -0.65  |       | -0.765 |       | ns   |
| Read block select to out disable time (when pipelined register is disabled)           | $T_{BLK2Q}$     |        | 2.036 |        | 2.396 | ns   |
| Read asynchronous reset removal time (pipelined clock)                                | $T_{RSTREM}$    | -0.023 |       | -0.027 |       | ns   |
| Read asynchronous reset removal time (non-pipelined clock)                            |                 | 0.046  |       | 0.054  |       | ns   |
| Read asynchronous reset recovery time (pipelined clock)                               | $T_{RSTREC}$    | 0.507  |       | 0.597  |       | ns   |
| Read asynchronous reset recovery time (non-pipelined clock)                           |                 | 0.236  |       | 0.278  |       | ns   |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$       |        | 0.835 |        | 0.983 | ns   |
| Read synchronous reset setup time                                                     | $T_{SRSTSU}$    | 0.271  |       | 0.319  |       | ns   |

**Table 242 •  $\mu$ SRAM (RAM512x2) in 512 × 2 Mode (continued)**

| Parameter                            | Symbol         | –1    |     | –Std  |     | Unit |
|--------------------------------------|----------------|-------|-----|-------|-----|------|
|                                      |                | Min   | Max | Min   | Max |      |
| Write clock period                   | $T_{CCY}$      | 4     |     | 4     |     | ns   |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8   |     | 1.8   |     | ns   |
| Write clock minimum pulse width low  | $T_{CCLKMPWL}$ | 1.8   |     | 1.8   |     | ns   |
| Write block setup time               | $T_{BLKCSU}$   | 0.404 |     | 0.476 |     | ns   |
| Write block hold time                | $T_{BLKCHD}$   | 0.007 |     | 0.008 |     | ns   |
| Write input data setup time          | $T_{DINCSU}$   | 0.101 |     | 0.118 |     | ns   |
| Write input data hold time           | $T_{DINCHD}$   | 0.137 |     | 0.161 |     | ns   |
| Write address setup time             | $T_{ADDRCSU}$  | 0.088 |     | 0.104 |     | ns   |
| Write address hold time              | $T_{ADDRCHD}$  | 0.247 |     | 0.29  |     | ns   |
| Write enable setup time              | $T_{WECSU}$    | 0.397 |     | 0.467 |     | ns   |
| Write enable hold time               | $T_{WECHD}$    | –0.03 |     | –0.03 |     | ns   |
| Maximum frequency                    | $F_{MAX}$      |       | 250 |       | 250 | MHz  |

The following table lists the  $\mu$ SRAM in 1024 × 1 mode in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 243 •  $\mu$ SRAM (RAM1024x1) in 1024 × 1 Mode**

| Parameter                                                                   | Symbol          | –1    |      | –Std  |      | Unit |
|-----------------------------------------------------------------------------|-----------------|-------|------|-------|------|------|
|                                                                             |                 | Min   | Max  | Min   | Max  |      |
| Read clock period                                                           | $T_{CY}$        | 4     |      | 4     |      | ns   |
| Read clock minimum pulse width high                                         | $T_{CLKMPWH}$   | 1.8   |      | 1.8   |      | ns   |
| Read clock minimum pulse width low                                          | $T_{CLKMPWL}$   | 1.8   |      | 1.8   |      | ns   |
| Read pipeline clock period                                                  | $T_{PLCY}$      | 4     |      | 4     |      | ns   |
| Read pipeline clock minimum pulse width high                                | $T_{PLCLKMPWH}$ | 1.8   |      | 1.8   |      | ns   |
| Read pipeline clock minimum pulse width low                                 | $T_{PLCLKMPWL}$ | 1.8   |      | 1.8   |      | ns   |
| Read access time with pipeline register                                     | $T_{CLK2Q}$     |       | 0.27 |       | 0.31 | ns   |
| Read access time without pipeline register                                  |                 |       | 1.78 |       | 2.1  | ns   |
| Read address setup time in synchronous mode                                 | $T_{ADDRSU}$    | 0.301 |      | 0.354 |      | ns   |
| Read address setup time in asynchronous mode                                |                 | 1.978 |      | 2.327 |      | ns   |
| Read address hold time in synchronous mode                                  | $T_{ADDRHD}$    | 0.137 |      | 0.161 |      | ns   |
| Read address hold time in asynchronous mode                                 |                 | –0.6  |      | –0.71 |      | ns   |
| Read enable setup time                                                      | $T_{RDENSU}$    | 0.278 |      | 0.327 |      | ns   |
| Read enable hold time                                                       | $T_{RDENHD}$    | 0.057 |      | 0.067 |      | ns   |
| Read block select setup time                                                | $T_{BLKSU}$     | 1.839 |      | 2.163 |      | ns   |
| Read block select hold time                                                 | $T_{BLKHD}$     | –0.65 |      | –0.77 |      | ns   |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$     |       | 2.16 |       | 2.54 | ns   |
| Read asynchronous reset removal time (pipelined clock)                      | $T_{RSTREM}$    | –0.02 |      | –0.03 |      | ns   |
| Read asynchronous reset removal time (non-pipelined clock)                  |                 | 0.046 |      | 0.054 |      | ns   |

**Table 259 • 2 Step IAP Programming (Fabric Only)**

| M2S/M2GL Device | Image size |     | Authenticate | Program | Verify | Unit |
|-----------------|------------|-----|--------------|---------|--------|------|
|                 | Bytes      |     |              |         |        |      |
| 005             | 302672     | 4   | 39           | 6       | Sec    |      |
| 010             | 568784     | 7   | 45           | 12      | Sec    |      |
| 025             | 1223504    | 14  | 55           | 23      | Sec    |      |
| 050             | 2424832    | 29  | 74           | 40      | Sec    |      |
| 060             | 2418896    | 39  | 83           | 50      | Sec    |      |
| 090             | 3645968    | 60  | 106          | 73      | Sec    |      |
| 150             | 6139184    | 100 | 154          | 120     | Sec    |      |

**Table 260 • 2 Step IAP Programming (eNVM Only)**

| M2S/M2GL Device | Image size |    | Authenticate | Program | Verify | Unit |
|-----------------|------------|----|--------------|---------|--------|------|
|                 | Bytes      |    |              |         |        |      |
| 005             | 137536     | 2  | 59           | 5       | Sec    |      |
| 010             | 274816     | 4  | 98           | 11      | Sec    |      |
| 025             | 274816     | 4  | 100          | 10      | Sec    |      |
| 050             | 2,78,528   | 3  | 107          | 9       | Sec    |      |
| 060             | 268480     | 5  | 98           | 22      | Sec    |      |
| 090             | 544496     | 10 | 174          | 43      | Sec    |      |
| 150             | 544496     | 10 | 175          | 44      | Sec    |      |

**Table 261 • 2 Step IAP Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size |     | Authenticate | Program | Verify | Unit |
|-----------------|------------|-----|--------------|---------|--------|------|
|                 | Bytes      |     |              |         |        |      |
| 005             | 439296     | 6   | 78           | 11      | Sec    |      |
| 010             | 842688     | 11  | 122          | 21      | Sec    |      |
| 025             | 1497408    | 19  | 135          | 32      | Sec    |      |
| 050             | 2695168    | 32  | 158          | 48      | Sec    |      |
| 060             | 2686464    | 43  | 159          | 70      | Sec    |      |
| 090             | 4190208    | 68  | 258          | 115     | Sec    |      |
| 150             | 6682768    | 109 | 308          | 162     | Sec    |      |

**Table 262 • SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|-----------------|------------------|--------------|---------|--------|------|
| 005             | 302672           | 6            | 41      | 8      | Sec  |
| 010             | 568784           | 10           | 48      | 14     | Sec  |
| 025             | 1223504          | 21           | 61      | 29     | Sec  |
| 050             | 2424832          | 39           | 82      | 50     | Sec  |
| 060             | 2418896          | 44           | 87      | 54     | Sec  |
| 090             | 3645968          | 66           | 112     | 79     | Sec  |
| 150             | 6139184          | 108          | 162     | 128    | Sec  |

**Table 263 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|-----------------|------------------|--------------|---------|--------|------|
| 005             | 137536           | 3            | 64      | 4      | Sec  |
| 010             | 274816           | 4            | 104     | 7      | Sec  |
| 025             | 274816           | 4            | 104     | 8      | Sec  |
| 050             | 2,78,528         | 4            | 102     | 8      | Sec  |
| 060             | 268480           | 6            | 102     | 8      | Sec  |
| 090             | 544496           | 10           | 179     | 15     | Sec  |
| 150             | 544496           | 10           | 180     | 15     | Sec  |

**Table 264 • SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|-----------------|------------------|--------------|---------|--------|------|
| 005             | 439296           | 9            | 83      | 11     | Sec  |
| 010             | 842688           | 15           | 129     | 21     | Sec  |
| 025             | 1497408          | 26           | 143     | 35     | Sec  |
| 050             | 2695168          | 43           | 163     | 55     | Sec  |
| 060             | 2686464          | 48           | 165     | 60     | Sec  |
| 090             | 4190208          | 75           | 266     | 91     | Sec  |
| 150             | 6682768          | 117          | 318     | 141    | Sec  |

## 2.3.14 Math Block Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC math block supports 18×18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently. The following table lists the math blocks with all registers used in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 268 • Math Blocks with all Registers Used**

| Parameter                           | Symbol          | –1     |       | –Std   |       | Unit |
|-------------------------------------|-----------------|--------|-------|--------|-------|------|
|                                     |                 | Min    | Max   | Min    | Max   |      |
| Input, control register setup time  | $T_{MISU}$      | 0.149  |       | 0.176  |       | ns   |
| Input, control register hold time   | $T_{MIHD}$      | 1.68   |       | 1.976  |       | ns   |
| CDIN input setup time               | $T_{MOCDINSU}$  | 0.185  |       | 0.218  |       | ns   |
| CDIN input hold time                | $T_{MOCDINHHD}$ | 0.08   |       | 0.094  |       | ns   |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | –0.419 |       | –0.493 |       | ns   |
| Synchronous reset/enable hold time  | $T_{MSRSTENHD}$ | 0.011  |       | 0.013  |       | ns   |
| Asynchronous reset removal time     | $T_{MARSTREM}$  | 0      |       | 0      |       | ns   |
| Asynchronous reset recovery time    | $T_{MARSTREC}$  | 0.088  |       | 0.104  |       | ns   |
| Output register clock to out delay  | $T_{MOCQ}$      |        | 0.232 |        | 0.273 | ns   |
| CLK minimum period                  | $T_{MCLKMP}$    | 2.245  |       | 2.641  |       | ns   |

The following table lists the math blocks with input bypassed and output registers used in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 269 • Math Block with Input Bypassed and Output Registers Used**

| Parameter                           | Symbol          | –1     |       | –Std   |       | Unit |
|-------------------------------------|-----------------|--------|-------|--------|-------|------|
|                                     |                 | Min    | Max   | Min    | Max   |      |
| Output register setup time          | $T_{MOSU}$      | 2.294  |       | 2.699  |       | ns   |
| Output register hold time           | $T_{MOHD}$      | 1.68   |       | 1.976  |       | ns   |
| CDIN input setup time               | $T_{MOCDINSU}$  | 0.115  |       | 0.136  |       | ns   |
| CDIN input hold time                | $T_{MOCDINHHD}$ | –0.444 |       | –0.522 |       | ns   |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | –0.419 |       | –0.493 |       | ns   |
| Synchronous reset/enable hold time  | $T_{MSRSTENHD}$ | 0.011  |       | 0.013  |       | ns   |
| Asynchronous reset removal time     | $T_{MARSTREM}$  | 0      |       | 0      |       | ns   |
| Asynchronous reset recovery time    | $T_{MARSTREC}$  | 0.014  |       | 0.017  |       | ns   |
| Output register clock to out delay  | $T_{MOCQ}$      |        | 0.232 |        | 0.273 | ns   |
| CLK minimum period                  | $T_{MCLKMP}$    | 2.179  |       | 2.563  |       | ns   |



**Table 277 • Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz) (continued)**

| Parameter                                              | Symbol | Min | Typ | Max | Unit | Condition                      |
|--------------------------------------------------------|--------|-----|-----|-----|------|--------------------------------|
| Startup time (with regard to stable oscillator output) | SUXTAL |     |     | 0.8 | ms   | 005, 010, 025, and 050 devices |
|                                                        |        |     |     | 1.0 | ms   | 090 and 150 devices            |

**Table 278 • Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)**

| Parameter                                              | Symbol     | Min                 | Typ   | Max                 | Unit | Condition                           |
|--------------------------------------------------------|------------|---------------------|-------|---------------------|------|-------------------------------------|
| Operating frequency                                    | FXTAL      |                     | 2     |                     | MHz  |                                     |
| Accuracy                                               | ACCXTAL    |                     |       | 0.00105             | %    | 050 devices                         |
|                                                        |            |                     |       | 0.003               | %    | 005, 010, 025, 090, and 150 devices |
|                                                        |            |                     |       | 0.004               | %    | 060 devices                         |
| Output duty cycle                                      | CYCXTAL    |                     | 49–51 | 47–53               | %    |                                     |
| Output period jitter (peak to peak)                    | JITPERXTAL |                     | 1     | 5                   | ns   |                                     |
| Output cycle to cycle jitter (peak to peak)            | JITCYCXTAL |                     | 1     | 5                   | ns   |                                     |
| Operating current                                      | IDYNXTAL   |                     | 0.3   |                     | mA   |                                     |
| Input logic level high                                 | VIHXTAL    | 0.9 V <sub>PP</sub> |       |                     | V    |                                     |
| Input logic level low                                  | VILXTAL    |                     |       | 0.1 V <sub>PP</sub> | V    |                                     |
| Startup time (with regard to stable oscillator output) | SUXTAL     |                     |       | 4.5                 | ms   | 010 and 050 devices                 |
|                                                        |            |                     |       | 5                   | ms   | 005 and 025 devices                 |
|                                                        |            |                     |       | 7                   | ms   | 090 and 150 devices                 |

**Table 279 • Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)**

| Parameter                                              | Symbol     | Min                 | Typ   | Max                 | Unit | Condition                                |
|--------------------------------------------------------|------------|---------------------|-------|---------------------|------|------------------------------------------|
| Operating frequency                                    | FXTAL      |                     | 32    |                     | kHz  |                                          |
| Accuracy                                               | ACCXTAL    |                     |       | 0.004               | %    | 005, 010, 025, 050, 060, and 090 devices |
|                                                        |            |                     |       | 0.005               | %    | 150 devices                              |
| Output duty cycle                                      | CYCXTAL    |                     | 49–51 | 47–53               | %    |                                          |
| Output period jitter (peak to peak)                    | JITPERXTAL |                     | 150   | 300                 | ns   |                                          |
| Output cycle to cycle jitter (peak to peak)            | JITCYCXTAL |                     | 150   | 300                 | ns   |                                          |
| Operating current                                      | IDYNXTAL   |                     | 0.044 |                     | mA   | 010 and 050 devices                      |
|                                                        |            |                     | 0.060 |                     | mA   | 005, 025, 060, 090, and 150 devices      |
| Input logic level high                                 | VIHXTAL    | 0.9 V <sub>PP</sub> |       |                     | V    |                                          |
| Input logic level low                                  | VILXTAL    |                     |       | 0.1 V <sub>PP</sub> | V    |                                          |
| Startup time (with regard to stable oscillator output) | SUXTAL     |                     |       | 115                 | ms   | 005, 025, 050, 090, and 150 devices      |
|                                                        |            |                     |       | 126                 | ms   | 010 devices                              |

The following table lists the system controller characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 286 • System Controller SPI Characteristics for All Devices**

| Symbol           | Description                                             | Conditions                                                                                            | Min | Typ   | Unit |
|------------------|---------------------------------------------------------|-------------------------------------------------------------------------------------------------------|-----|-------|------|
| sp1              | SC_SPI_SCK minimum period                               |                                                                                                       | 20  |       | ns   |
| sp2              | SC_SPI_SCK minimum pulse width high                     |                                                                                                       | 10  |       | ns   |
| sp3              | SC_SPI_SCK minimum pulse width low                      |                                                                                                       | 10  |       | ns   |
| sp4 <sup>1</sup> | SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%–90%) 1 | I/O configuration: LVTTTL 3.3 V–20 mA<br>AC loading: 35 pF<br>Test conditions: Typical voltage, 25 °C |     | 1.239 | ns   |
| sp5 <sup>1</sup> | SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%–90%) 1 | I/O configuration: LVTTTL 3.3 V–20 mA<br>AC loading: 35 pF<br>Test conditions: Typical voltage, 25 °C |     | 1.245 | ns   |
| sp6              | Data from master (SC_SPI_SDO) setup time                |                                                                                                       | 160 |       | ns   |
| sp7              | Data from master (SC_SPI_SDO) hold time                 |                                                                                                       | 160 |       | ns   |
| sp8              | SC_SPI_SDI setup time                                   |                                                                                                       | 20  |       | ns   |
| sp9              | SC_SPI_SDI hold time                                    |                                                                                                       | 20  |       | ns   |

1. For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>. Use the supported I/O Configurations for the System Controller SPI in the following table.

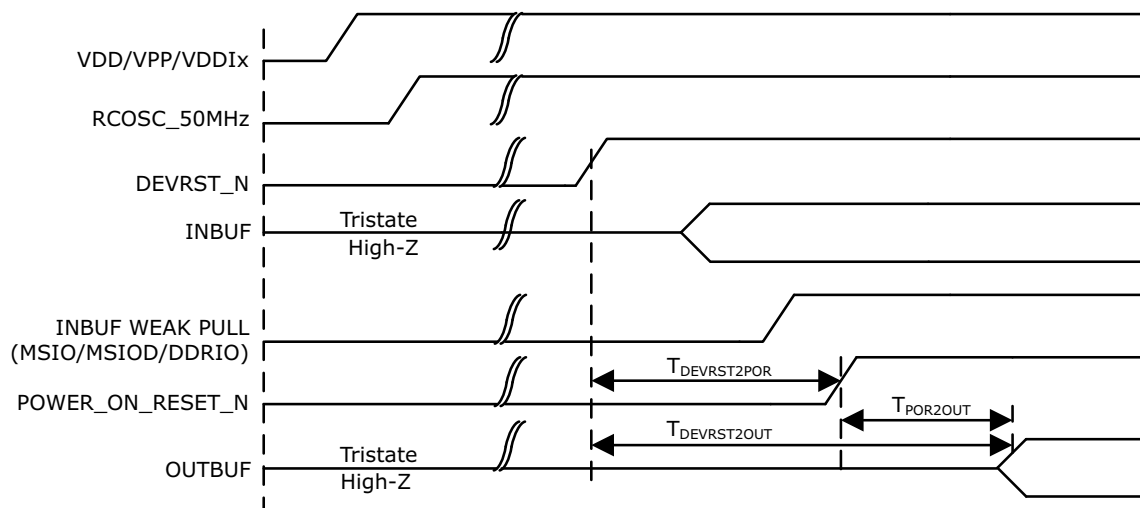
**Table 287 • Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)**

| Voltage Supply | I/O Drive Configuration | Unit |
|----------------|-------------------------|------|
| 3.3 V          | 20                      | mA   |
| 2.5 V          | 16                      | mA   |
| 1.8 V          | 12                      | mA   |
| 1.5 V          | 8                       | mA   |
| 1.2 V          | 4                       | mA   |

The following table lists the IGLOO2 DEVRST\_N to functional times in worst-case industrial conditions when  $T_J = 100\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 292 • DEVRST\_N to Functional Times for IGLOO2**

| Symbol                  | From             | To                      | Description                                       | Maximum Power-up to Functional Time for IGLOO2 (uS) |     |     |     |     |     |     |
|-------------------------|------------------|-------------------------|---------------------------------------------------|-----------------------------------------------------|-----|-----|-----|-----|-----|-----|
|                         |                  |                         |                                                   | 005                                                 | 010 | 025 | 050 | 060 | 090 | 150 |
| $T_{\text{POR2OUT}}$    | POWER_ON_RESET_N | Output available at I/O | Fabric to output                                  | 114                                                 | 116 | 113 | 113 | 115 | 115 | 114 |
| $T_{\text{DEVRST2OUT}}$ | DEVRST_N         | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 314                                                 | 353 | 314 | 307 | 343 | 341 | 341 |
| $T_{\text{DEVRST2POR}}$ | DEVRST_N         | POWER_ON_RESET_N        | $V_{DD}$ at its minimum threshold level to fabric | 200                                                 | 238 | 201 | 195 | 230 | 229 | 227 |
| $T_{\text{DEVRST2WPU}}$ | DEVRST_N         | DDRIO Inbuf weak pull   | DEVRST_N to Inbuf weak pull                       | 208                                                 | 202 | 197 | 193 | 216 | 215 | 215 |
|                         | DEVRST_N         | MSIO Inbuf weak pull    | DEVRST_N to Inbuf weak pull                       | 208                                                 | 202 | 197 | 193 | 216 | 215 | 215 |
|                         | DEVRST_N         | MSIOD Inbuf weak pull   | DEVRST_N to Inbuf weak pull                       | 208                                                 | 202 | 197 | 193 | 216 | 215 | 215 |

**Figure 20 • DEVRST\_N to Functional Timing Diagram for IGLOO2**

### 2.3.27 Flash\*Freeze Timing Characteristics

The following table lists the Flash\*Freeze entry and exit times in worst-case industrial conditions when  $T_J = 100^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 293 • Flash\*Freeze Entry and Exit Times**

| Parameter                                  | Symbol    | Entry/Exit Timing<br>FCLK = 100MHz     |     | Entry/Exit<br>Timing<br>FCLK = 3 MHz |  | Unit          | Conditions                                                                          |
|--------------------------------------------|-----------|----------------------------------------|-----|--------------------------------------|--|---------------|-------------------------------------------------------------------------------------|
|                                            |           | 005, 010, 025,<br>060, 090, and<br>150 | 050 | All Devices                          |  |               |                                                                                     |
| Entry time                                 | TFF_ENTRY | 160                                    | 150 | 320                                  |  | $\mu\text{s}$ | eNVM and MSS/HPMS PLL = ON                                                          |
|                                            |           | 215                                    | 200 | 430                                  |  | $\mu\text{s}$ | eNVM and MSS/HPMS PLL= OFF                                                          |
| Exit time with respect to the MSS PLL Lock | TFF_EXIT  | 100                                    | 100 | 140                                  |  | $\mu\text{s}$ | eNVM and MSS/HPMS PLL = ON during F*F                                               |
|                                            |           | 136                                    | 120 | 190                                  |  | $\mu\text{s}$ | eNVM = ON and MSS/HPMS PLL = OFF during F*F and MSS/HPMS PLL turned back on at exit |
|                                            |           | 200                                    | 200 | 285                                  |  | $\mu\text{s}$ | eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit          |
|                                            |           | 200                                    | 200 | 285                                  |  | $\mu\text{s}$ | eNVM = OFF and MSS/HPMS PLL = ON during F*F and eNVM turned back on at exit         |

**Table 303 • I2C Characteristics (continued)**

| Parameter                                                          | Symbol     | Min | Typ | Max | Unit | Conditions    |
|--------------------------------------------------------------------|------------|-----|-----|-----|------|---------------|
| Maximum data rate                                                  | $D_{MAX}$  |     |     | 400 | Kbps | Fast mode     |
|                                                                    |            |     |     | 100 | Kbps | Standard mode |
| Pulse width of spikes which must be suppressed by the input filter | $T_{FILT}$ |     | 50  |     | ns   | Fast mode     |

- These values are provided for MSIO Bank–LVTTL 8 mA Low Drive at 25 °C, typical conditions. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
- These maximum values are provided for information only. Minimum output buffer resistance values depend on  $V_{DDIX}$ , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
- $R(PULL-DOWN-MAX) = (VOL_{spec})/IOL_{spec}$ .
- $R(PULL-UP-MAX) = (VDDImax - VOH_{spec})/IOH_{spec}$ .

The following table lists the I<sup>2</sup>C switching characteristics in worst-case industrial conditions when  $T_J = 100\text{ °C}$ ,  $V_{DD} = 1.14\text{ V}$

**Table 304 • I2C Switching Characteristics**

| Parameter                | Symbol       | –1  | Std | Unit        |
|--------------------------|--------------|-----|-----|-------------|
|                          |              | Min | Min |             |
| Low period of I2C_x_SCL  | $T_{LOW}$    | 1   | 1   | PCLK cycles |
| High period of I2C_x_SCL | $T_{HIGH}$   | 1   | 1   | PCLK cycles |
| START hold time          | $T_{HD;STA}$ | 1   | 1   | PCLK cycles |
| START setup time         | $T_{SU;STA}$ | 1   | 1   | PCLK cycles |
| DATA hold time           | $T_{HD;DAT}$ | 1   | 1   | PCLK cycles |
| DATA setup time          | $T_{SU;DAT}$ | 1   | 1   | PCLK cycles |
| STOP setup time          | $T_{SU;STO}$ | 1   | 1   | PCLK cycles |

**Figure 21 • I<sup>2</sup>C Timing Parameter Definition**