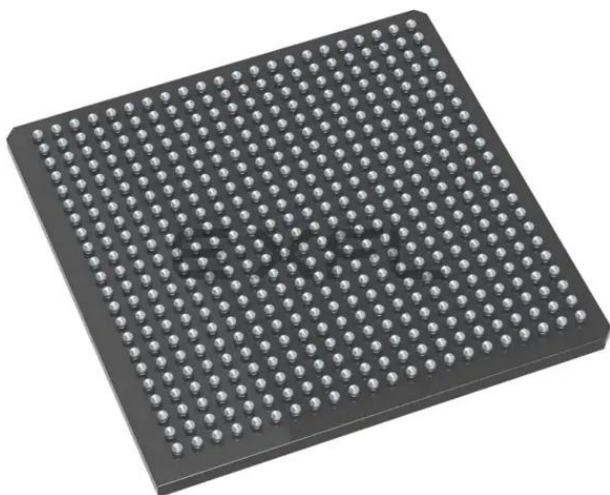




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	146124
Total RAM Bits	5120000
Number of I/O	248
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BFBGA
Supplier Device Package	484-BGA
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl150t-1fcvg484i



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Tables

Table 1	IGLOO2 and SmartFusion2 Design Security Densities	4
Table 2	IGLOO2 and SmartFusion2 Data Security Densities	4
Table 3	Absolute Maximum Ratings	5
Table 4	Recommended Operating Conditions	6
Table 5	FPGA Operating Limits	7
Table 6	Embedded Operating Flash Limits	8
Table 7	Device Storage Temperature and Retention	8
Table 8	High Temperature Data Retention (HTR) Lifetime	8
Table 9	Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices	10
Table 10	Quiescent Supply Current Characteristics	12
Table 11	SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD} = 1.2\text{ V}$) – Typical Process	12
Table 12	Currents During Program Cycle, $0\text{ }^{\circ}\text{C} \leq T_J \leq 85\text{ }^{\circ}\text{C}$ – Typical Process	13
Table 13	Currents During Verify Cycle, $0\text{ }^{\circ}\text{C} \leq T_J \leq 85\text{ }^{\circ}\text{C}$ – Typical Process	13
Table 14	SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD} = 1.26\text{ V}$) – Worst-Case Process	13
Table 15	Average Junction Temperature and Voltage Derating Factors for Fabric Timing Delays	14
Table 16	Inrush Currents at Power up, $-40\text{ }^{\circ}\text{C} \leq T_J \leq 100\text{ }^{\circ}\text{C}$ – Typical Process	14
Table 17	Timing Model Parameters	15
Table 18	Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions	19
Table 19	Maximum Data Rate Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions	20
Table 20	Maximum Data Rate Summary Table for Differential I/O in Worst-Case Industrial Conditions	20
Table 21	Maximum Frequency Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions	20
Table 22	Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions	21
Table 23	Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions	21
Table 24	Input Capacitance, Leakage Current, and Ramp Time	22
Table 25	I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank	22
Table 26	I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank	23
Table 27	I/O Weak Pull-up/Pull-down Resistances for MSIOD I/O Bank	23
Table 28	Schmitt Trigger Input Hysteresis	23
Table 29	LVTTL/LVC MOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)	24
Table 30	LVTTL/LVC MOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)	24
Table 31	LVC MOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)	24
Table 32	LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)	24
Table 33	LVTTL/LVC MOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)	24
Table 34	LVTTL/LVC MOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)	25
Table 35	LVTTL/LVC MOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)	25
Table 36	LVTTL/LVC MOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only)	25
Table 37	LVTTL/LVC MOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank	25
Table 38	LVC MOS 2.5 V DC Recommended DC Operating Conditions	26
Table 39	LVC MOS 2.5 V DC Input Voltage Specification	26
Table 40	LVC MOS 2.5 V DC Output Voltage Specification	26
Table 41	LVC MOS 2.5 V AC Minimum and Maximum Switching Speed	26
Table 42	LVC MOS 2.5 V AC Calibrated Impedance Option	26
Table 43	LVC MOS 2.5 V Receiver Characteristics (Input Buffers)	27
Table 44	LVC MOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)	27
Table 45	LVC MOS 2.5 V AC Test Parameter Specifications	27
Table 46	LVC MOS 2.5 V Transmitter Drive Strength Specifications	27
Table 47	LVC MOS 2.5 V Transmitter Characteristics for MSIO Bank (Output and Tristate Buffers)	28
Table 48	LVC MOS 1.8 V DC Recommended Operating Conditions	29
Table 49	LVC MOS 1.8 V DC Input Voltage Specification	29
Table 50	LVC MOS 1.8 V DC Output Voltage Specification	29

Table 108	SSTL2 AC Differential Voltage Specifications	44
Table 109	SSTL2 Minimum and Maximum AC Switching Speeds	44
Table 110	SSTL2 AC Impedance Specifications	44
Table 111	DDR1/SSTL2 AC Test Parameter Specifications	44
Table 112	SSTL2 Receiver Characteristics for MSIO I/O Bank (Input Buffers)	45
Table 113	DDR1/SSTL2 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)	45
Table 114	SSTL2 Class I Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)	45
Table 115	DDR1/SSTL2 Class I Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)	45
Table 116	DDR1/SSTL2 Class I Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)	45
Table 117	DDR1/SSTL2 Class II Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)	45
Table 118	SSTL18 DC Recommended DC Operating Conditions	46
Table 119	SSTL18 DC Input Voltage Specification	46
Table 120	SSTL18 DC Output Voltage Specification	46
Table 121	DDR1/SSTL2 Class II Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)	46
Table 122	DDR2/SSTL18 Receiver Characteristics for DDRIO I/O Bank with Fixed Code	47
Table 123	SSTL18 DC Differential Voltage Specification	47
Table 124	SSTL18 AC Differential Voltage Specifications (Applicable to DDRIO Bank Only)	47
Table 125	SSTL18 Minimum and Maximum AC Switching Speed (Applicable to DDRIO Bank Only)	47
Table 126	SSTL18 AC Impedance Specifications (Applicable to DDRIO Bank Only)	47
Table 127	SSTL18 AC Test Parameter Specifications (Applicable to DDRIO Bank Only)	47
Table 128	SSTL15 DC Recommended DC Operating Conditions (for DDRIO I/O Bank Only)	48
Table 129	SSTL15 DC Input Voltage Specification (for DDRIO I/O Bank Only)	48
Table 130	DDR2/SSTL18 Transmitter Characteristics (Output and Tristate Buffers)	48
Table 131	SSTL15 AC SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)	49
Table 132	SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)	49
Table 133	SSTL15 AC Calibrated Impedance Option (for DDRIO I/O Bank Only)	49
Table 134	SSTL15 DC Output Voltage Specification (for DDRIO I/O Bank Only)	49
Table 135	SSTL15 DC Differential Voltage Specification (for DDRIO I/O Bank Only)	49
Table 136	DDR3/SSTL15 Receiver Characteristics for DDRIO I/O Bank – with Calibration Only	50
Table 137	DDR3/SSTL15 Transmitter Characteristics (Output and Tristate Buffers)	50
Table 138	SSTL15 AC Test Parameter Specifications (for DDRIO I/O Bank Only)	50
Table 139	LPDDR DC Recommended DC Operating Conditions	51
Table 140	LPDDR DC Input Voltage Specification	51
Table 141	LPDDR DC Output Voltage Specification Reduced Drive	51
Table 142	LPDDR DC Output Voltage Specification Full Drive	51
Table 143	LPDDR DC Differential Voltage Specification	51
Table 144	LPDDR Receiver Characteristics for DDRIO I/O Bank with Fixed Codes	52
Table 145	LPDDR Reduced Drive for DDRIO I/O Bank (Output and Tristate Buffers)	52
Table 146	LPDDR AC Differential Voltage Specifications (for DDRIO I/O Bank Only)	52
Table 147	LPDDR AC Specifications (for DDRIO I/O Bank Only)	52
Table 148	LPDDR AC Calibrated Impedance Option (for DDRIO I/O Bank Only)	52
Table 149	LPDDR AC Test Parameter Specifications (for DDRIO I/O Bank Only)	52
Table 150	LPDDR-LVCMOS 1.8 V Mode Recommended DC Operating Conditions	53
Table 151	LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification	53
Table 152	LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification	53
Table 153	LPDDR-LVCMOS 1.8 V Minimum and Maximum AC Switching Speeds	53
Table 154	LPDDR-LVCMOS 1.8 V Calibrated Impedance Option	53
Table 155	LPDDR Full Drive for DDRIO I/O Bank (Output and Tristate Buffers)	53
Table 156	LPDDR-LVCMOS 1.8 V AC Test Parameter Specifications	54
Table 157	LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification for DDRIO Bank	54
Table 158	LPDDR-LVCMOS 1.8V AC Switching Characteristics for Receiver (for DDRIO I/O Bank with Fixed Code - Input Buffers)	54
Table 159	LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers)	54
Table 160	LVDS Recommended DC Operating Conditions	55

Table 214	LVPECL Recommended DC Operating Conditions	64
Table 215	LVPECL Receiver Characteristics for MSIO I/O Bank	65
Table 216	LVPECL DC Input Voltage Specification	65
Table 217	LVPECL DC Differential Voltage Specification	65
Table 218	LVPECL Minimum and Maximum AC Switching Speeds	65
Table 219	Input Data Register Propagation Delays	67
Table 220	Output/Enable Data Register Propagation Delays	69
Table 221	Input DDR Propagation Delays	71
Table 222	Output DDR Propagation Delays	74
Table 223	Combinatorial Cell Propagation Delays	76
Table 224	Register Delays	77
Table 225	150 Device Global Resource	78
Table 226	090 Device Global Resource	78
Table 227	050 Device Global Resource	78
Table 228	025 Device Global Resource	78
Table 229	010 Device Global Resource	79
Table 230	005 Device Global Resource	79
Table 231	RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18	79
Table 232	RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9	80
Table 233	RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4	81
Table 234	RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2	83
Table 235	RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1	84
Table 236	RAM1K18 – Two-Port Mode for Depth × Width Configuration 512 × 36	85
Table 237	μSRAM (RAM64x18) in 64 × 18 Mode	86
Table 238	μSRAM (RAM64x16) in 64 × 16 Mode	87
Table 239	μSRAM (RAM128x9) in 128 × 9 Mode	88
Table 240	μSRAM (RAM128x8) in 128 × 8 Mode	89
Table 241	μSRAM (RAM256x4) in 256 × 4 Mode	91
Table 242	μSRAM (RAM512x2) in 512 × 2 Mode	92
Table 243	μSRAM (RAM1024x1) in 1024 × 1 Mode	93
Table 244	JTAG Programming (Fabric Only)	94
Table 245	JTAG Programming (eNVM Only)	95
Table 246	JTAG Programming (Fabric and eNVM)	95
Table 247	2 Step IAP Programming (Fabric Only)	95
Table 248	2 Step IAP Programming (eNVM Only)	96
Table 249	2 Step IAP Programming (Fabric and eNVM)	96
Table 250	SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)	96
Table 251	SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)	96
Table 252	SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)	97
Table 253	Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)	97
Table 254	Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)	97
Table 255	Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)	98
Table 256	JTAG Programming (Fabric Only)	99
Table 257	JTAG Programming (eNVM Only)	99
Table 258	JTAG Programming (Fabric and eNVM)	99
Table 259	2 Step IAP Programming (Fabric Only)	100
Table 260	2 Step IAP Programming (eNVM Only)	100
Table 261	2 Step IAP Programming (Fabric and eNVM)	100
Table 262	SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)	101
Table 263	SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)	101
Table 264	SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)	101
Table 265	Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)	102
Table 266	Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)	102
Table 267	Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)	102
Table 268	Math Blocks with all Registers Used	103
Table 269	Math Block with Input Bypassed and Output Registers Used	103
Table 270	Math Block with Input Register Used and Output in Bypass Mode	104
Table 271	Math Block with Input and Output in Bypass Mode	104
Table 272	eNVM Read Performance	104

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- Updated [Table 24](#), page 22 with minimum and maximum values for input current low and high (SAR 73114 and 80314).
- Added [Non-Deterministic Random Bit Generator \(NRBG\) Characteristics](#), page 106 (SAR 73114 and 79517).
- Added 060 device in [Table 282](#), page 110 (SAR 79860).
- Added [DEVRST_N to Functional Times](#), page 116 (SAR 73114).
- Added [Cryptographic Block Characteristics](#), page 106 (SAR 73114 and 79516).
- Update [Table 296](#), page 121 with VTX-AMP details (SAR 81756).
- Update note in [Table 297](#), page 122 (SAR 74570 and 80677).
- Update [Table 298](#), page 122 with generic EPCS details (SAR 75307).
- Added [Table 308](#), page 129 (SAR 50424).

1.2 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- The Surge Current on VDD during DEVRST_B Assertion and Surge Current on VDD during Digest Check using System Services tables were deleted and added reference to [AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note](#). (SAR 76865 and 76623).
- Added 060 device in [Table 4](#), page 6 (SAR 76383).
- Updated [Table 24](#), page 22 for ramp time input (SAR 72103).
- Added 060 device details in [Table 284](#), page 112 (SAR 74927).
- Updated [Table 290](#), page 116 for name change (SAR 74925).
- Updated [Table 283](#), page 111 for 060 FG676 Package details (SAR 78849).
- Updated [Table 305](#), page 126 for SmartFusion2 and [Table 310](#), page 129 for IGLOO2 for SPI timing and Fmax (SAR 56645, 75331).
- Updated [Table 293](#), page 119 for Flash*Freeze entry and exit times (SAR 75329, 75330).
- Updated [Table 297](#), page 122 for RX-CID information (SAR 78271).
- Added [Table 8](#), page 8 and [Figure 1](#), page 9 (SAR 78932).
- Updated [Table 223](#), page 76 for timing characteristics and [Table 224](#), page 77 (SAR 75998).
- Added [SRAM PUF](#), page 105 (SAR 64406).
- Added a footnote on digest cycle in [Table 5](#), page 7 (SAR 79812).

1.3 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document.

- Added a note in [Table 5](#), page 7 (SAR 71506).
- Added a note in [Table 6](#), page 8 (SAR 74616).
- Added a note in [Figure 3](#), page 17 (SAR 71506).
- Updated Quiescent Supply Current for 060 in [Table 11](#), page 12 and [Table 12](#), page 13 (SAR 74483).
- Updated programming currents for 060 in [Table 13](#), page 13, [Table 14](#), page 13, and [Table 15](#), page 14.
- Added DEVRST_B assertion tables (SAR 74708).
- Updated I/O speeds for LVDS 3.3 V in [Table 18](#), page 19 and [Table 21](#), page 20 (SAR 69829).
- Updated [Table 24](#), page 22 (SAR 69418).
- Updated [Table 25](#), page 22, [Table 26](#), page 23, [Table 27](#), page 23 (SAR 74570).
- Updated all AC/DC table to link to the [Input Capacitance, Leakage Current, and Ramp Time](#), page 22 for reference (SAR 69418).

2.2 References

The following documents are recommended references:

- [PB0121: IGLOO2 Product Brief](#)
- [DS0124: IGLOO2 Pin Descriptions](#)
- [PB0115: SmartFusion2 SoC FPGA Product Brief](#)
- [DS0115: SmartFusion2 Pin Descriptions](#)

All product documentation for IGLOO2 and SmartFusion2 is available at:

<http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga>

<http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#overview>

2.3 Electrical Specifications

2.3.1 Operating Conditions

The following table lists the stress limits. Stress applied above the specified limit may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table are not implied.

Table 3 • Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
DC core supply voltage. Must always power this pin.	V _{DD}	−0.3	1.32	V
Power supply for charge pumps (for normal operation and programming). Must always power this pin.	V _{PP}	−0.3	3.63	V
Analog power pad for MDDR PLL	MSS_MDDR_PLL_VDDA	−0.3	3.63	V
Analog power pad for MDDR PLL	HPMS_MDDR_PLL_VDDA	−0.3	3.63	V
Analog power pad for FDDR PLL	FDDR_PLL_VDDA	−0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_MSS_MDDR_VDDA	−0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_HPMS_MDDR_VDDA	−0.3	3.63	V
Analog power pad for PLL0–5	CCC_XX[01]_PLL_VDDA	−0.3	3.63	V
High supply voltage for PLL SerDes[01]	SERDES_[01]_PLL_VDDA	−0.3	3.63	V
Analog power for SerDes[01] PLL lane0 to lane3. This is a 2.5 V SerDes internal PLL supply.	SERDES_[01]_L[0123]_VDDAPLL	−0.3	2.75	V
TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply.	SERDES_[01]_L[0123]_VDDAIO	−0.3	1.32	V
PCIe/PCS power supply	SERDES_[01]_VDD	−0.3	1.32	V
DC FPGA I/O buffer supply voltage for MSIO I/O bank	V _{DDI_x}	−0.3	3.63	V
DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks	V _{DDI_x}	−0.3	2.75	V
I/O Input voltage for MSIO I/O bank	V _I	−0.3	3.63	V
I/O Input voltage for MSIOD/DDRIO I/O bank	V _I	−0.3	2.75	V
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to V _{PP} .	V _{PPNVM}	−0.3	3.63	V
Storage temperature ¹	T _{STG}	−65	150	°C
Junction temperature	T _J	−55	135	°C

The following table lists the embedded operating flash limits.

Table 6 • Embedded Operating Flash Limits

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Commercial	Embedded flash	Min $T_J = 0\text{ }^{\circ}\text{C}$ Max $T_J = 85\text{ }^{\circ}\text{C}$	Min $T_J = 0\text{ }^{\circ}\text{C}$ Max $T_J = 85\text{ }^{\circ}\text{C}$	< 1000 cycles per page, up to two million cycles per eNVM array	20 years
			Min $T_J = 0\text{ }^{\circ}\text{C}$ Max $T_J = 85\text{ }^{\circ}\text{C}$	< 10000 cycles per page, up to 20 million cycles per eNVM array	10 years
Industrial	Embedded flash	Min $T_J = -40\text{ }^{\circ}\text{C}$ Max $T_J = 100\text{ }^{\circ}\text{C}$	Min $T_J = -40\text{ }^{\circ}\text{C}$ Max $T_J = 100\text{ }^{\circ}\text{C}$	< 1000 cycles per page, up to two million cycles per eNVM array	20 years
			Min $T_J = -40\text{ }^{\circ}\text{C}$ Max $T_J = 100\text{ }^{\circ}\text{C}$	< 10000 cycles per page, up to 20 million cycles per eNVM array	10 years

Note: If your product qualification requires accelerated programming cycles, see [Microsemi SoC Products Quality and Reliability Report](#) about recommended methodologies.

Table 7 • Device Storage Temperature and Retention

Product Grade	Storage Temperature (T_{stg})	Retention
Commercial	Min $T_J = 0\text{ }^{\circ}\text{C}$ Max $T_J = 85\text{ }^{\circ}\text{C}$	20 years
Industrial	Min $T_J = -40\text{ }^{\circ}\text{C}$ Max $T_J = 100\text{ }^{\circ}\text{C}$	20 years

Table 8 • High Temperature Data Retention (HTR) Lifetime

T_J (C)	HTR Lifetime ¹ (yrs)
90	20.5
95	20.5
100	20.5
105	17.0
110	15.0
115	13.0
120	11.5
125	10.0
130	8.0
135	6.0
140	4.5
145	3.0
150	1.5

1. HTR Lifetime is the period during which a verify failure is not expected due to flash leakage.

Table 17 • Timing Model Parameters (continued)

Index	Symbol	Description	-1	Unit	For More Information
F	T_{DP}	Propagation delay of an OR gate	0.179	ns	See Table 223 , page 76
G	T_{DP}	Propagation delay of an LVDS transmitter	2.136	ns	See Table 169 , page 57
H	T_{DP}	Propagation delay of a three-input XOR Gate	0.241	ns	See Table 223 , page 76
I	T_{DP}	Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 16 mA on the MSIO bank	2.412	ns	See Table 46 , page 27
J	T_{DP}	Propagation delay of a two-input NAND gate	0.179	ns	See Table 223 , page 76
K	T_{DP}	Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 8 mA on the MSIO bank	2.309	ns	See Table 46 , page 27
L	T_{CLKQ}	Clock-to-Q of the data register	0.108	ns	See Table 224 , page 77
	T_{SUD}	Setup time of the data register	0.254	ns	See Table 224 , page 77
M	T_{DP}	Propagation delay of a two-input AND gate	0.179	ns	See Table 223 , page 76
N	T_{OCLKQ}	Clock-to-Q of the output data register	0.263	ns	See Table 220 , page 69
	T_{OSUD}	Setup time of the output data register	0.19	ns	See Table 220 , page 69
O	T_{DP}	Propagation delay of SSTL2, Class I transmitter on the MSIO bank	2.055	ns	See Table 114 , page 45
P	T_{DP}	Propagation delay of LVCMOS 1.5 V transmitter, drive strength of 12 mA, fast slew on the DDRIO bank	3.316	ns	See Table 70 , page 34

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIO I/O bank at V_{OH}/V_{OL} Level.

Table 26 • I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank

V_{DDI} Domain	R(WEAK PULL-UP) at V_{OH} (Ω)		R(WEAK PULL-DOWN) at V_{OL} (Ω)	
	Min	Max	Min	Max
3.3 V	9.9K	17.1K	9.98K	17.5K
2.5 V ^{1, 2}	10K	17.6K	10.1K	18.4K
1.8 V ^{1, 2}	10.4K	19.1K	10.4K	20.4K
1.5 V ^{1, 2}	10.7K	20.4K	10.8K	22.2K
1.2 V ^{1, 2}	11.3K	23.2K	11.5K	26.7K

1. $R(\text{WEAK PULL-DOWN}) = (V_{OLspec})/I(\text{WEAK PULL-DOWN MAX})$.
2. $R(\text{WEAK PULL-UP}) = (V_{DDImax} - V_{OHspec})/I(\text{WEAK PULL-UP MIN})$.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIOD I/O bank at V_{OH}/V_{OL} Level.

Table 27 • I/O Weak Pull-up/Pull-down Resistances for MSIOD I/O Bank

V_{DDI} Domain	R(WEAK PULL-UP) at V_{OH} (Ω)		R(WEAK PULL-DOWN) at V_{OL} (Ω)	
	Min	Max	Min	Max
2.5 V ^{1, 2}	9.6K	16.6K	9.5K	16.4K
1.8 V ^{1, 2}	9.7K	17.3K	9.7K	17.1K
1.5 V ^{1, 2}	9.9K	18K	9.8K	17.6K
1.2 V ^{1, 2}	10.3K	19.6K	10K	19.1K

1. $R(\text{WEAK PULL-DOWN}) = (V_{OLspec})/I(\text{WEAK PULL-DOWN MAX})$.
2. $R(\text{WEAK PULL-UP}) = (V_{DDImax} - V_{OHspec})/I(\text{WEAK PULL-UP MIN})$.

The following table lists the hysteresis voltage value for schmitt trigger mode input buffers.

Table 28 • Schmitt Trigger Input Hysteresis

Input Buffer Configuration	Hysteresis Value (Typical, unless otherwise noted)
3.3 V LVTTTL/LVCMOS/ PCI/PCI-X	$0.05 \times V_{DDI}$ (worst-case)
2.5 V LVCMOS	$0.05 \times V_{DDI}$ (worst-case)
1.8 V LVCMOS	$0.1 \times V_{DDI}$ (worst-case)
1.5 V LVCMOS	60 mV
1.2 V LVCMOS	20 mV

Table 62 • LVCMOS 1.5 V DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC output logic high	VOH	$V_{DDI} \times 0.75$		V
DC output logic low	VOL		$V_{DDI} \times 0.25$	V

Table 63 • LVCMOS 1.5 V AC Minimum and Maximum Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D _{MAX}	235	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D _{MAX}	160	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	D _{MAX}	220	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 64 • LVCMOS 1.5 V AC Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CA L	75, 60, 50, 40	Ω

Table 65 • LVCMOS 1.5 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point	V _{TRIP}	0.75	V
Resistance for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	R _{ENT}	2K	Ω
Capacitive loading for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	C _{ENT}	5	pF
Capacitive loading for data path (T _{DP})	C _{LOAD}	5	pF

Table 66 • LVCMOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			V _{OH} (V)	V _{OL} (V)	IOH (at V _{OH}) mA	IOL (at V _{OL}) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	2	2
4 mA	4 mA	4 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	4	4
6 mA	6 mA	6 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	6	6
8 mA		8 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	8	8
		10 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	10	10
		12 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	12	12

Note: For a detailed I/V curve, use the corresponding IBIS models:

www.microsemi.com/soc/download/ibis/default.aspx.

Table 122 • SSTL18 DC Differential Voltage Specification

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID} (DC)	0.3	V

Table 123 • SSTL18 AC Differential Voltage Specifications (Applicable to DDRIO Bank Only)

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF} (AC)	0.5		V
AC differential cross point voltage	V_x (AC)	$0.5 \times V_{DDI} - 0.175$	$0.5 \times V_{DDI} + 0.175$	V

Table 124 • SSTL18 Minimum and Maximum AC Switching Speed (Applicable to DDRIO Bank Only)

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	667	Mbps	AC loading: per JEDEC specification

Table 125 • SSTL18 AC Impedance Specifications (Applicable to DDRIO Bank Only)

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	R_{REF}	20, 42	Ω	Reference resistor = 150 Ω
Effective impedance value (ODT)	R_{TT}	50, 75, 150	Ω	Reference resistor = 150 Ω

Table 126 • SSTL18 AC Test Parameter Specifications (Applicable to DDRIO Bank Only)

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.9	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for SSTL18 Class I (T_{DP})	RTT_TEST	50	Ω
Reference resistance for data test path for SSTL18 Class II (T_{DP})	RTT_TEST	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

Table 127 • DDR2/SSTL18 Receiver Characteristics for DDRIO I/O Bank with Fixed Code

		T_{PY}		Unit
		-1	-Std	
Pseudo differential	None	1.567	1.844	ns
True differential	None	1.588	1.869	ns

Table 162 • LVDS DC Output Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 163 • LVDS DC Differential Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
Differential output voltage swing	V_{OD}	250	350	450	mV
Output common mode voltage	V_{OCM}	1.125	1.25	1.375	V
Input common mode voltage	V_{ICM}	0.05	1.25	2.35	V
Input differential voltage	V_{ID}	100	350	600	mV

Table 164 • LVDS Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	535	Mbps	AC loading: 12 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank) no pre-emphasis	D_{MAX}	620	Mbps	AC loading: 10 pF / 100 Ω differential load
		700	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 165 • LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Max	Unit
Termination resistance	R_T	100		Ω

Table 166 • LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

LVDS25 AC Switching Characteristics

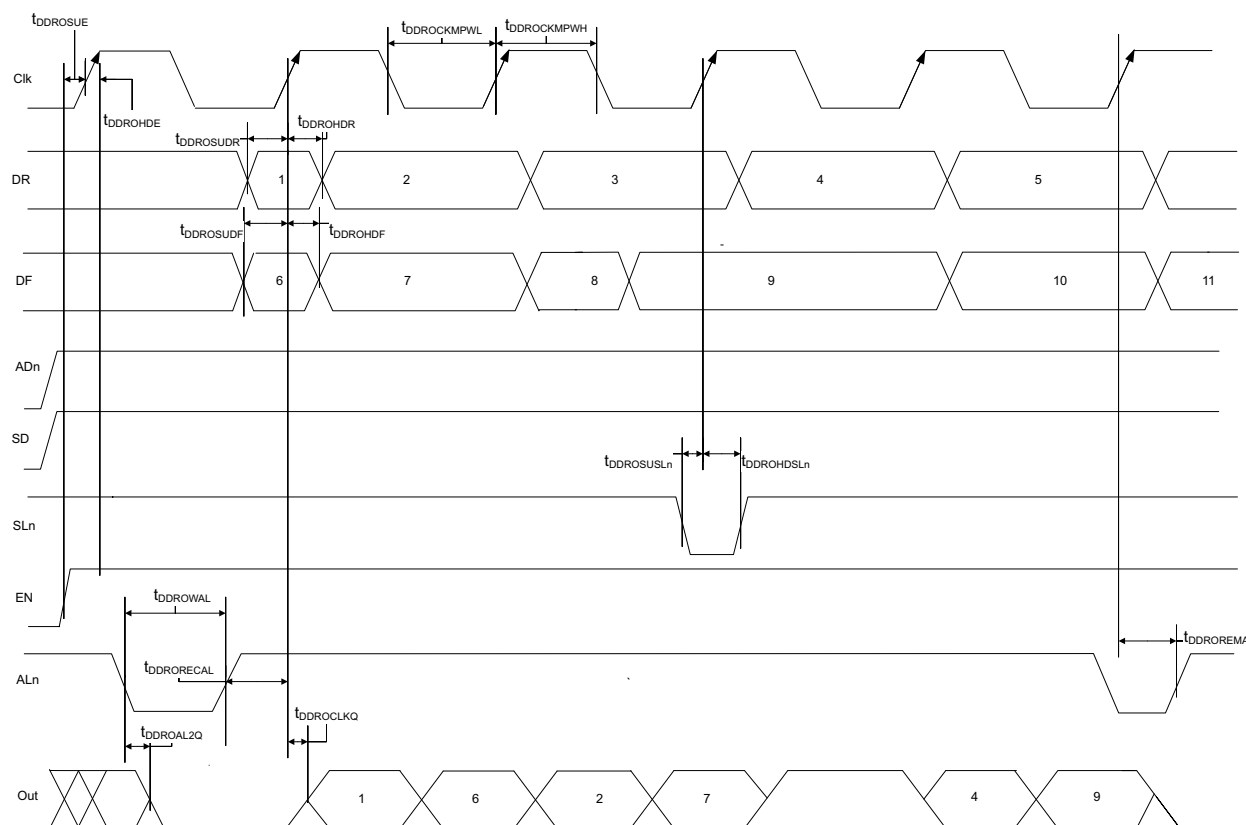
Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 167 • LVDS25 Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.774	3.263	ns
100	2.775	3.264	ns

Table 221 • Input DDR Propagation Delays (continued)

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
T _{DDRIWAL}	Asynchronous load minimum pulse width for input DDR	F, F	0.304	0.357	ns
T _{DDRICKMPWH}	Clock minimum pulse width high for input DDR	B, B	0.075	0.088	ns
T _{DDRICKMPWL}	Clock minimum pulse width low for input DDR	B, B	0.159	0.187	ns

Figure 13 • Output DDR Timing Diagram**2.3.9.5 Timing Characteristics**

The following table lists the output DDR propagation delays in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 222 • Output DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDROCLKQ}$	Clock-to-out of DDR for output DDR	E, G	0.263	0.309	ns
$T_{DDROSUDF}$	Data_F data setup for output DDR	F, E	0.143	0.168	ns
$T_{DDROSUDR}$	Data_R data setup for output DDR	A, E	0.19	0.223	ns
$T_{DDROHDF}$	Data_F data hold for output DDR	F, E	0	0	ns
$T_{DDROHDR}$	Data_R data hold for output DDR	A, E	0	0	ns
$T_{DDROSUE}$	Enable setup for input DDR	B, E	0.419	0.493	ns
T_{DDROHE}	Enable hold for input DDR	B, E	0	0	ns
$T_{DDROSUSLn}$	Synchronous load setup for input DDR	D, E	0.196	0.231	ns
$T_{DDROHSLn}$	Synchronous load hold for input DDR	D, E	0	0	ns
$T_{DDROAL2Q}$	Asynchronous load-to-out for output DDR	C, G	0.528	0.621	ns
$T_{DDRORECAL}$	Asynchronous load removal time for output DDR	C, E	0	0	ns
$T_{DDRORECAL}$	Asynchronous load recovery time for output DDR	C, E	0.034	0.04	ns

Table 239 • μ SRAM (RAM128x9) in 128 × 9 Mode (continued)

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.982	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 128 × 8 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 240 • μ SRAM (RAM128x8) in 128 × 8 Mode

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns

Table 242 • μ SRAM (RAM512x2) in 512 × 2 Mode (continued)

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.101		0.118		ns
Write input data hold time	T_{DINCHD}	0.137		0.161		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.247		0.29		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.03		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 1024 × 1 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 243 • μ SRAM (RAM1024x1) in 1024 × 1 Mode

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.27		0.31	ns
Read access time without pipeline register			1.78		2.1	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.978		2.327		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.137		0.161		ns
Read address hold time in asynchronous mode		–0.6		–0.71		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.77		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.16		2.54	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.02		–0.03		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns

The following table lists the programming times in worst-case conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 256 • JTAG Programming (Fabric Only)

M2S/M2GL Device	Image size		Program	Verify	Unit
	Bytes				
005	302672	44	10		Sec
010	568784	50	18		Sec
025	1223504	73	26		Sec
050	2424832	88	54		Sec
060	2418896	99	54		Sec
090	3645968	135	126		Sec
150	6139184	177	193		Sec

Table 257 • JTAG Programming (eNVM Only)

M2S/M2GL Device	Image size		Program	Verify	Unit
	Bytes				
005	137536	61	4		Sec
010	274816	100	9		Sec
025	274816	100	9		Sec
050	2,78,528	106	8		Sec
060	268480	98	8		Sec
090	544496	176	15		Sec
150	544496	177	15		Sec

Table 258 • JTAG Programming (Fabric and eNVM)

M2S/M2GL Device	Image size		Program	Verify	Unit
	Bytes				
005	439296	71	11		Sec
010	842688	129	20		Sec
025	1497408	142	35		Sec
050	2695168	184	59		Sec
060	2686464	180	70		Sec
090	4190208	288	147		Sec
150	6682768	338	231		Sec

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 270 • Math Block with Input Register Used and Output in Bypass Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input register setup time	T_{MISU}	0.149		0.176		ns
Input register hold time	T_{MIHD}	0.185		0.218		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	0.08		0.094		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	-0.012		-0.014		ns
Asynchronous reset removal time	$T_{MARSTREM}$	-0.005		-0.005		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.088		0.104		ns
Input register clock to output delay	T_{MICQ}		2.52		2.964	ns
CDIN to output delay	$T_{MCDIN2Q}$		1.951		2.295	ns

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 271 • Math Block with Input and Output in Bypass Mode

Parameter	Symbol	-1	-Std	Unit
		Max	Max	
Input to output delay	T_{MIQ}	2.568	3.022	ns
CDIN to output delay	$T_{MCDIN2Q}$	1.951	2.295	ns

2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when $V_{DD} = 1.14\text{ V}$, $V_{PPNVM} = V_{PP} = 2.375\text{ V}$.

Table 272 • eNVM Read Performance

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
T_J	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$F_{MAXREAD}$	eNVM maximum read frequency	25	25	25	25	25	25	MHz

The following table lists the eNVM page programming in worst-case conditions when $V_{DD} = 1.14\text{ V}$, $V_{PPNVM} = V_{PP} = 2.375\text{ V}$.

Table 273 • eNVM Page Programming

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
T_J	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$T_{PAGEPGM}$	eNVM page programming time	40	40	40	40	40	40	ms

2.3.21 Clock Conditioning Circuits (CCC)

The following table lists the CCC/PLL specifications in worst-case industrial conditions when $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 282 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification

Parameter	Min	Typ	Max	Unit	Conditions
Clock conditioning circuitry input frequency F_{IN_CCC}	1		200	MHz	All CCC
	0.032		200	MHz	32 kHz capable CCC
Clock conditioning circuitry output frequency $F_{OUT_CCC}^1$	0.078		400	MHz	
PLL VCO frequency ²	500		1000	MHz	
Delay increments in programmable delay blocks		75	100	ps	
Number of programmable values in each programmable delay block			64		
Acquisition time		70	100	μs	$F_{IN} \geq 1\text{ MHz}$
		1	16	ms	$F_{IN} = 32\text{ kHz}$
Input duty cycle (reference clock)					Internal Feedback
	10		90	%	$1\text{ MHz} \leq F_{IN_CCC} \leq 25\text{ MHz}$
	25		75	%	$25\text{ MHz} \leq F_{IN_CCC} \leq 100\text{ MHz}$
	35		65	%	$100\text{ MHz} \leq F_{IN_CCC} \leq 150\text{ MHz}$
	45		55	%	$150\text{ MHz} \leq F_{IN_CCC} \leq 200\text{ MHz}$
					External Feedback (CCC, FPGA, Off-chip)
	25		75	%	$1\text{ MHz} \leq F_{IN_CCC} \leq 25\text{ MHz}$
	35		65	%	$25\text{ MHz} \leq F_{IN_CCC} \leq 35\text{ MHz}$
	45		55	%	$35\text{ MHz} \leq F_{IN_CCC} \leq 50\text{ MHz}$
Output duty cycle	48		52	%	050 devices $F_{OUT} \leq 400\text{ MHz}$
	48		52	%	005, 010, and 025 devices $F_{OUT} < 350\text{ MHz}$
	46		54	%	005, 010, and 025 devices $350\text{ MHz} \leq F_{out} \leq 400\text{ MHz}$
	48		52	%	060 and 090 devices $F_{OUT} \leq 100\text{ MHz}$
	44		52	%	060 and 090 devices $100\text{ MHz} \leq F_{OUT} \leq 400\text{ MHz}$
	48		52	%	150 devices $F_{OUT} \leq 120\text{ MHz}$
	45		52	%	150 devices $120\text{ MHz} \leq F_{OUT} \leq 400\text{ MHz}$
Spread Spectrum Characteristics					
Modulation frequency range	25	35	50	k	
Modulation depth range	0		1.5	%	
Modulation depth control		0.5		%	

The following table lists the receiver pa in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 297 • Receiver Parameters

Symbol	Description	Min	Typ	Max	Unit
VRX-IN-PP-CC	Differential input peak-to-peak sensitivity (2.5 Gbps)	0.238		1.2	V
	Differential input peak-to-peak sensitivity (2.5 Gbps, de-emphasized)	0.219		1.2	V
	Differential input peak-to-peak sensitivity (5.0 Gbps)	0.300		1.2	V
	Differential input peak-to-peak sensitivity (5.0 Gbps, de-emphasized)	0.300		1.2	V
VRX-CM-AC-P	Input common mode range (AC coupled)			150	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset			15	μs
RLRX-DIFF	Return loss differential mode (2.5 Gbps)	-10			dB
	Return loss differential mode (5.0 Gbps)				
	0.05 GHz to 1.25 GHz	-10			dB
	1.25 GHz to 2.5 GHz	-8			dB
RLRX-CM	Return loss common mode (2.5 Gbps, 5.0 Gbps)	-6			dB
RX-CID ¹	CID limit PCIe Gen1/2			200	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65		175	mV

1. AC-coupled, BER = e^{-12} , using synchronous clock.

Table 298 • SerDes Protocol Compliance

Protocol	Maximum Data Rate (Gbps)	-1	-Std
PCIe Gen 1	2.5	Yes	Yes
PCIe Gen 2	5.0	Yes	
XAUI	3.125	Yes	
Generic EPCS	3.2	Yes	
Generic EPCS	2.5	Yes	Yes