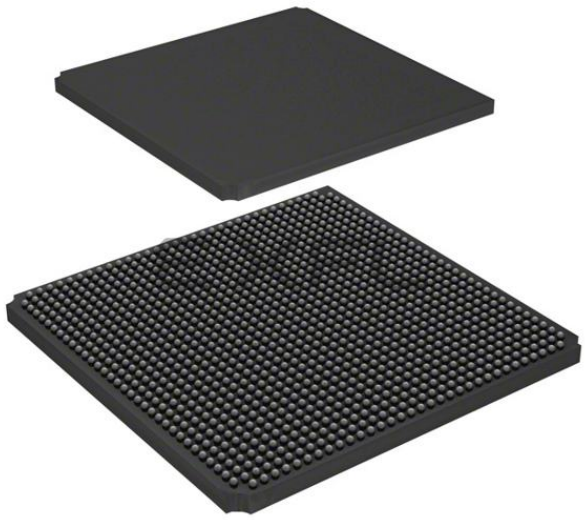

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 146124 |
| Total RAM Bits | 5120000 |
| Number of I/O | 574 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2gl150t-fc1152i |

# 2 IGLOO2 FPGA and SmartFusion2 SoC FPGA

Microsemi's mainstream SmartFusion®2 SoC and IGLOO®2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated math blocks, multiple embedded memory blocks, and high-performance SerDes communication interfaces on a single chip. Both families benefit from low-power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to 5 MBs of embedded RAM, up to 16 SerDes lanes, and up to four PCI Express Gen 2 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 devices integrate an entire low-power, real-time microcontroller subsystem (MSS) with a rich set of industry-standard peripherals including Ethernet, USB, and CAN, while IGLOO2 devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

## 2.1 Device Status

The following table shows the design security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

***Table 1 •*** **IGLOO2 and SmartFusion2 Design Security Densities**

| Design Security Device Densities | Status |
|---|---|
| 005 | Production |
| 010, 010T | Production |
| 025, 025T | Production |
| 050, 050T | Production |
| 060, 060T | Production |
| 090, 090T | Production |
| 150, 150T | Production |

The following table shows the data security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

***Table 2 •*** **IGLOO2 and SmartFusion2 Data Security Densities**

| Data Security Device Densities | Status |
|---|---|
| 005S | Production |
| 010TS | Production |
| 025TS | Production |
| 050TS | Production |
| 060TS | Production |
| 090TS | Production |
| 150TS | Production |

***Table 4 •*** **Recommended Operating Conditions *(continued)***

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| 3.3 V DC supply voltage | $V_{DDIx}$ | 3.15 | 3.3 | 3.45 | V | |
| LVDS differential I/O | $V_{DDIx}$ | 2.375 | 2.5 | 3.45 | V | |
| B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O | $V_{DDIx}$ | 2.375 | 2.5 | 2.625 | V | |
| LVPECL differential I/O | $V_{DDIx}$ | 3.15 | 3.3 | 3.45 | V | |
| Reference voltage supply for FDDR (Bank0) and MDDR (Bank5) | $V_{REFx}$ | 0.49 × $V_{DDIx}$ | 0.5 × $V_{DDIx}$ | 0.51 × $V_{DDIx}$ | V | |
| Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to $V_{PP}$. | $V_{PPNVM}$ | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |

1. Programming at Industrial temperature range is available only with $V_{PP}$ = 3.3 V.

**Note:** Power supply ramps must all be strictly monotonic, without plateaus.

***Table 5 •*** **FPGA Operating Limits**

| Product Grade | Element | Programming Temperature | Operating Temperature | Programming Cycles | Digest Temperature | Digest Cycles | Retention (Biased/ Unbiased) |
|---|---|---|---|---|---|---|---|
| Commercial | FPGA | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | 500 | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | 2000 | 20 years |
| Industrial[1] | FPGA | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | 500 | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | 2000 | 20 years |

1. Programming at Industrial temperature range is available only with VPP = 3.3 V.

**Note:** The retention specification is defined as the total number of programing and digest cycles. For example, 20 years of retention after 500 programming cycles.

**Note:** The digest cycle specification is 2000 digest cycles for every program cycle with a maximum of 500 programming cycles.

**Note:** If your product qualification requires accelerated programming cycles, see *Microsemi SoC Products Quality and Reliability Report* about recommended methodologies.

***Table 22 •*** **Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---|---|---|---|---|
| LPDDR | | | 200 | MHz |
| HSTL1.5 V | | | 200 | MHz |
| SSTL 2.5 V | 255 | 350 | 200 | MHz |
| SSTL 1.8 V | | | 334 | MHz |
| SSTL 1.5 V | | | 334 | MHz |

***Table 23 •*** **Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | Unit |
|---|---|---|---|
| LVPECL (input only) | 450 | | MHz |
| LVDS 3.3 V | 267.5 | | MHz |
| LVDS 2.5 V | 267.5 | 350 | MHz |
| RSDS | 260 | 350 | MHz |
| BLVDS | 250 | | MHz |
| MLVDS | 250 | | MHz |
| Mini-LVDS | 260 | 350 | MHz |

### 2.3.5.6 Single-Ended I/O Standards

#### 2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

#### 2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 29 •*** **LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 3.15 | 3.3 | 3.45 | V |

***Table 30 •*** **LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | 2.0 | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.8 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 31 •*** **LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high[1] | $V_{OH}$ | $V_{DDI}$ – 0.4 | | V |
| DC output logic low[1] | $V_{OL}$ | | 0.4 | V |

1. The $V_{OH}/V_{OL}$ test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

***Table 32 •*** **LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 2.4 | | V |
| DC output logic low | $V_{OL}$ | | 0.4 | V |

***Table 33 •*** **LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 600 | Mbps | AC loading: 17 pF load, maximum drive/slew |

***Table 53 •*** **LVCMOS 1.8 V AC Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | Rodt_cal | 75, 60, 50, 33, 25, 20 | Ω |

***Table 54 •*** **LVCMOS 1.8 V AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.9 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2k | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

***Table 55 •*** **LVCMOS 1.8 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | $V_{OH}$ (V) | $V_{OL}$ (V) | IOH (at $V_{OH}$) | IOL (at $V_{OL}$) |
|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank | Min | Max | mA | mA |
| 2 mA | 2 mA | 2 mA | $V_{DDI}$ – 0.45 | 0.45 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | $V_{DDI}$ – 0.45 | 0.45 | 4 | 4 |
| 6 mA | 6 mA | 6 mA | $V_{DDI}$ – 0.45 | 0.45 | 6 | 6 |
| 8 mA | 8 mA | 8 mA | $V_{DDI}$ – 0.45 | 0.45 | 8 | 8 |
| 10 mA | 10 mA | 10 mA | $V_{DDI}$ – 0.45 | 0.45 | 10 | 10 |
| 12 mA | | 12 mA | $V_{DDI}$ – 0.45 | 0.45 | 12 | 12 |
| | | 16 mA[1] | $V_{DDI}$ – 0.45 | 0.45 | 16 | 16 |

1. 16 mA drive strengths, all slews, meets LPDDR JEDEC electrical compliance.

### AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 1.71 V

***Table 56 •*** **LVCMOS 1.8 V Receiver Characteristics (Input Buffers)**

| | On-Die Termination (ODT) | $T_{PY}$ | | $T_{PYS}$ | | Unit |
|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | |
| **LVCMOS 1.8 V (for DDRIO I/O bank with Fixed Codes)** | None | 1.968 | 2.315 | 2.099 | 2.47 | ns |
| **LVCMOS 1.8 V (for MSIO I/O bank)** | None | 2.898 | 3.411 | 2.883 | 3.393 | ns |
| | 50 | 3.05 | 3.59 | 3.044 | 3.583 | ns |
| | 75 | 2.999 | 3.53 | 2.987 | 3.516 | ns |
| | 150 | 2.947 | 3.469 | 2.933 | 3.452 | ns |
| **LVCMOS 1.8 V (for MSIOD I/O bank)** | None | 2.611 | 3.071 | 2.598 | 3.057 | ns |
| | 50 | 2.775 | 3.264 | 2.775 | 3.265 | ns |
| | 75 | 2.72 | 3.2 | 2.712 | 3.19 | ns |
| | 150 | 2.666 | 3.137 | 2.655 | 3.123 | ns |

***Table 62 •*** **LVCMOS 1.5 V DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | VOH | $V_{DDI}$ × 0.75 | | V |
| DC output logic low | VOL | | $V_{DDI}$ × 0.25 | V |

***Table 63 •*** **LVCMOS 1.5 V AC Minimum and Maximum Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 235 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 160 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 220 | Mbps | AC loading: 17 pF load, maximum drive/slew |

***Table 64 •*** **LVCMOS 1.5 V AC Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | RODT_CAL | 75, 60, 50, 40 | Ω |

***Table 65 •*** **LVCMOS 1.5 V AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point | $V_{TRIP}$ | 0.75 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

***Table 66 •*** **LVCMOS 1.5 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | $V_{OH}$ (V) | $V_{OL}$ (V) | IOH (at $V_{OH}$) | IOL (at $V_{OL}$) |
|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank | Min | Max | mA | mA |
| 2 mA | 2 mA | 2 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 4 | 4 |
| 6 mA | 6 mA | 6 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 6 | 6 |
| 8 mA | | 8 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 8 | 8 |
| | | 10 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 10 | 10 |
| | | 12 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 12 | 12 |

**Note:** For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

***Table 70 •*** **LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers) *(continued)***

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 6 mA | Slow | 4.244 | 4.993 | 3.465 | 4.076 | 4.233 | 4.979 | 6.39 | 7.518 | 5.736 | 6.748 | ns |
| | Medium | 3.774 | 4.44 | 3.05 | 3.587 | 3.762 | 4.426 | 6.114 | 7.193 | 5.397 | 6.35 | ns |
| | Medium fast | 3.544 | 4.17 | 2.839 | 3.339 | 3.529 | 4.152 | 5.978 | 7.033 | 5.27 | 6.2 | ns |
| | Fast | 3.519 | 4.14 | 2.82 | 3.317 | 3.504 | 4.122 | 5.965 | 7.017 | 5.259 | 6.187 | ns |
| 8 mA | Slow | 4.099 | 4.823 | 3.311 | 3.894 | 4.087 | 4.807 | 6.584 | 7.746 | 5.854 | 6.888 | ns |
| | Medium | 3.656 | 4.301 | 2.927 | 3.443 | 3.642 | 4.284 | 6.311 | 7.425 | 5.553 | 6.533 | ns |
| | Medium fast | 3.437 | 4.044 | 2.731 | 3.213 | 3.42 | 4.023 | 6.182 | 7.273 | 5.435 | 6.394 | ns |
| | Fast | 3.41 | 4.012 | 2.715 | 3.193 | 3.393 | 3.991 | 6.178 | 7.269 | 5.425 | 6.383 | ns |
| 10 mA | Slow | 4.029 | 4.74 | 3.238 | 3.809 | 4.015 | 4.723 | 6.732 | 7.921 | 5.965 | 7.018 | ns |
| | Medium | 3.601 | 4.237 | 2.867 | 3.372 | 3.586 | 4.218 | 6.473 | 7.615 | 5.669 | 6.669 | ns |
| | Medium fast | 3.384 | 3.981 | 2.672 | 3.143 | 3.365 | 3.958 | 6.351 | 7.471 | 5.55 | 6.529 | ns |
| | Fast | 3.357 | 3.949 | 2.655 | 3.123 | 3.338 | 3.927 | 6.345 | 7.464 | 5.54 | 6.518 | ns |
| 12 mA | Slow | 3.974 | 4.675 | 3.196 | 3.759 | 3.958 | 4.656 | 6.842 | 8.049 | 6.068 | 7.139 | ns |
| | Medium | 3.55 | 4.176 | 2.827 | 3.326 | 3.534 | 4.157 | 6.584 | 7.746 | 5.751 | 6.766 | ns |
| | Medium fast | 3.345 | 3.935 | 2.638 | 3.103 | 3.325 | 3.911 | 6.488 | 7.633 | 5.641 | 6.637 | ns |
| | Fast | 3.316 | 3.902 | 2.621 | 3.083 | 3.297 | 3.878 | 6.486 | 7.63 | 5.626 | 6.619 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 71 •*** **LVCMOS 1.5 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2 mA | Slow | 4.423 | 5.203 | 5.397 | 6.35 | 5.686 | 6.69 | 5.609 | 6.599 | 5.561 | 6.542 | ns |
| 4 mA | Slow | 4.05 | 4.765 | 4.503 | 5.298 | 4.92 | 5.788 | 7.358 | 8.657 | 6.525 | 7.677 | ns |
| 6 mA | Slow | 4.081 | 4.801 | 4.259 | 5.012 | 4.699 | 5.528 | 7.659 | 9.011 | 6.709 | 7.893 | ns |
| 8 mA | Slow | 4.234 | 4.98 | 4.068 | 4.786 | 4.521 | 5.319 | 8.218 | 9.668 | 7.05 | 8.294 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 112 •*** **SSTL2 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

| | On-Die Termination (ODT) | $T_{PY}$ | | |
|---|---|---|---|---|
| | | –1 | –Std | Unit |
| Pseudo differential | None | 2.798 | 3.293 | ns |
| True differential | None | 2.733 | 3.215 | ns |

***Table 113 •*** **DDR1/SSTL2 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

| | On-Die Termination (ODT) | $T_{PY}$ | | |
|---|---|---|---|---|
| | | –1 | –Std | Unit |
| Pseudo differential | None | 2.476 | 2.913 | ns |
| True differential | None | 2.475 | 2.911 | ns |

***Table 114 •*** **SSTL2 Class I Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 2.26 | 2.66 | 1.99 | 2.341 | 1.985 | 2.335 | 2.135 | 2.512 | 2.13 | 2.505 | ns |
| Differential | 2.26 | 2.658 | 2.202 | 2.591 | 2.201 | 2.589 | 2.393 | 2.815 | 2.392 | 2.814 | ns |

***Table 115 •*** **DDR1/SSTL2 Class I Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 2.055 | 2.417 | 2.037 | 2.396 | 2.03 | 2.388 | 2.068 | 2.433 | 2.061 | 2.425 | ns |
| Differential | 2.192 | 2.58 | 2.434 | 2.864 | 2.425 | 2.852 | 2.164 | 2.545 | 2.156 | 2.536 | ns |

***Table 116 •*** **DDR1/SSTL2 Class I Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 1.512 | 1.779 | 1.462 | 1.72 | 1.462 | 1.72 | 1.676 | 1.972 | 1.676 | 1.971 | ns |
| Differential | 1.676 | 1.971 | 1.774 | 2.087 | 1.766 | 2.077 | 1.854 | 2.181 | 1.845 | 2.171 | ns |

***Table 117 •*** **DDR1/SSTL2 Class II Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 2.122 | 2.497 | 1.906 | 2.243 | 1.902 | 2.237 | 2.061 | 2.424 | 2.056 | 2.418 | ns |
| Differential | 2.127 | 2.501 | 2.042 | 2.402 | 2.043 | 2.403 | 2.363 | 2.78 | 2.365 | 2.781 | ns |

***Table 144 •*** **LPDDR AC Differential Voltage Specifications (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| AC input differential voltage | $V_{DIFF}$ | 0.6 × $V_{DDI}$ | | V |
| AC differential cross point voltage | $V_x$ | 0.4 × $V_{DDI}$ | 0.6 × $V_{DDI}$ | V |

***Table 145 •*** **LPDDR AC Specifications (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | 400 | Mbps | AC loading: per JEDEC specifications |

***Table 146 •*** **LPDDR AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Typ | Unit | Conditions |
|---|---|---|---|---|
| Supported output driver calibrated impedance | $R_{REF}$ | 20, 42 | Ω | Reference resistor = 150 Ω |
| Effective impedance value (ODT) | $R_{TT}$ | 50, 70, 150 | Ω | Reference resistor = 150 Ω |

***Table 147 •*** **LPDDR AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.9 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for LPDDR ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | Ω |

**AC Switching Characteristics**

Worst-case commercial conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, worst-case $V_{DDI}$.

***Table 148 •*** **LPDDR Receiver Characteristics for DDRIO I/O Bank with Fixed Codes**

| | | $T_{PY}$ | | |
|---|---|---|---|---|
| | On-Die Termination (ODT) | –1 | –Std | Unit |
| Pseudo differential | None | 1.568 | 1.845 | ns |
| True differential | None | 1.588 | 1.869 | ns |

***Table 149 •*** **LPDDR Reduced Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ENZL}$ | | $T_{ENZH}$ | | $T_{ENHZ}$ | | $T_{ENLZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 2.383 | 2.804 | 2.23 | 2.623 | 2.229 | 2.622 | 2.202 | 2.591 | 2.201 | 2.59 | ns |
| Differential | 2.396 | 2.819 | 2.764 | 3.252 | 2.764 | 3.252 | 2.255 | 2.653 | 2.255 | 2.653 | ns |

**Table 185 • M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

**Table 186 • M-LVDS Differential Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Differential output voltage swing (for MSIO I/O bank only) | $V_{OD}$ | 300 | 650 | mV |
| Output common mode voltage (for MSIO I/O bank only) | $V_{OCM}$ | 0.3 | 2.1 | V |
| Input common mode voltage | $V_{ICM}$ | 0.3 | 1.2 | V |
| Input differential voltage | $V_{ID}$ | 50 | 2400 | mV |

**Table 187 • M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | 500 | Mbps | AC loading: 2 pF / 100 Ω differential load |

**Table 188 • M-LVDS AC Impedance Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Termination resistance | $R_T$ | 50 | Ω |

**Table 189 • M-LVDS AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | Cross point | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V

**Table 190 • M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| On-Die Termination (ODT) | –1 | –Std | Unit |
| None | 2.738 | 3.221 | ns |
| 100 | 2.735 | 3.218 | ns |

**Table 191 • M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.495 | 2.934 | ns |
| 100 | 2.495 | 2.935 | ns |

**Table 192 • M-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2.258 | 2.656 | 2.348 | 2.762 | 2.334 | 2.746 | 2.123 | 2.497 | 2.125 | 2.5 | ns |

### 2.3.7.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

**Mini-LVDS Minimum and Maximum Input and Output Levels**

**Table 193 • Mini-LVDS Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

**Table 194 • Mini-LVDS DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC Input voltage | $V_I$ | 0 | 2.925 | V |

**Table 195 • Mini-LVDS DC Output Voltage Specification**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

**Table 196 • Mini-LVDS DC Differential Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Differential output voltage swing | $V_{OD}$ | 300 | 600 | mV |
| Output common mode voltage | $V_{OCM}$ | 1 | 1.4 | V |
| Input common mode voltage | $V_{ICM}$ | 0.3 | 1.2 | V |
| Input differential voltage | $V_{ID}$ | 100 | 600 | mV |

**Table 197 • Mini-LVDS Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 520 | Mbps | AC loading: 2 pF / 100 Ω differential load |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 700 | Mbps | AC loading: 2 pF / 100 Ω differential load |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V.

***Table 210 •*** **RSDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.855 | 3.359 | ns |
| 100 | 2.85 | 3.353 | ns |

***Table 211 •*** **RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.602 | 3.061 | ns |
| 100 | 2.597 | 3.055 | ns |

***Table 212 •*** **RSDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2.097 | 2.467 | 2.303 | 2.709 | 2.291 | 2.695 | 1.961 | 2.307 | 1.947 | 2.29 | ns |

***Table 213 •*** **RSDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| No pre-emphasis | 1.614 | 1.899 | 1.559 | 1.834 | 1.55 | 1.823 | 1.59 | 1.87 | 1.575 | 1.852 | ns |
| Min pre-emphasis | 1.604 | 1.887 | 1.742 | 2.05 | 1.728 | 2.032 | 1.889 | 2.222 | 1.858 | 2.185 | ns |
| Med pre-emphasis | 1.521 | 1.79 | 1.753 | 2.062 | 1.737 | 2.043 | 1.9 | 2.235 | 1.868 | 2.197 | ns |
| Max pre-emphasis | 1.492 | 1.754 | 1.762 | 2.073 | 1.745 | 2.052 | 1.91 | 2.247 | 1.876 | 2.206 | ns |

### *2.3.7.6 LVPECL*

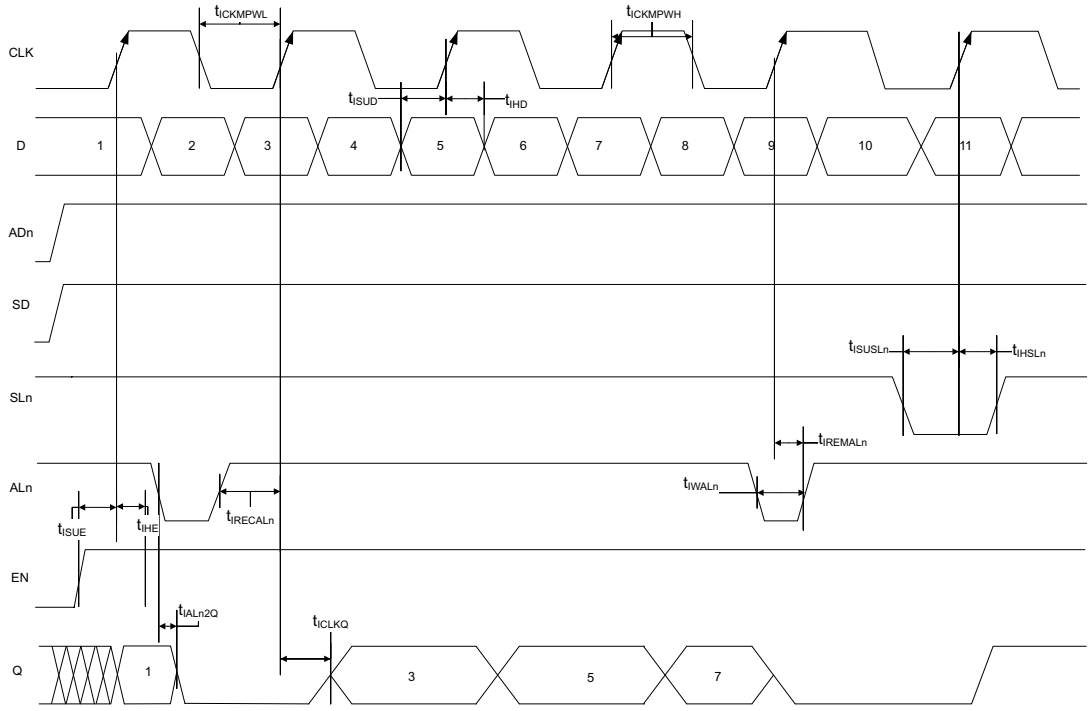
Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

**Minimum and Maximum Input and Output Levels (Applicable to MSIO I/O Bank Only)**

***Table 214 •*** **LVPECL Recommended DC Operating Conditions**

| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 3.15 | 3.3 | 3.45 | V |

***Figure 7 •*** **I/O Register Input Timing Diagram**



### 2.3.10.2 Timing Characteristics

The following table lists the combinatorial cell propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

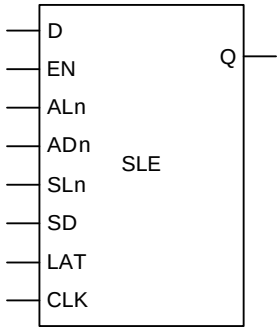
***Table 223 •*** **Combinatorial Cell Propagation Delays**

| Combinatorial Cell | Equation | Symbol | –1 | –Std | Unit |
|---|---|---|---|---|---|
| INV | Y = !A | $T_{PD}$ | 0.1 | 0.118 | ns |
| AND2 | Y = A · B | $T_{PD}$ | 0.164 | 0.193 | ns |
| NAND2 | Y = !(A · B) | $T_{PD}$ | 0.147 | 0.173 | ns |
| OR2 | Y = A + B | $T_{PD}$ | 0.164 | 0.193 | ns |
| NOR2 | Y = !(A + B) | $T_{PD}$ | 0.147 | 0.173 | ns |
| XOR2 | Y = A ⊕ B | $T_{PD}$ | 0.164 | 0.193 | ns |
| XOR3 | Y = A ⊕ B ⊕ C | $T_{PD}$ | 0.225 | 0.265 | ns |
| AND3 | Y = A · B · C | $T_{PD}$ | 0.209 | 0.246 | ns |
| AND4 | Y = A · B · C · D | $T_{PD}$ | 0.287 | 0.338 | ns |

### 2.3.10.3 Sequential Module

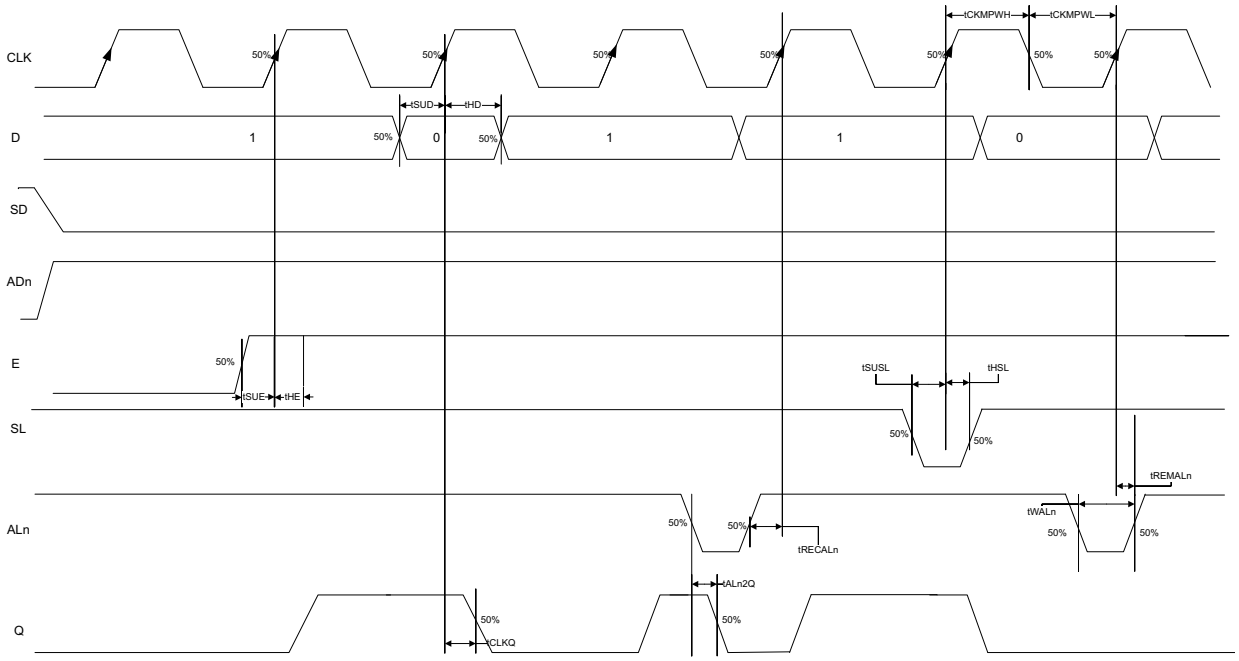
IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

***Figure 15 •*** **Sequential Module**



The following figure shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

***Figure 16 •*** **Sequential Module Timing Diagram**




## 2.3.10.3.1 Timing Characteristics

The following table lists the register delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 224 •*** **Register Delays**

| Parameter | Symbol | –1 | –Std | Unit |
|---|---|---|---|---|
| Clock-to-Q of the core register | $T_{CLKQ}$ | 0.108 | 0.127 | ns |
| Data setup time for the core register | $T_{SUD}$ | 0.254 | 0.298 | ns |
| Data hold time for the core register | $T_{HD}$ | 0 | 0 | ns |
| Enable setup time for the core register | $T_{SUE}$ | 0.335 | 0.394 | ns |
| Enable hold time for the core register | $T_{HE}$ | 0 | 0 | ns |
| Synchronous load setup time for the core register | $T_{SUSL}$ | 0.335 | 0.394 | ns |
| Synchronous load hold time for the core register | $T_{HSL}$ | 0 | 0 | ns |
| Asynchronous Clear-to-Q of the core register (ADn = 1) | $T_{ALN2Q}$ | 0.473 | 0.556 | ns |
| Asynchronous preset-to-Q of the core register (ADn = 0) | | 0.451 | 0.531 | ns |
| Asynchronous load removal time for the core register | $T_{REMALN}$ | 0 | 0 | ns |
| Asynchronous load recovery time for the core register | $T_{RECALN}$ | 0.353 | 0.415 | ns |
| Asynchronous load minimum pulse width for the core register | $T_{WALN}$ | 0.266 | 0.313 | ns |
| Clock minimum pulse width high for the core register | $T_{CKMPWH}$ | 0.065 | 0.077 | ns |
| Clock minimum pulse width low for the core register | $T_{CKMPWL}$ | 0.139 | 0.164 | ns |

**Table 254 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only) *(continued)***

| M2S/M2GL Device | Auto Programming 100 kHz | Auto Update 25 MHz | Programming Recovery 12.5 MHz | Unit |
|---|---|---|---|---|
| 150 | 161 | 161 | 161 | Sec |

**Table 255 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

| M2S/M2GL Device | Auto Programming 100 kHz | Auto Update 25 MHz | Programming Recovery 12.5 MHz | Unit |
|---|---|---|---|---|
| 005 | 47 | 27 | 28 | Sec |
| 010 | 77 | 35 | 35 | Sec |
| 025 | 150 | 42 | 41 | Sec |
| 050 | 33[1] | Not Supported | Not Supported | Sec |
| 060 | 291 | 83 | 82 | Sec |
| 090 | 427 | 109 | 108 | Sec |
| 150 | 708 | 157 | 160 | Sec |
| 005 | 41 | 48 | 49 | Sec |
| 010 | 86 | 87 | 87 | Sec |
| 025 | 87 | 85 | 86 | Sec |
| 050 | 85 | Not Supported | Not Supported | Sec |
| 060 | 78 | 86 | 86 | Sec |
| 090 | 154 | 162 | 162 | Sec |
| 150 | 161 | 161 | 161 | Sec |
| 005 | 87 | 67 | 66 | Sec |
| 010 | 161 | 113 | 113 | Sec |
| 025 | 229 | 120 | 121 | Sec |
| 050 | 112 | Not Supported | Not Supported | Sec |
| 060 | 368 | 161 | 158 | Sec |
| 090 | 582 | 261 | 260 | Sec |
| 150 | 867 | 309 | 310 | Sec |

1. Auto Programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

The following table lists the programming times in worst-case conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V. External SPI flash part# AT25DF641-s3H is used during this measurement.

***Table 256 •*** **JTAG Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 302672 | 44 | 10 | Sec |
| 010 | 568784 | 50 | 18 | Sec |
| 025 | 1223504 | 73 | 26 | Sec |
| 050 | 2424832 | 88 | 54 | Sec |
| 060 | 2418896 | 99 | 54 | Sec |
| 090 | 3645968 | 135 | 126 | Sec |
| 150 | 6139184 | 177 | 193 | Sec |

***Table 257 •*** **JTAG Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 137536 | 61 | 4 | Sec |
| 010 | 274816 | 100 | 9 | Sec |
| 025 | 274816 | 100 | 9 | Sec |
| 050 | 2,78,528 | 106 | 8 | Sec |
| 060 | 268480 | 98 | 8 | Sec |
| 090 | 544496 | 176 | 15 | Sec |
| 150 | 544496 | 177 | 15 | Sec |

***Table 258 •*** **JTAG Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 439296 | 71 | 11 | Sec |
| 010 | 842688 | 129 | 20 | Sec |
| 025 | 1497408 | 142 | 35 | Sec |
| 050 | 2695168 | 184 | 59 | Sec |
| 060 | 2686464 | 180 | 70 | Sec |
| 090 | 4190208 | 288 | 147 | Sec |
| 150 | 6682768 | 338 | 231 | Sec |

***Table 276 •*** **Cryptographic Block Characteristics *(continued)***

| Service | Conditions | Timing | Unit |
|---|---|---|---|
| SHA256 | 512 bits | 540 | kbps |
| | 1024 bits | 780 | kbps |
| | 2048 bits | 950 | kbps |
| | 24 kbits | 1140 | kbps |
| HMAC | 512 bytes | 820 | kbps |
| | 1024 bytes | 890 | kbps |
| | 2048 bytes | 930 | kbps |
| | 24 kbytes | 980 | kbps |
| KeyTree | | 1.8 | ms |
| Challenge-response | PUF = OFF | 25 | ms |
| | PUF = ON | 7 | ms |
| ECC point multiplication | | 590 | ms |
| ECC point addition | | 8 | ms |

1. Using cypher block chaining (CBC) mode.

## 2.3.19 Crystal Oscillator

The following table describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

***Table 277 •*** **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 20 | | MHz | |
| Accuracy | ACCXTAL | | | 0.0047 | % | 005, 010, 025, 050, 060, and 090 devices |
| | | | | 0.0058 | % | 150 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 200 | 300 | ps | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 200 | 300 | ps | 010, 025, 050, and 060 devices |
| | | | 250 | 410 | ps | 150 devices |
| | | | 250 | 550 | ps | 005 and 090 devices |
| Operating current | IDYNXTAL | | 1.5 | | mA | 010, 050, and 060 devices |
| | | | 1.65 | | mA | 005, 025, 090, and 150 devices |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |

## 2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 308 •*** **MMUART Characteristics**

| Parameter | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| FMMUART_REF_CLK | Internally sourced MMUART reference clock frequency. | 166 | 142 | MHz |
| BAUDMMUARTTx | Maximum transmit baud rate | 10.375 | 8.875 | Mbps |
| BAUDMMUARTRx | Maximum receive baud rate | 10.375 | 8.875 | Mbps |

## 2.3.35 IGLOO2 Specifications

### 2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 309 •*** **Maximum Frequency for HPMS Main Clock**

| Symbol | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| HPMS_CLK | Maximum frequency for the HPMS main clock | 166 | 142 | MHz |

### 2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, see Figure 23, page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 310 •*** **SPI Characteristics for All Devices**

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| SPIFMAX | Maximum operating frequency of SPI interface | | | 20 | MHz | |
| sp1 | SPI_[0\|1]_CLK minimum period | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 12 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 48.2 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.1 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.19 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.39 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.77 | | | µs | |

***Table 310 •*** **SPI Characteristics for All Devices *(continued)***

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| SPI master configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 7.0 | | | ns | |
| sp7m | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) – 9.5 | | | ns | |
| sp8m | SPI_[0\|1]_DI setup time[2] | 15 | | | ns | |
| sp9m | SPI_[0\|1]_DI hold time[2] | –2.5 | | | ns | |
| SPI slave configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 16.0 | | | ns | |
| sp7s | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) - 3.5 | | | ns | |
| sp8s | SPI_[0\|1]_DI setup time[2] | 3 | | | ns | |
| sp9s | SPI_[0\|1]_DI hold time[2] | 2.5 | | | ns | |

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. For allowable pclk configurations, see the Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

***Figure 23 •*** **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**