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#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

| Product Status                 | Active  |
|--------------------------------|---|
| Number of LABs/CLBs            | -   |
| Number of Logic Elements/Cells | 146124  |
| Total RAM Bits                 | 5120000   |
| Number of I/O                  | 248   |
| Number of Gates                | -   |
| Voltage - Supply               | 1.14V ~ 2.625V  |
| Mounting Type                  | Surface Mount   |
| Operating Temperature          | 0°C ~ 85°C (TJ)   |
| Package / Case                 | 484-BFBGA   |
| Supplier Device Package        | 484-FBGA (19x19)  |
| Purchase URL                   | https://www.e-xfl.com/product-detail/microchip-technology/m2gl150t-fcv484 |
|                                |   |

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Power Matters."

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1. For flash programming and retention maximum limits, see Table 5, page 7. For recommended operating conditions, see Table 4, page 6.

 Table 4 •
 Recommended Operating Conditions

| Parameter   | Symbol                          | Min   | Тур | Max   | Unit | Conditions  |
|---|---------------------------------|-------|-----|-------|------|-------------|
| Operating junction temperature  | TJ                              | 0     | 25  | 85    | °C   | Commercial  |
|   |                                 | -40   | 25  | 100   | °C   | Industrial  |
| Programming junction temperatures <sup>1</sup>  | TJ                              | 0     | 25  | 85    | °C   | Commercial  |
|   |                                 | -40   | 25  | 100   | °C   | Industrial  |
| DC core supply voltage.<br>Must always power this pin.  | V <sub>DD</sub>                 | 1.14  | 1.2 | 1.26  | V    |             |
| Power supply for charge pumps   | V <sub>PP</sub>                 | 2.375 | 2.5 | 2.625 | V    | 2.5 V range |
| (for normal operation and<br>programming) for the 005, 010,<br>025, 050, 060 devices                                |                                 | 3.15  | 3.3 | 3.45  | V    | 3.3 V range |
| Power supply for charge pumps (for<br>normal operation and programming)<br>for the 090 and 150 devices              | V <sub>PP</sub>                 | 3.15  | 3.3 | 3.45  | V    | 3.3 V range |
| Analog power pad for MDDR PLL   | MSS_MDDR_PLL_VDDA               | 2.375 | 2.5 | 2.625 | V    | 2.5 V range |
|   |                                 | 3.15  | 3.3 | 3.45  | V    | 3.3 V range |
| Analog power pad for MDDR PLL   | HPMS_MDDR_PLL_VDDA              | 2.375 | 2.5 | 2.625 | V    | 2.5 V range |
|   |                                 | 3.15  | 3.3 | 3.45  | V    | 3.3 V range |
| Analog power pad for FDDR PLL   | FDDR_PLL_VDDA                   | 2.375 | 2.5 | 2.625 | V    | 2.5 V range |
|   |                                 | 3.15  | 3.3 | 3.45  | V    | 3.3 V range |
| Analog power pad for MDDR PLL   | PLL0_PLL1_MSS_MDDR_V            | 2.375 | 2.5 | 2.625 | V    | 2.5 V range |
|   | DDA                             | 3.15  | 3.3 | 3.45  | V    | 3.3 V range |
| Analog power pad for MDDR PLL   | PLL0_PLL1_HPMS_MDDR_            | 2.375 | 2.5 | 2.625 | V    | 2.5 V range |
|   | VDDA                            | 3.15  | 3.3 | 3.45  | V    | 3.3 V range |
| Analog power pad for PLL0 to PLL5   | CCC_XX[01]_PLL_VDDA             | 2.375 | 2.5 | 2.625 | V    | 2.5 V range |
|   |                                 | 3.15  | 3.3 | 3.45  | V    | 3.3 V range |
| High supply voltage for PLL   | SERDES_[01]_PLL_VDDA            | 2.375 | 2.5 | 2.625 | V    | 2.5 V range |
| SerDes[01]  |                                 | 3.15  | 3.3 | 3.45  | V    | 3.3 V range |
| Analog power for SerDes[01] PLL<br>Lane 0 to Lane 3. This is a 2.5 V<br>SerDes internal PLL supply.                 | SERDES_[01]_L[0123]_VD<br>DAPLL | 2.375 | 2.5 | 2.625 | V    |             |
| TX/RX analog I/O voltage. Low<br>voltage power for the lanes of<br>SerDesIF0. This is a 1.2 V SerDes<br>PMA supply. | SERDES_[01]_L[0123]_VD<br>DAIO  | 1.14  | 1.2 | 1.26  | V    |             |
| PCIe/PCS power supply   | SERDES_[01]_VDD                 | 1.14  | 1.2 | 1.26  | V    |             |
| 1.2 V DC supply voltage   | V <sub>DDIx</sub>               | 1.14  | 1.2 | 1.26  | V    |             |
| 1.5 V DC supply voltage   | V <sub>DDIx</sub>               | 1.425 | 1.5 | 1.575 | V    |             |
| 1.8 V DC supply voltage   | V <sub>DDIx</sub>               | 1.71  | 1.8 | 1.89  | V    |             |
| 2.5 V DC supply voltage   | V <sub>DDIx</sub>               | 2.375 | 2.5 | 2.625 | V    |             |



Figure 1 • High Temperature Data Retention (HTR)



## 2.3.1.1 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to  $V_{CCI}$  + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

**Note:** The above specifications do not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant with the PCI standard including the PCI overshoot/undershoot specifications.

## 2.3.1.2 Thermal Characteristics

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ1 through EQ3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

$$\theta_{\rm JC} = \frac{T_{\rm J} - T_{\rm C}}{P}$$

EQ 3



## 2.3.2 Power Consumption

The following sections describe the power consumptions of the devices.

## 2.3.2.1 Quiescent Supply Current

#### Table 10 • Quiescent Supply Current Characteristics

|   | Modes and Configurations |              |  |  |  |  |
|---|--------------------------|--------------|--|--|--|--|
| Power Supplies/Blocks   | Non-Flash*Freeze         | Flash*Freeze |  |  |  |  |
| FPGA Core   | On                       | Off          |  |  |  |  |
| V <sub>DD</sub> /SERDES_[01]_VDD <sup>1</sup>   | On                       | On           |  |  |  |  |
| V <sub>PP</sub> /V <sub>PPNVM</sub>   | On                       | On           |  |  |  |  |
| HPMS_MDDR_PLL_VDDA/FDDR_PLL_VDDA/<br>CCC_XX[01]_PLL_VDDA/PLL0_PLL1_HPMS_MDDR_VDD<br>A | 0 V                      | 0 V          |  |  |  |  |
| SERDES_[01]_PLL_VDDA <sup>2</sup>   | 0 V                      | 0 V          |  |  |  |  |
| SERDES_[01]_L[0123]_VDDAPLL/VDD_2V5 <sup>2</sup>                                      | On                       | On           |  |  |  |  |
| SERDES_[01]_L[0123]_VDDAIIO <sup>2</sup>  | On                       | On           |  |  |  |  |
| V <sub>DDlx</sub> <sup>3, 4</sup>   | On                       | On           |  |  |  |  |
| V <sub>REFx</sub>   | On                       | On           |  |  |  |  |
| MSSDDR CLK  | 32 kHz                   | 32 kHz       |  |  |  |  |
| RAM   | On                       | Sleep state  |  |  |  |  |
| System controller   | 50 MHz                   | 50 MHz       |  |  |  |  |
| 50 MHz oscillator (enable/disable)  | Enable                   | Disabled     |  |  |  |  |
| 1 MHz oscillator (enable/disable)   | Disabled                 | Disabled     |  |  |  |  |
| Crystal oscillator (enable/disable)   | Disabled                 | Disabled     |  |  |  |  |

1. SERDES\_[01]\_VDD Power Supply is shorted to  $V_{DD}$ .

2. SerDes and DDR blocks to be unused.

3. V<sub>DDIx</sub> has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate V<sub>DDI</sub> bank supplies. For details on bank power supplies, see "Recommendation for Unused Bank Supplies" table in the *AC393: SmartFusion2 and IGLO02 Board Design Guidelines Application Note.* 

4. No Differential (that is to say, LVDS) I/Os or ODT attributes to be used.

#### Table 11 • SmartFusion2 and IGLOO2 Quiescent Supply Current (V<sub>DD</sub> = 1.2 V) – Typical Process

| Symbol | Modes                | 005  | 010  | 025  | 050   | 060   | 090   | 150   | Unit | Conditions                              |
|--------|----------------------|------|------|------|-------|-------|-------|-------|------|---|
| IDC1   | Non-<br>Flash*Freeze | 6.2  | 6.9  | 8.9  | 13.1  | 15.3  | 15.4  | 27.5  | mA   | Typical<br>(T <sub>J</sub> = 25 °C)     |
|        |                      | 24.0 | 28.4 | 40.6 | 67.8  | 80.6  | 81.4  | 144.7 | mA   | Commercial<br>(T <sub>J</sub> = 85 °C)  |
|        |                      | 35.2 | 41.9 | 60.5 | 102.1 | 121.4 | 122.6 | 219.1 | mA   | Industrial<br>(T <sub>J</sub> = 100 °C) |



## 2.3.5.2 Output Buffer and AC Loading

The following figure shows the output buffer and AC loading.

#### Figure 4 • Output Buffer AC Loading



Voltage-Referenced, Singled-Ended I/O Test Setup



Differential I/O Test Setup





# Table 22 • Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions

| 1/0        | MSIO | MSIOD | DDRIO | Unit |
|------------|------|-------|-------|------|
| LPDDR      |      |       | 200   | MHz  |
| HSTL1.5 V  |      |       | 200   | MHz  |
| SSTL 2.5 V | 255  | 350   | 200   | MHz  |
| SSTL 1.8 V |      |       | 334   | MHz  |
| SSTL 1.5 V |      |       | 334   | MHz  |

# Table 23 • Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions Industrial Conditions

| I/O                 | MSIO  | MSIOD | Unit |
|---------------------|-------|-------|------|
| LVPECL (input only) | 450   |       | MHz  |
| LVDS 3.3 V          | 267.5 |       | MHz  |
| LVDS 2.5 V          | 267.5 | 350   | MHz  |
| RSDS                | 260   | 350   | MHz  |
| BLVDS               | 250   |       | MHz  |
| MLVDS               | 250   |       | MHz  |
| Mini-LVDS           | 260   | 350   | MHz  |



| Output           |         | Т     | DP    |       | ZL    |       | Г <sub>ZH</sub> | Т     | HZ <sup>1</sup> | Т     | LZ <sup>1</sup> | _    |
|------------------|---------|-------|-------|-------|-------|-------|-----------------|-------|-----------------|-------|-----------------|------|
| Selection Contro | Control | -1    | -Std  | -1    | -Std  | -1    | -Std            | -1    | -Std            | -1    | -Std            | Unit |
| 2 mA             | Slow    | 2.735 | 3.218 | 3.371 | 3.966 | 3.618 | 4.257           | 6.03  | 7.095           | 5.705 | 6.712           | ns   |
| 4 mA             | Slow    | 2.426 | 2.854 | 2.992 | 3.521 | 3.221 | 3.79            | 6.738 | 7.927           | 6.298 | 7.41            | ns   |
| 6 mA             | Slow    | 2.433 | 2.862 | 2.81  | 3.306 | 3.031 | 3.566           | 7.123 | 8.38            | 6.596 | 7.76            | ns   |

#### Table 72 • LVCMOS 1.5 V Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

#### 2.3.5.10 1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-12A.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

#### Table 73 • LVCMOS 1.2 V DC Recommended DC Operating Conditions

| Parameter      | Symbol           | Min   | Тур | Max  | Unit |
|----------------|------------------|-------|-----|------|------|
| Supply voltage | V <sub>DDI</sub> | 1.140 | 1.2 | 1.26 | V    |

#### Table 74 • LVCMOS 1.2 V DC Input Voltage Specification

| Parameter   | Symbol               | Min                     | Max                   | Unit |
|---|----------------------|-------------------------|-----------------------|------|
| DC input logic high (for<br>MSIOD and DDRIO I/O<br>banks) | V <sub>IH</sub> (DC) | 0.65 × V <sub>DDI</sub> | 1.26                  | V    |
| DC input logic high (for<br>MSIO I/O bank)                | V <sub>IH</sub> (DC) | 0.65 × V <sub>DDI</sub> | 3.45                  | V    |
| DC input logic low  | V <sub>IL</sub> (DC) | -0.3                    | $0.35 \times V_{DDI}$ | V    |
| Input current high <sup>1</sup>                           | I <sub>IH</sub> (DC) |                         |                       |      |
| Input current low <sup>1</sup>                            | I <sub>IL</sub> (DC) |                         |                       |      |

1. See Table 24, page 22.

#### Table 75 • LVCMOS 1.2 V DC Output Voltage Specification

| Parameter            | Symbol          | Min                   | Max                     | Unit |
|----------------------|-----------------|-----------------------|-------------------------|------|
| DC output logic high | V <sub>OH</sub> | $V_{DDI} \times 0.75$ |                         | V    |
| DC output logic low  | V <sub>OL</sub> |                       | V <sub>DDI</sub> × 0.25 | V    |

#### Table 76 • LVCMOS 1.2 V Minimum and Maximum AC Switching Speed

| Parameter                              | Symbol           | Max | Unit | Conditions                                 |
|--|------------------|-----|------|--|
| Maximum data rate (for DDRIO I/O bank) | D <sub>MAX</sub> | 200 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank)  | D <sub>MAX</sub> | 120 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank) | D <sub>MAX</sub> | 160 | Mbps | AC loading: 17 pF load, maximum drive/slew |



#### **AC Switching Characteristics**

Worst commercial-case conditions:  $T_J$  = 85 °C,  $V_{DD}$  = 1.14 V,  $V_{DDI}$  = 3.0 V

 
 Table 91 •
 PCI/PCIX AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)

|                          | -     | Г <sub>РҮ</sub> | Т     | PYS   |      |
|--------------------------|-------|-----------------|-------|-------|------|
| On-Die Termination (ODT) | -1    | -Std            | -1    | -Std  | Unit |
| None                     | 2.229 | 2.623           | 2.238 | 2.633 | ns   |

 Table 92 •
 PCI/PCIX AC switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)

| T     | DP    | Т     | ZL    | Tz    | ZH    | T     | HZ    | Т     | LZ    |      |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|------|
| -1    | -Std  | Unit |
| 2.146 | 2.525 | 2.043 | 2.404 | 2.084 | 2.452 | 6.095 | 7.171 | 5.558 | 6.539 | ns   |

### 2.3.6 Memory Interface and Voltage Referenced I/O Standards

This section describes High-Speed Transceiver Logic (HSTL) memory interface and voltage reference I/O standards.

#### 2.3.6.1 High-Speed Transceiver Logic (HSTL)

The HSTL standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO2 FPGA and SmartFusion2 SoC FPGA devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification (Applicable to DDRIO Bank Only)

| Table 93 • | HSTL Recommended DO | 0 0 | perating | Conditions |
|------------|---------------------|-----|----------|------------|
|------------|---------------------|-----|----------|------------|

| Parameter               | Symbol           | Min   | Тур   | Max   | Unit |
|-------------------------|------------------|-------|-------|-------|------|
| Supply voltage          | V <sub>DDI</sub> | 1.425 | 1.5   | 1.575 | V    |
| Termination voltage     | V <sub>TT</sub>  | 0.698 | 0.750 | 0.803 | V    |
| Input reference voltage | V <sub>REF</sub> | 0.698 | 0.750 | 0.803 | V    |

#### Table 94 • HSTL DC Input Voltage Specification

| Parameter                       | Symbol               | Min                    | Max                    | Unit |
|---------------------------------|----------------------|------------------------|------------------------|------|
| DC input logic high             | V <sub>IH</sub> (DC) | V <sub>REF</sub> + 0.1 | 1.575                  | V    |
| DC input logic low              | V <sub>IL</sub> (DC) | -0.3                   | V <sub>REF</sub> – 0.1 | V    |
| Input current high <sup>1</sup> | I <sub>IH</sub> (DC) |                        |                        |      |
| Input current low <sup>1</sup>  | I <sub>IL</sub> (DC) |                        |                        |      |
|                                 |                      |                        |                        |      |

1. See Table 24, page 22.



#### Table 100 • HSTL AC Test Parameter Specification

| Parameter  | Symbol            | Тур  | Unit |
|--|-------------------|------|------|
| Measuring/trip point for data path   | V <sub>TRIP</sub> | 0.75 | V    |
| Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )         | R <sub>ENT</sub>  | 2K   | Ω    |
| Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ ) | C <sub>ENT</sub>  | 5    | pF   |
| Reference resistance for data test path for HSTL15 Class I ( $T_{DP}$ )          | RTT_TEST          | 50   | Ω    |
| Reference resistance for data test path for HSTL15 Class II ( $T_{DP}$ )         | RTT_TEST          | 25   | Ω    |
| Capacitive loading for data path (T <sub>DP</sub> )                              | C <sub>LOAD</sub> | 5    | pF   |

#### **AC Switching Characteristics**

Worst-case commercial conditions:  $T_J$  = 85 °C,  $V_{DD}$  = 1.14 V, worst-case  $V_{DDI}$ .

| Table 101 • | HSTL Rece | eiver Characteristic | s for DDRIO I/O | Bank with Fix | ed Code (Input Buffers |
|-------------|-----------|----------------------|-----------------|---------------|------------------------|
|-------------|-----------|----------------------|-----------------|---------------|------------------------|

|                     |                          |       | T <sub>PY</sub> |      |  |  |
|---------------------|--------------------------|-------|-----------------|------|--|--|
|                     | On-Die Termination (ODT) | -1    | -Std            | Unit |  |  |
| Pseudo differential | None                     | 1.605 | 1.888           | ns   |  |  |
|                     | 47.8                     | 1.614 | 1.898           | ns   |  |  |
| True differential   | None                     | 1.622 | 1.909           | ns   |  |  |
|                     | 47.8                     | 1.628 | 1.916           | ns   |  |  |

#### Table 102 • HSTL Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

|              | ٦     | Г <sub>DP</sub> |       | T <sub>ZL</sub> |          | Т <sub>ZH</sub> |       | т <sub>нz</sub> |       | T <sub>LZ</sub> |      |
|--------------|-------|-----------------|-------|-----------------|----------|-----------------|-------|-----------------|-------|-----------------|------|
|              | -1    | -Std            | -1    | -Std            | -1       | -Std            | –1    | -Std            | –1    | -Std            | Unit |
|              |       |                 |       | ŀ               | HSTL Cla | ss I            |       |                 |       |                 |      |
| Single-ended | 2.6   | 3.059           | 2.514 | 2.958           | 2.514    | 2.958           | 2.431 | 2.86            | 2.431 | 2.86            | ns   |
| Differential | 2.621 | 3.083           | 2.648 | 3.115           | 2.647    | 3.113           | 2.925 | 3.442           | 2.923 | 3.44            | ns   |
|              |       |                 |       | ŀ               | ISTL Cla | ss II           |       |                 |       |                 |      |
| Single-ended | 2.511 | 2.954           | 2.488 | 2.927           | 2.49     | 2.93            | 2.409 | 2.833           | 2.411 | 2.836           | ns   |
| Differential | 2.528 | 2.974           | 2.552 | 3.003           | 2.551    | 3.001           | 2.897 | 3.409           | 2.896 | 3.408           | ns   |

#### 2.3.6.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.



#### Table 107 • SSTL2 AC Differential Voltage Specifications

| Parameter                           | Symbol                 | Min                          | Мах                          | Unit |
|-------------------------------------|------------------------|------------------------------|------------------------------|------|
| AC input differential voltage       | V <sub>DIFF</sub> (AC) | 0.7                          |                              | V    |
| AC differential cross point voltage | V <sub>x</sub> (AC)    | 0.5 × V <sub>DDI</sub> – 0.2 | 0.5 × V <sub>DDI</sub> + 0.2 | V    |

#### Table 108 • SSTL2 Minimum and Maximum AC Switching Speeds

| Parameter                                 | Symbol           | Max | Unit | Conditions                           |
|---|------------------|-----|------|--------------------------------------|
| Maximum data rate (for<br>DDRIO I/O bank) | D <sub>MAX</sub> | 400 | Mbps | AC loading: per JEDEC specifications |
| Maximum data rate (for<br>MSIO I/O bank)  | D <sub>MAX</sub> | 575 | Mbps | AC loading: 17pF load                |
| Maximum data rate (for MSIOD I/O bank)    | D <sub>MAX</sub> | 700 | Mbps | AC loading: 3 pF / 50 $\Omega$ load  |
|   |                  | 510 | Mbps | AC loading: 17pF load                |

#### Table 109 • SSTL2 AC Impedance Specifications

| Parameter                          | Тур    | Unit | Conditions                        |
|------------------------------------|--------|------|-----------------------------------|
| Supported output driver calibrated | 20, 42 | Ω    | Reference resistor = 150 $\Omega$ |
| impedance (for DDRIO I/O bank)     |        |      |                                   |

#### Table 110 • DDR1/SSTL2 AC Test Parameter Specifications

| Parameter  | Symbol            | Тур  | Unit |
|--|-------------------|------|------|
| Measuring/trip point for data path                                       | V <sub>TRIP</sub> | 1.25 | V    |
| Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ ) | R <sub>ENT</sub>  | 2K   | Ω    |
| Capacitive loading for enable path $(T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})$    | C <sub>ENT</sub>  | 5    | pF   |
| Reference resistance for data test path for SSTL2 Class I $(T_{DP})$     | RTT_TEST          | 50   | Ω    |
| Reference resistance for data test path for SSTL2 Class II $(T_{DP})$    | RTT_TEST          | 25   | Ω    |
| Capacitive loading for data path (T <sub>DP</sub> )                      | C <sub>LOAD</sub> | 5    | pF   |

#### **AC Switching Characteristics**

Worst commercial-case conditions: T\_J = 85 °C, V\_{DD} = 1.14 V, V\_{DDI} = 2.375 V

| Table 111 • | SSTL2 Receiver | Characteristics | for DDR | IO I/O | Bank (Input | t Buffers) |
|-------------|----------------|-----------------|---------|--------|-------------|------------|
|-------------|----------------|-----------------|---------|--------|-------------|------------|

|                     | On-Die            |       |       |      |
|---------------------|-------------------|-------|-------|------|
|                     | Termination (ODT) | -1    | -Std  | Unit |
| Pseudo differential | None              | 1.549 | 1.821 | ns   |
| True differential   | None              | 1.589 | 1.87  | ns   |



# Table 185 • M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)

| Parameter            | Symbol          | Min  | Тур   | Max  | Unit |
|----------------------|-----------------|------|-------|------|------|
| DC output logic high | V <sub>OH</sub> | 1.25 | 1.425 | 1.6  | V    |
| DC output logic low  | V <sub>OL</sub> | 0.9  | 1.075 | 1.25 | V    |

#### Table 186 • M-LVDS Differential Voltage Specification

| Parameter  | Symbol           | Min | Max  | Unit |
|--|------------------|-----|------|------|
| Differential output voltage swing (for MSIO I/O bank only) | V <sub>OD</sub>  | 300 | 650  | mV   |
| Output common mode voltage (for MSIO I/O bank only)        | V <sub>OCM</sub> | 0.3 | 2.1  | V    |
| Input common mode voltage                                  | V <sub>ICM</sub> | 0.3 | 1.2  | V    |
| Input differential voltage                                 | V <sub>ID</sub>  | 50  | 2400 | mV   |

#### Table 187 • M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank

| Parameter         | Symbol           | Max | Unit | Conditions  |
|-------------------|------------------|-----|------|---|
| Maximum data rate | D <sub>MAX</sub> | 500 | Mbps | AC loading: 2 pF / 100 $\Omega$ differential load |

#### Table 188 • M-LVDS AC Impedance Specifications

| Parameter              | Symbol         | Тур | Unit |
|------------------------|----------------|-----|------|
| Termination resistance | R <sub>T</sub> | 50  | Ω    |

#### Table 189 • M-LVDS AC Test Parameter Specifications

| Parameter   | Symbol            | Тур         | Unit |
|---|-------------------|-------------|------|
| Measuring/trip point for data path  | V <sub>TRIP</sub> | Cross point | V    |
| Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )                                    | R <sub>ENT</sub>  | 2K          | Ω    |
| Capacitive loading for enable path (T <sub>ZH</sub> , T <sub>ZL</sub> , T <sub>HZ</sub> , T <sub>LZ</sub> ) | C <sub>ENT</sub>  | 5           | pF   |

#### **AC Switching Characteristics**

Worst commercial-case conditions:  $T_J$  = 85 °C,  $V_{DD}$  = 1.14 V,  $V_{DDI}$  = 2.375 V

#### Table 190 • M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank -Input Buffers)

|                          |       | T <sub>PY</sub> |      |  |
|--------------------------|-------|-----------------|------|--|
| On-Die Termination (ODT) | -1    | -Std            | Unit |  |
| None                     | 2.738 | 3.221           | ns   |  |
| 100                      | 2.735 | 3.218           | ns   |  |







The following table lists the output/enable propagation delays in worst commercial-case conditions when  $T_J$  = 85 °C,  $V_{DD}$  = 1.14 V.

| Table 220 • | Output/Enable Data | <b>Register Pr</b> | opagation Delays |
|-------------|--------------------|--------------------|------------------|
|-------------|--------------------|--------------------|------------------|

|  |                      | Measuring               |       |       |      |
|--|----------------------|-------------------------|-------|-------|------|
| Parameter  | Symbol               | (from, to) <sup>1</sup> | -1    | -Std  | Unit |
| Bypass delay of the output/enable register                           | T <sub>OBYP</sub>    | F, G or H, I            | 0.353 | 0.415 | ns   |
| Clock-to-Q of the output/enable register                             | T <sub>OCLKQ</sub>   | E, G or E, I            | 0.263 | 0.309 | ns   |
| Data setup time for the output/enable register                       | T <sub>OSUD</sub>    | A, E or J, E            | 0.19  | 0.223 | ns   |
| Data hold time for the output/enable register                        | T <sub>OHD</sub>     | A, E or J, E            | 0     | 0     | ns   |
| Enable setup time for the output/enable register                     | T <sub>OSUE</sub>    | B, E                    | 0.419 | 0.493 | ns   |
| Enable hold time for the output/enable register                      | T <sub>OHE</sub>     | B, E                    | 0     | 0     | ns   |
| Synchronous load setup time for the output/enable register           | T <sub>OSUSL</sub>   | D, E                    | 0.196 | 0.231 | ns   |
| Synchronous load hold time for the output/enable register            | T <sub>OHSL</sub>    | D, E                    | 0     | 0     | ns   |
| Asynchronous clear-to-q of the output/enable register (ADn = 1)      | T <sub>OALN2Q</sub>  | C, G or C, I            | 0.505 | 0.594 | ns   |
| Asynchronous preset-to-q of the output/enable register (ADn = 0)     | -                    | C, G or C, I            | 0.528 | 0.621 | ns   |
| Asynchronous load removal time for the output/enable register        | TOREMALN             | C, E                    | 0     | 0     | ns   |
| Asynchronous load recovery time for the output/enable register       | T <sub>ORECALN</sub> | C, E                    | 0.034 | 0.04  | ns   |
| Asynchronous load minimum pulse width for the output/enable register | T <sub>OWALN</sub>   | C, C                    | 0.304 | 0.357 | ns   |
| Clock minimum pulse width high for the output/enable register        | T <sub>OCKMPWH</sub> | E, E                    | 0.075 | 0.088 | ns   |
| Clock minimum pulse width low for the output/enable register         | TOCKMPWL             | E, E                    | 0.159 | 0.187 | ns   |

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.



### 2.3.9.4 Output DDR Module











#### 2.3.9.5 Timing Characteristics

The following table lists the output DDR propagation delays in worst commercial-case conditions when  $T_J$  = 85 °C,  $V_{DD}$  = 1.14 V.

|                        |  | Measuring Nodes |       |       |      |
|------------------------|--|-----------------|-------|-------|------|
| Symbol                 | Description                                    | (from, to)      | -1    | -Std  | Unit |
| T <sub>DDROCLKQ</sub>  | Clock-to-out of DDR for output DDR             | E, G            | 0.263 | 0.309 | ns   |
| T <sub>DDROSUDF</sub>  | Data_F data setup for output DDR               | F, E            | 0.143 | 0.168 | ns   |
| T <sub>DDROSUDR</sub>  | Data_R data setup for output DDR               | A, E            | 0.19  | 0.223 | ns   |
| T <sub>DDROHDF</sub>   | Data_F data hold for output DDR                | F, E            | 0     | 0     | ns   |
| T <sub>DDROHDR</sub>   | Data_R data hold for output DDR                | A, E            | 0     | 0     | ns   |
| T <sub>DDROSUE</sub>   | Enable setup for input DDR                     | B, E            | 0.419 | 0.493 | ns   |
| T <sub>DDROHE</sub>    | Enable hold for input DDR                      | B, E            | 0     | 0     | ns   |
| T <sub>DDROSUSLN</sub> | Synchronous load setup for input DDR           | D, E            | 0.196 | 0.231 | ns   |
| T <sub>DDROHSLN</sub>  | Synchronous load hold for input DDR            | D, E            | 0     | 0     | ns   |
| T <sub>DDROAL2Q</sub>  | Asynchronous load-to-out for output DDR        | C, G            | 0.528 | 0.621 | ns   |
| T <sub>DDROREMAL</sub> | Asynchronous load removal time for output DDR  | C, E            | 0     | 0     | ns   |
| T <sub>DDRORECAL</sub> | Asynchronous load recovery time for output DDR | C, E            | 0.034 | 0.04  | ns   |

#### Table 222 • Output DDR Propagation Delays



## Table 240 • µSRAM (RAM128x8) in 128 × 8 Mode (continued)

|   |                       | -      | ·1    | -8     | Std   |      |
|---|-----------------------|--------|-------|--------|-------|------|
| Parameter   | Symbol                | Min    | Max   | Min    | Max   | Unit |
| Read address hold time in synchronous mode  | T                     | 0.091  |       | 0.107  |       | ns   |
| Read address hold time in asynchronous mode   | - 'ADDRHD             | -0.778 |       | -0.915 |       | ns   |
| Read enable setup time  | T <sub>RDENSU</sub>   | 0.278  |       | 0.327  |       | ns   |
| Read enable hold time   | T <sub>RDENHD</sub>   | 0.057  |       | 0.067  |       | ns   |
| Read block select setup time  | T <sub>BLKSU</sub>    | 1.839  |       | 2.163  |       | ns   |
| Read block select hold time   | T <sub>BLKHD</sub>    | -0.65  |       | -0.765 |       | ns   |
| Read block select to out disable time (when pipelined register is disabled)           | T <sub>BLK2Q</sub>    |        | 2.036 |        | 2.396 | ns   |
| Read asynchronous reset removal time (pipelined clock)                                |                       | -0.023 |       | -0.027 |       | ns   |
| Read asynchronous reset removal time (non-pipelined clock)                            | T <sub>RSTREM</sub>   | 0.046  |       | 0.054  |       | ns   |
| Read asynchronous reset recovery time (pipelined clock)                               |                       | 0.507  |       | 0.597  |       | ns   |
| Read asynchronous reset recovery time (non-pipelined clock)                           | T <sub>RSTREC</sub>   | 0.236  |       | 0.278  |       | ns   |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | T <sub>R2Q</sub>      |        | 0.835 |        | 0.982 | ns   |
| Read synchronous reset setup time   | T <sub>SRSTSU</sub>   | 0.271  |       | 0.319  |       | ns   |
| Read synchronous reset hold time  | T <sub>SRSTHD</sub>   | 0.061  |       | 0.071  |       | ns   |
| Write clock period  | T <sub>CCY</sub>      | 4      |       | 4      |       | ns   |
| Write clock minimum pulse width high  | T <sub>CCLKMPWH</sub> | 1.8    |       | 1.8    |       | ns   |
| Write clock minimum pulse width low   | T <sub>CCLKMPWL</sub> | 1.8    |       | 1.8    |       | ns   |
| Write block setup time  | T <sub>BLKCSU</sub>   | 0.404  |       | 0.476  |       | ns   |
| Write block hold time   | T <sub>BLKCHD</sub>   | 0.007  |       | 0.008  |       | ns   |
| Write input data setup time   | T <sub>DINCSU</sub>   | 0.115  |       | 0.135  |       | ns   |
| Write input data hold time  | T <sub>DINCHD</sub>   | 0.15   |       | 0.177  |       | ns   |
| Write address setup time  | T <sub>ADDRCSU</sub>  | 0.088  |       | 0.104  |       | ns   |
| Write address hold time   | T <sub>ADDRCHD</sub>  | 0.128  |       | 0.15   |       | ns   |
| Write enable setup time   | TWECSU                | 0.397  |       | 0.467  |       | ns   |
| Write enable hold time  | T <sub>WECHD</sub>    | -0.026 |       | -0.03  |       | ns   |
| Maximum frequency   | F <sub>MAX</sub>      |        | 250   |        | 250   | MHz  |



#### Table 245 • JTAG Programming (eNVM Only)

| M2S/M2GL |                  |         |        |      |
|----------|------------------|---------|--------|------|
| Device   | Image size Bytes | Program | Verify | Unit |
| 005      | 137536           | 39      | 4      | Sec  |
| 010      | 274816           | 78      | 9      | Sec  |
| 025      | 274816           | 78      | 9      | Sec  |
| 050      | 278528           | 84      | 8      | Sec  |
| 060      | 268480           | 76      | 8      | Sec  |
| 090      | 544496           | 154     | 15     | Sec  |
| 150      | 544496           | 155     | 15     | Sec  |

Table 246 • JTAG Programming (Fabric and eNVM)

| M2S/M2GL<br>Device | Image size Bytes | Program | Verify | Unit |
|--------------------|------------------|---------|--------|------|
| 005                | 439296           | 59      | 11     | Sec  |
| 010                | 842688           | 107     | 20     | Sec  |
| 025                | 1497408          | 120     | 35     | Sec  |
| 050                | 2695168          | 162     | 59     | Sec  |
| 060                | 2686464          | 158     | 70     | Sec  |
| 090                | 4190208          | 266     | 147    | Sec  |
| 150                | 6682768          | 316     | 231    | Sec  |

Table 247 • 2 Step IAP Programming (Fabric Only)

| M2S/M2GL<br>Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|--------------------|------------------|--------------|---------|--------|------|
| 005                | 302672           | 4            | 17      | 6      | Sec  |
| 010                | 568784           | 7            | 23      | 12     | Sec  |
| 025                | 1223504          | 14           | 33      | 23     | Sec  |
| 050                | 2424832          | 29           | 52      | 40     | Sec  |
| 060                | 2418896          | 39           | 61      | 50     | Sec  |
| 090                | 3645968          | 60           | 84      | 73     | Sec  |
| 150                | 6139184          | 100          | 132     | 120    | Sec  |



The following table lists the IGLOO2 DEVRST\_N to functional times in worst-case industrial conditions when T<sub>J</sub> = 100 °C, V<sub>DD</sub> = 1.14 V.

#### Table 292 • DEVRST\_N to Functional Times for IGLOO2

|                         |                      |                               | Maximum Power-up to Functional Time for IGLOO2<br>(uS)               |     |     |     |     | IGLOO2 |     |     |
|-------------------------|----------------------|-------------------------------|--|-----|-----|-----|-----|--------|-----|-----|
| Symbol                  | From                 | То                            | Description  | 005 | 010 | 025 | 050 | 060    | 090 | 150 |
| T <sub>POR2OUT</sub>    | POWER_ON<br>_RESET_N | Output<br>available at<br>I/O | Fabric to output   | 114 | 116 | 113 | 113 | 115    | 115 | 114 |
| T <sub>DEVRST2OUT</sub> | DEVRST_N             | Output<br>available at<br>I/O | V <sub>DD</sub> at its<br>minimum<br>threshold<br>level to<br>output | 314 | 353 | 314 | 307 | 343    | 341 | 341 |
| T <sub>DEVRST2POR</sub> | DEVRST_N             | POWER_O<br>N_RESET_<br>N      | V <sub>DD</sub> at its<br>minimum<br>threshold<br>level to<br>fabric | 200 | 238 | 201 | 195 | 230    | 229 | 227 |
| T <sub>DEVRST2WPU</sub> | DEVRST_N             | DDRIO<br>Inbuf weak<br>pull   | DEVRST_N<br>to Inbuf weak<br>pull                                    | 208 | 202 | 197 | 193 | 216    | 215 | 215 |
|                         | DEVRST_N             | MSIO Inbuf<br>weak pull       | DEVRST_N<br>to Inbuf weak<br>pull                                    | 208 | 202 | 197 | 193 | 216    | 215 | 215 |
|                         | DEVRST_N             | MSIOD<br>Inbuf weak<br>pull   | DEVRST_N<br>to Inbuf weak<br>pull                                    | 208 | 202 | 197 | 193 | 216    | 215 | 215 |







## 2.3.32 CAN Controller Characteristics

The following table lists the CAN controller characteristics in worst-case industrial conditions when  $T_J$  = 100 °C,  $V_{DD}$  = 1.14 V.

#### Table 306 • CAN Controller Characteristics

| Parameter               | Description   | -1   | -Std | Unit |
|-------------------------|---|------|------|------|
| FCANREFCLK <sup>1</sup> | Internally sourced CAN reference<br>clock frequency | 160  | 136  | MHz  |
| BAUDCANMAX              | Maximum CAN performance baud rate                   | 1    | 1    | Mbps |
| BAUDCANMIN              | Minimum CAN performance baud rate                   | 0.05 | 0.05 | Mbps |

1. PCLK to CAN controller must be a multiple of 8 MHz.

## 2.3.33 USB Characteristics

The following table lists the USB characteristics in worst-case industrial conditions when  $T_J = 100$  °C,  $V_{DD} = 1.14$  V.

| Table 307 • | USB Characteristics |  |
|-------------|---------------------|--|
|             |                     |  |

| Parameter  | Description   | -1    | -Std  | Unit |
|------------|---|-------|-------|------|
| FUSBREFCLK | Internally sourced USB reference clock<br>frequency | 166   | 142   | MHz  |
| TUSBCLK    | USB clock period                                    | 16.66 | 16.66 | ns   |
| TUSBPD     | Clock to USB data propagation delay                 | 9.0   | 9.0   | ns   |
| TUSBSU     | Setup time for USB data                             | 6.0   | 6.0   | ns   |
| TUSBHD     | Hold time for USB data                              | 0     | 0     | ns   |