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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	146124
Total RAM Bits	5120000
Number of I/O	574
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl150ts-fcg1152i



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- Updated [Table 24](#), page 22 with minimum and maximum values for input current low and high (SAR 73114 and 80314).
- Added [Non-Deterministic Random Bit Generator \(NRBG\) Characteristics](#), page 106 (SAR 73114 and 79517).
- Added 060 device in [Table 282](#), page 110 (SAR 79860).
- Added [DEVRST_N to Functional Times](#), page 116 (SAR 73114).
- Added [Cryptographic Block Characteristics](#), page 106 (SAR 73114 and 79516).
- Update [Table 296](#), page 121 with VTX-AMP details (SAR 81756).
- Update note in [Table 297](#), page 122 (SAR 74570 and 80677).
- Update [Table 298](#), page 122 with generic EPCS details (SAR 75307).
- Added [Table 308](#), page 129 (SAR 50424).

1.2 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- The Surge Current on VDD during DEVRST_B Assertion and Surge Current on VDD during Digest Check using System Services tables were deleted and added reference to [AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note](#). (SAR 76865 and 76623).
- Added 060 device in [Table 4](#), page 6 (SAR 76383).
- Updated [Table 24](#), page 22 for ramp time input (SAR 72103).
- Added 060 device details in [Table 284](#), page 112 (SAR 74927).
- Updated [Table 290](#), page 116 for name change (SAR 74925).
- Updated [Table 283](#), page 111 for 060 FG676 Package details (SAR 78849).
- Updated [Table 305](#), page 126 for SmartFusion2 and [Table 310](#), page 129 for IGLOO2 for SPI timing and Fmax (SAR 56645, 75331).
- Updated [Table 293](#), page 119 for Flash*Freeze entry and exit times (SAR 75329, 75330).
- Updated [Table 297](#), page 122 for RX-CID information (SAR 78271).
- Added [Table 8](#), page 8 and [Figure 1](#), page 9 (SAR 78932).
- Updated [Table 223](#), page 76 for timing characteristics and [Table 224](#), page 77 (SAR 75998).
- Added [SRAM PUF](#), page 105 (SAR 64406).
- Added a footnote on digest cycle in [Table 5](#), page 7 (SAR 79812).

1.3 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document.

- Added a note in [Table 5](#), page 7 (SAR 71506).
- Added a note in [Table 6](#), page 8 (SAR 74616).
- Added a note in [Figure 3](#), page 17 (SAR 71506).
- Updated Quiescent Supply Current for 060 in [Table 11](#), page 12 and [Table 12](#), page 13 (SAR 74483).
- Updated programming currents for 060 in [Table 13](#), page 13, [Table 14](#), page 13, and [Table 15](#), page 14.
- Added DEVRST_B assertion tables (SAR 74708).
- Updated I/O speeds for LVDS 3.3 V in [Table 18](#), page 19 and [Table 21](#), page 20 (SAR 69829).
- Updated [Table 24](#), page 22 (SAR 69418).
- Updated [Table 25](#), page 22, [Table 26](#), page 23, [Table 27](#), page 23 (SAR 74570).
- Updated all AC/DC table to link to the [Input Capacitance, Leakage Current, and Ramp Time](#), page 22 for reference (SAR 69418).

where

- θ_{JA} = Junction-to-air thermal resistance
 θ_{JB} = Junction-to-board thermal resistance
 θ_{JC} = Junction-to-case thermal resistance
 T_J = Junction temperature
 T_A = Ambient temperature
 T_B = Board temperature (measured 1.0 mm away from the package edge)
 T_C = Case temperature
 P = Total power dissipated by the device

Table 9 • Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices

	Still Air	1.0 m/s	2.5 m/s			
Device	θ_{JA}			θ_{JB}	θ_{JC}	Unit
005						
FG484	19.36	15.81	14.63	9.74	5.27	°C/W
VF256	41.30	38.16	35.30	28.41	3.94	°C/W
VF400	20.19	16.94	15.41	8.86	4.95	°C/W
TQ144	42.80	36.80	34.50	37.20	10.80	°C/W
010						
FG484	18.22	14.83	13.62	8.83	4.92	°C/W
VF256	37.36	34.26	31.45	24.84	7.89	°C/W
VF400	19.40	15.75	14.22	8.11	4.22	°C/W
TQ144	38.60	32.60	30.30	31.80	8.60	°C/W
025						
FG484	17.03	13.66	12.45	7.66	4.18	°C/W
VF256	33.85	30.59	27.85	21.63	6.13	°C/W
VF400	18.36	14.89	13.36	7.12	3.41	°C/W
FCS325	29.17	24.87	23.12	14.44	2.31	°C/W
050						
FG484	15.29	12.19	10.99	6.27	3.24	°C/W
FG896	14.70	12.50	10.90	7.20	4.90	°C/W
VF400	17.53	14.17	12.63	6.32	2.81	°C/W
FCS325	27.38	23.18	21.41	12.47	1.59	°C/W
060						
FG484	15.40	12.06	10.85	6.14	3.15	°C/W
FG676	15.49	12.21	11.06	7.07	3.87	°C/W
VF400	17.45	14.01	12.47	6.22	2.69	°C/W
FCS325	27.03	22.91	21.25	12.33	1.54	°C/W
090						
FG484	14.64	11.37	10.16	5.43	2.77	°C/W
FG676	14.52	11.19	10.37	6.17	3.24	°C/W
FCS325	26.63	22.26	20.13	14.24	2.50	°C/W

2.3.2 Power Consumption

The following sections describe the power consumptions of the devices.

2.3.2.1 Quiescent Supply Current

Table 10 • Quiescent Supply Current Characteristics

Power Supplies/Blocks	Modes and Configurations	
	Non-Flash*Freeze	Flash*Freeze
FPGA Core	On	Off
V _{DD} /SERDES_[01]_VDD ¹	On	On
V _{PP} /V _{PPNVM}	On	On
HPMS_MDDR_PLL_VDDA/FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA/PLL0_PLL1_HPMS_MDDR_VDD A	0 V	0 V
SERDES_[01]_PLL_VDDA ²	0 V	0 V
SERDES_[01]_L[0123]_VDDAPLL/VDD_2V5 ²	On	On
SERDES_[01]_L[0123]_VDDAIIO ²	On	On
V _{DDIx} ^{3, 4}	On	On
V _{REFx}	On	On
MSSDDR CLK	32 kHz	32 kHz
RAM	On	Sleep state
System controller	50 MHz	50 MHz
50 MHz oscillator (enable/disable)	Enable	Disabled
1 MHz oscillator (enable/disable)	Disabled	Disabled
Crystal oscillator (enable/disable)	Disabled	Disabled

1. SERDES_[01]_VDD Power Supply is shorted to V_{DD}.
2. SerDes and DDR blocks to be unused.
3. V_{DDIx} has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate V_{DDI} bank supplies. For details on bank power supplies, see "Recommendation for Unused Bank Supplies" table in the *AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.
4. No Differential (that is to say, LVDS) I/Os or ODT attributes to be used.

Table 11 • SmartFusion2 and IGLOO2 Quiescent Supply Current (V_{DD} = 1.2 V) – Typical Process

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC1	Non-Flash*Freeze	6.2	6.9	8.9	13.1	15.3	15.4	27.5	mA	Typical (T _J = 25 °C)
		24.0	28.4	40.6	67.8	80.6	81.4	144.7	mA	Commercial (T _J = 85 °C)
		35.2	41.9	60.5	102.1	121.4	122.6	219.1	mA	Industrial (T _J = 100 °C)

Table 17 • Timing Model Parameters (continued)

Index	Symbol	Description	-1	Unit	For More Information
F	T_{DP}	Propagation delay of an OR gate	0.179	ns	See Table 223 , page 76
G	T_{DP}	Propagation delay of an LVDS transmitter	2.136	ns	See Table 169 , page 57
H	T_{DP}	Propagation delay of a three-input XOR Gate	0.241	ns	See Table 223 , page 76
I	T_{DP}	Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 16 mA on the MSIO bank	2.412	ns	See Table 46 , page 27
J	T_{DP}	Propagation delay of a two-input NAND gate	0.179	ns	See Table 223 , page 76
K	T_{DP}	Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 8 mA on the MSIO bank	2.309	ns	See Table 46 , page 27
L	T_{CLKQ}	Clock-to-Q of the data register	0.108	ns	See Table 224 , page 77
	T_{SUD}	Setup time of the data register	0.254	ns	See Table 224 , page 77
M	T_{DP}	Propagation delay of a two-input AND gate	0.179	ns	See Table 223 , page 76
N	T_{OCLKQ}	Clock-to-Q of the output data register	0.263	ns	See Table 220 , page 69
	T_{OSUD}	Setup time of the output data register	0.19	ns	See Table 220 , page 69
O	T_{DP}	Propagation delay of SSTL2, Class I transmitter on the MSIO bank	2.055	ns	See Table 114 , page 45
P	T_{DP}	Propagation delay of LVCMOS 1.5 V transmitter, drive strength of 12 mA, fast slew on the DDRIO bank	3.316	ns	See Table 70 , page 34

2.3.5 User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the I/Os section of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

2.3.5.1 Input Buffer and AC Loading

The following figure shows the input buffer and AC loading.

Figure 3 • Input Buffer AC Loading

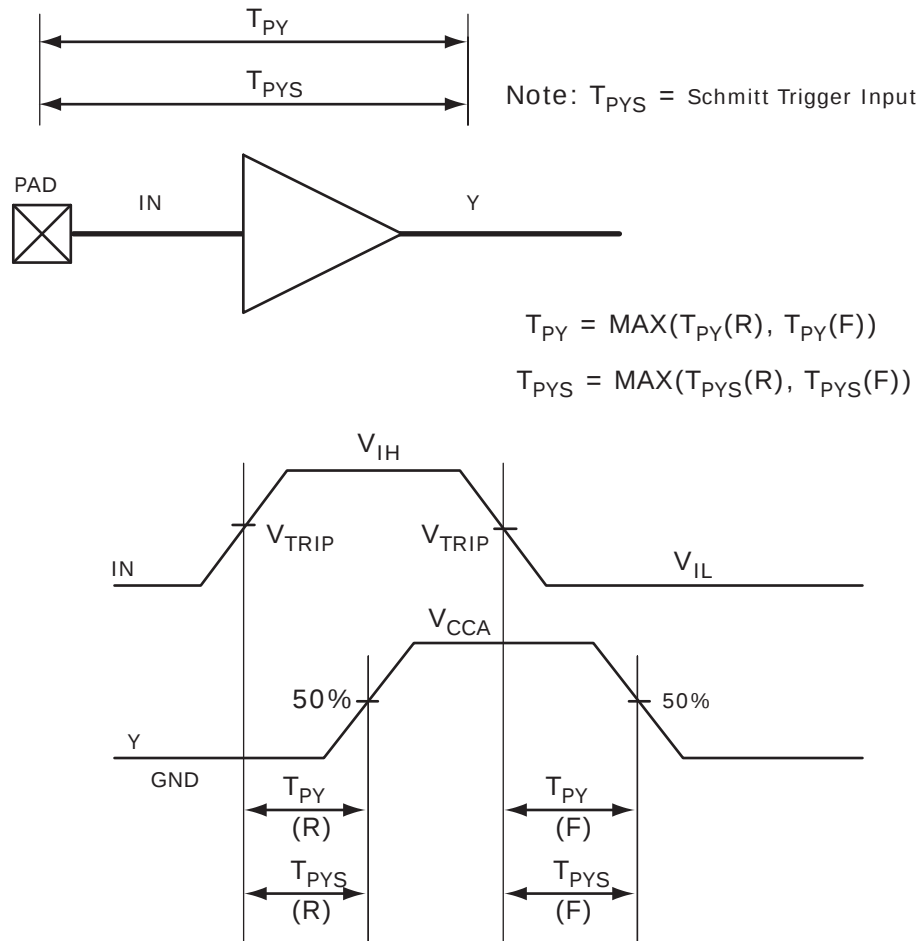


Table 34 • LVTTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.4	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 35 • LVTTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank

Output Drive Selection	V_{OH} (V)	V_{OL} (V)	IOH (at V_{OH}) mA	IOL (at V_{OL}) mA
2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	$V_{DDI} - 0.4$	0.4	4	4
8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA	$V_{DDI} - 0.4$	0.4	16	16
20 mA	$V_{DDI} - 0.4$	0.4	20	20

Note: For a detailed I/V curve, use the corresponding IBIS models:
www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.0\text{ V}$

Table 36 • LVTTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	2.262	2.663	2.289	2.695	ns

Table 37 • LVTTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.192	3.755	3.47	4.083	2.969	3.494	1.856	2.183	3.337	3.926	ns
4 mA	Slow	2.331	2.742	2.673	3.145	2.526	2.973	3.034	3.569	4.451	5.236	ns
8 mA	Slow	2.135	2.511	2.33	2.741	2.297	2.703	4.532	5.331	4.825	5.676	ns
12 mA	Slow	2.052	2.414	2.107	2.479	2.162	2.544	5.75	6.764	5.445	6.406	ns
16 mA	Slow	2.062	2.425	2.072	2.438	2.145	2.525	5.993	7.05	5.625	6.618	ns
20 mA	Slow	2.148	2.527	1.999	2.353	2.088	2.458	6.262	7.367	5.876	6.913	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 43 • LVCMOS 2.5 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.2	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	$\Omega\sigma$
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 44 • LVCMOS 2.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (With Software Default Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	4 mA	4 mA	$V_{DDI} - 0.4$	0.4	4	4
6 mA	6 mA	6 mA	$V_{DDI} - 0.4$	0.4	6	6
8 mA	8 mA	8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	12 mA	12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA		16 mA	$V_{DDI} - 0.4$	0.4	16	16

Note: For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at:
www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 45 • LVCMOS 2.5 V Receiver Characteristics (Input Buffers)

	On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
		-1	-Std	-1	-Std	
LVCMOS 2.5 V (for DDRIO I/O bank)	None	1.823	2.145	1.932	2.274	ns
LVCMOS 2.5 V (for MSIO I/O bank)	None	2.486	2.925	2.495	2.935	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	None	2.29	2.694	2.305	2.712	ns

Table 46 • LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.657	4.302	3.393	3.991	3.675	4.323	3.894	4.582	3.552	4.18	ns
	Medium	3.374	3.97	3.139	3.693	3.396	3.995	3.635	4.277	3.253	3.828	ns
	Medium fast	3.239	3.811	3.036	3.572	3.261	3.836	3.519	4.141	3.128	3.681	ns
	Fast	3.224	3.793	3.029	3.563	3.246	3.818	3.512	4.132	3.119	3.67	ns

Table 57 • LVCMOS 1.8 V Transmitter Characteristics for DDRIO I/O Bank with Fixed Code (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	Medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	Medium fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	Fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4 mA	Slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	Medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	Medium fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	Fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6 mA	Slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	Medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	Medium fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	Fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns
8 mA	Slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns
	Medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	Medium fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	Fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10 mA	Slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	Medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	Medium fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	Fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12 mA	Slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	Medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	Medium fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	Fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16 mA	Slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	Medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	Medium fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	Fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 62 • LVCMOS 1.5 V DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC output logic high	VOH	$V_{DDI} \times 0.75$		V
DC output logic low	VOL		$V_{DDI} \times 0.25$	V

Table 63 • LVCMOS 1.5 V AC Minimum and Maximum Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D _{MAX}	235	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D _{MAX}	160	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	D _{MAX}	220	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 64 • LVCMOS 1.5 V AC Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CA L	75, 60, 50, 40	Ω

Table 65 • LVCMOS 1.5 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point	V _{TRIP}	0.75	V
Resistance for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	R _{ENT}	2K	Ω
Capacitive loading for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	C _{ENT}	5	pF
Capacitive loading for data path (T _{DP})	C _{LOAD}	5	pF

Table 66 • LVCMOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			V _{OH} (V)	V _{OL} (V)	IOH (at V _{OH}) mA	IOL (at V _{OL}) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	2	2
4 mA	4 mA	4 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	4	4
6 mA	6 mA	6 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	6	6
8 mA		8 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	8	8
		10 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	10	10
		12 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	12	12

Note: For a detailed I/V curve, use the corresponding IBIS models:

www.microsemi.com/soc/download/ibis/default.aspx.

Table 70 • LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)
(continued)

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
6 mA	Slow	4.244	4.993	3.465	4.076	4.233	4.979	6.39	7.518	5.736	6.748	ns
	Medium	3.774	4.44	3.05	3.587	3.762	4.426	6.114	7.193	5.397	6.35	ns
	Medium fast	3.544	4.17	2.839	3.339	3.529	4.152	5.978	7.033	5.27	6.2	ns
	Fast	3.519	4.14	2.82	3.317	3.504	4.122	5.965	7.017	5.259	6.187	ns
8 mA	Slow	4.099	4.823	3.311	3.894	4.087	4.807	6.584	7.746	5.854	6.888	ns
	Medium	3.656	4.301	2.927	3.443	3.642	4.284	6.311	7.425	5.553	6.533	ns
	Medium fast	3.437	4.044	2.731	3.213	3.42	4.023	6.182	7.273	5.435	6.394	ns
	Fast	3.41	4.012	2.715	3.193	3.393	3.991	6.178	7.269	5.425	6.383	ns
10 mA	Slow	4.029	4.74	3.238	3.809	4.015	4.723	6.732	7.921	5.965	7.018	ns
	Medium	3.601	4.237	2.867	3.372	3.586	4.218	6.473	7.615	5.669	6.669	ns
	Medium fast	3.384	3.981	2.672	3.143	3.365	3.958	6.351	7.471	5.55	6.529	ns
	Fast	3.357	3.949	2.655	3.123	3.338	3.927	6.345	7.464	5.54	6.518	ns
12 mA	Slow	3.974	4.675	3.196	3.759	3.958	4.656	6.842	8.049	6.068	7.139	ns
	Medium	3.55	4.176	2.827	3.326	3.534	4.157	6.584	7.746	5.751	6.766	ns
	Medium fast	3.345	3.935	2.638	3.103	3.325	3.911	6.488	7.633	5.641	6.637	ns
	Fast	3.316	3.902	2.621	3.083	3.297	3.878	6.486	7.63	5.626	6.619	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 71 • LVCMOS 1.5 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	4.423	5.203	5.397	6.35	5.686	6.69	5.609	6.599	5.561	6.542	ns
4 mA	Slow	4.05	4.765	4.503	5.298	4.92	5.788	7.358	8.657	6.525	7.677	ns
6 mA	Slow	4.081	4.801	4.259	5.012	4.699	5.528	7.659	9.011	6.709	7.893	ns
8 mA	Slow	4.234	4.98	4.068	4.786	4.521	5.319	8.218	9.668	7.05	8.294	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 95 • HSTL DC Output Voltage Specification Applicable to DDRIO I/O Bank Only

Parameter	Symbol	Min	Max	Unit
HSTL Class I				
DC output logic high	V_{OH}	$V_{DDI} - 0.4$		V
DC output logic low	V_{OL}		0.4	V
Output minimum source DC current (MSIO and DDRIO I/O banks)	I_{OH} at V_{OH}	-8.0		mA
Output minimum sink current (MSIO and DDRIO I/O banks)	I_{OL} at V_{OL}	8.0		mA
HSTL Class II				
DC output logic high	V_{OH}	$V_{DDI} - 0.4$		V
DC output logic low	V_{OL}		0.4	V
Output minimum source DC current	I_{OH} at V_{OH}	-16.0		mA
Output minimum sink current	I_{OL} at V_{OL}	16.0		mA

Table 96 • HSTL DC Differential Voltage Specification

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID} (DC)	0.2	V

Table 97 • HSTL AC Differential Voltage Specifications

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF}	0.4		V
AC differential cross point voltage	V_x	0.68	0.9	V

Table 98 • HSTL Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	400	Mbps	AC loading: per JEDEC specifications

Table 99 • HSTL Impedance Specification

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	R_{REF}	25.5, 47.8	Ω	Reference resistance = 191 Ω
Effective impedance value (ODT for DDRIO I/O bank only)	R_{TT}	47.8	Ω	Reference resistance = 191 Ω

Table 168 • LVDS25 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.554	3.004	ns
100	2.549	2.999	ns

Table 169 • LVDS25 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.136	2.513	2.416	2.842	2.402	2.825	2.423	2.85	2.409	2.833	ns

Table 170 • LVDS25 Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
No pre-emphasis	1.61	1.893	1.749	2.058	1.735	2.041	1.897	2.231	1.866	2.195	ns
Min pre-emphasis	1.527	1.796	1.757	2.067	1.744	2.052	1.905	2.241	1.876	2.207	ns
Med pre-emphasis	1.496	1.76	1.765	2.077	1.751	2.06	1.914	2.252	1.884	2.216	ns

LVDS33 AC Switching Characteristics**Table 171 • LVDS33 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

On Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.572	3.025	ns
100	2.569	3.023	ns

Table 172 • LVDS33 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
1.942	2.284	1.98	2.33	1.97	2.318	1.953	2.298	1.96	2.307	ns

Table 215 • LVPECL DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	3.45	V

Table 216 • LVPECL DC Differential Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
Input common mode voltage	V_{ICM}	0.3		2.8	V
Input differential voltage	V_{IDIFF}	100	300	1,000	mV

Table 217 • LVPECL Minimum and Maximum AC Switching Speeds

Parameter	Symbol	Max	Unit
Maximum data rate	D_{MAX}	900	Mbps

AC Switching Characteristics

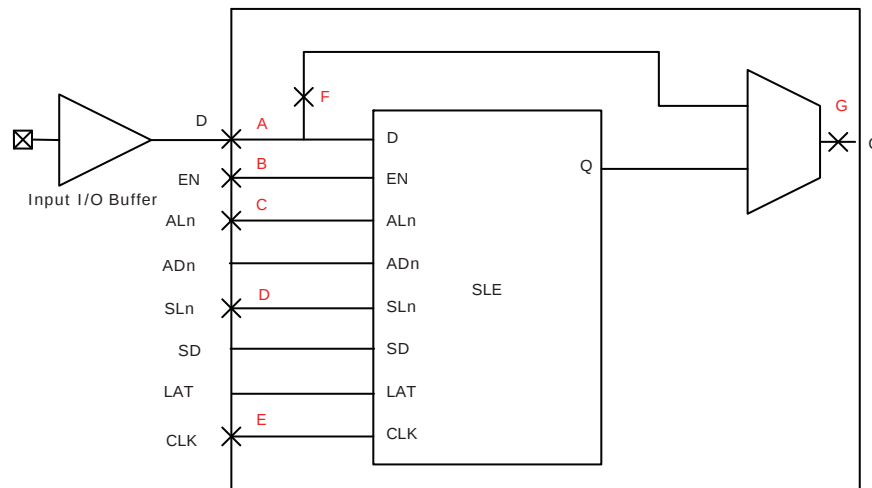
Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$.

Table 218 • LVPECL Receiver Characteristics for MSIO I/O Bank

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.572	3.025	ns
100	2.569	3.023	ns

2.3.8 I/O Register Specifications

This section describes input and output register specifications.

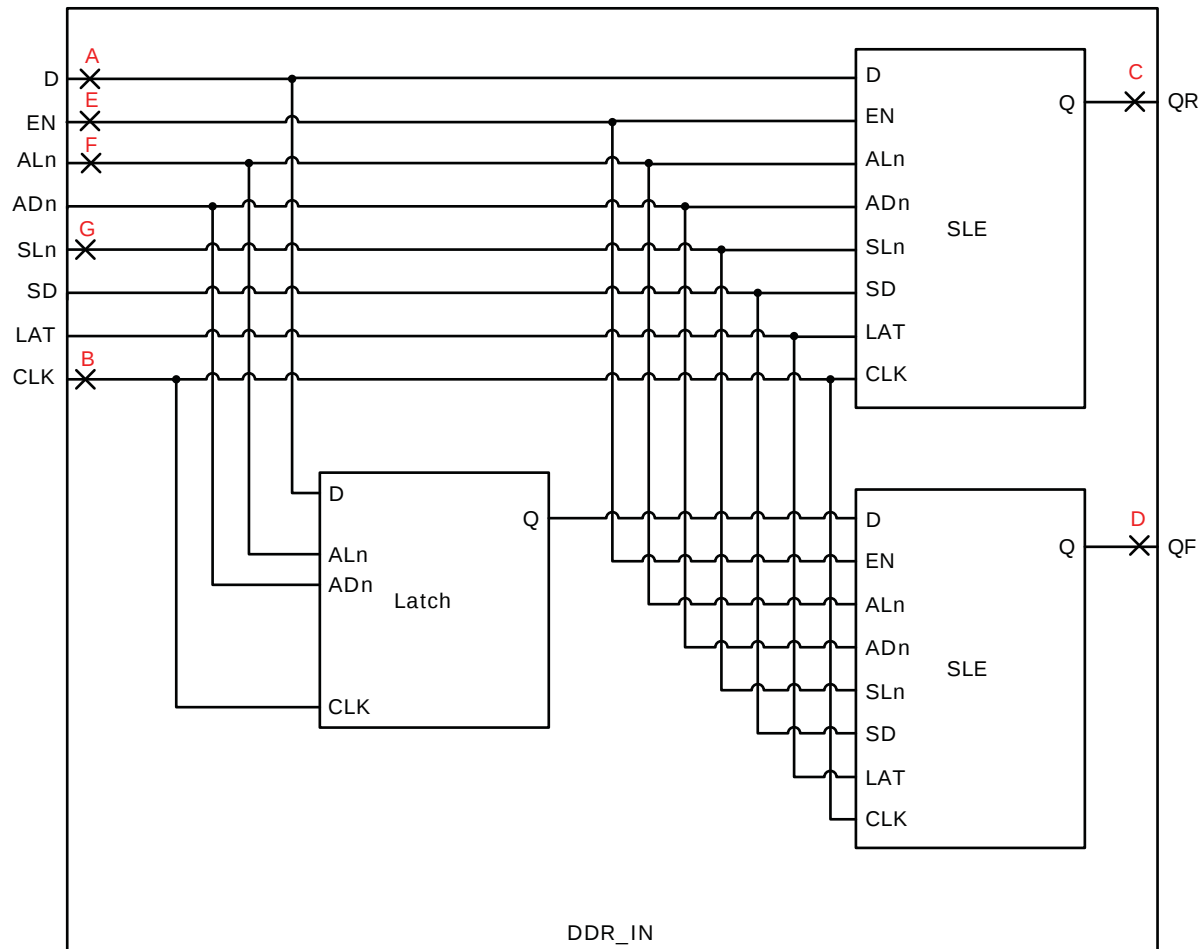
2.3.8.1 Input Register**Figure 6 • Timing Model for Input Register**

2.3.9 DDR Module Specification

This section describes input and output DDR module and timing specifications.

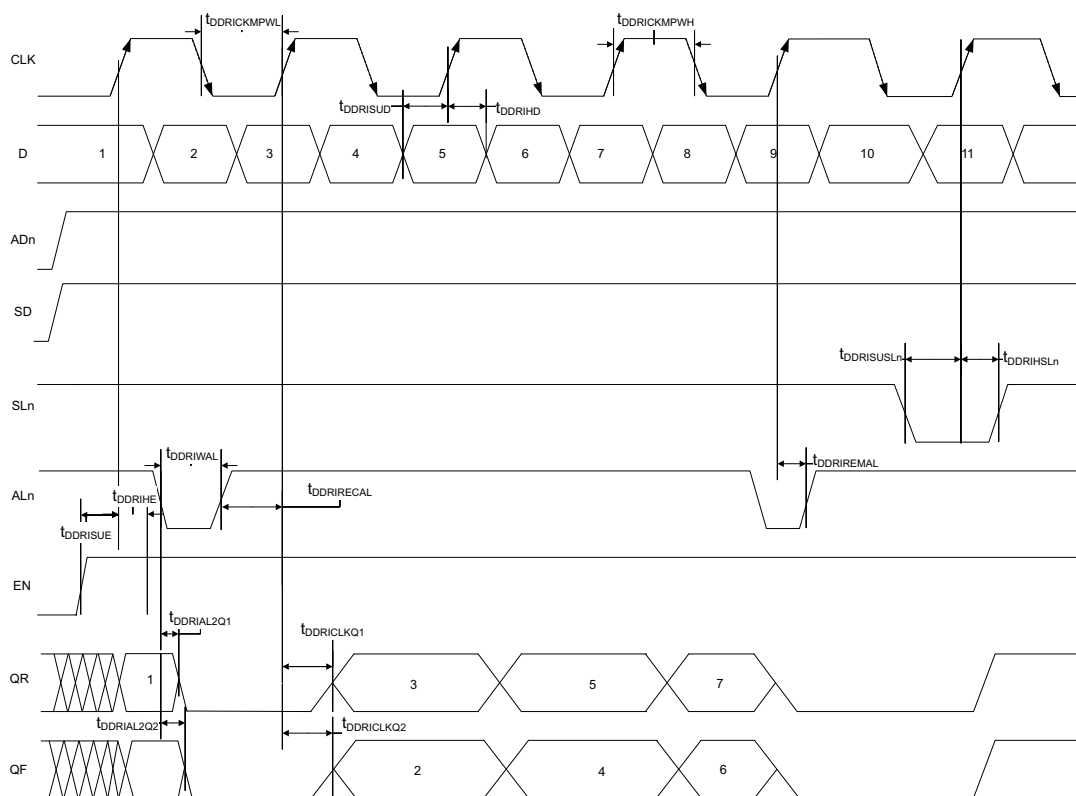
2.3.9.1 Input DDR Module

Figure 10 • Input DDR Module



2.3.9.2 Input DDR Timing Diagram

Figure 11 • Input DDR Timing Diagram



2.3.9.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 221 • Input DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDRICKQ1}$	Clock-to-Out Out_QR for input DDR	B, C	0.16	0.188	ns
$T_{DDRICKQ2}$	Clock-to-Out Out_QF for input DDR	B, D	0.166	0.195	ns
$T_{DDRISUD}$	Data setup for input DDR	A, B	0.357	0.421	ns
T_{DDRIHD}	Data hold for input DDR	A, B	0	0	ns
$T_{DDRISUE}$	Enable setup for input DDR	E, B	0.46	0.542	ns
T_{DDRIHE}	Enable hold for input DDR	E, B	0	0	ns
$T_{DDRISUSLn}$	Synchronous load setup for input DDR	G, B	0.46	0.542	ns
$T_{DDRIHSLn}$	Synchronous load hold for input DDR	G, B	0	0	ns
$T_{DDRIAL2Q1}$	Asynchronous load-to-out QR for input DDR	F, C	0.587	0.69	ns
$T_{DDRIAL2Q2}$	Asynchronous load-to-out QF for input DDR	F, D	0.541	0.636	ns
$T_{DDRIREMAL}$	Asynchronous load removal time for input DDR	F, B	0	0	ns
$T_{DDRIRECAL}$	Asynchronous load recovery time for input DDR	F, B	0.074	0.087	ns

Table 241 • μ SRAM (RAM256x4) in 256 × 4 Mode (continued)

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Write address hold time	$T_{ADDRCHD}$	0.245		0.288		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.03		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 512 × 2 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 242 • μ SRAM (RAM512x2) in 512 × 2 Mode

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.27		0.31	ns
Read access time without pipeline register			1.76		2.08	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.96		2.306		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.137		0.161		ns
Read address hold time in asynchronous mode		–0.58		–0.68		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.77		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.14		2.52	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.02		–0.03		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.83		0.98	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns

Table 276 • Cryptographic Block Characteristics (continued)

Service	Conditions	Timing	Unit
SHA256	512 bits	540	kbps
	1024 bits	780	kbps
	2048 bits	950	kbps
	24 kbits	1140	kbps
HMAC	512 bytes	820	kbps
	1024 bytes	890	kbps
	2048 bytes	930	kbps
	24 kbytes	980	kbps
KeyTree		1.8	ms
Challenge-response	PUF = OFF	25	ms
	PUF = ON	7	ms
ECC point multiplication		590	ms
ECC point addition		8	ms

1. Using cypher block chaining (CBC) mode.

2.3.19 Crystal Oscillator

The following table describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

Table 277 • Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		20		MHz	
Accuracy	ACCXTAL			0.0047	%	005, 010, 025, 050, 060, and 090 devices
				0.0058	%	150 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		200	300	ps	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		200	300	ps	010, 025, 050, and 060 devices
			250	410	ps	150 devices
			250	550	ps	005 and 090 devices
Operating current	IDYNXTAL		1.5		mA	010, 050, and 060 devices
			1.65		mA	005, 025, 090, and 150 devices
Input logic level high	VIHXTAL	0.9 V _{PP}			V	
Input logic level low	VILXTAL			0.1 V _{PP}	V	

Table 303 • I2C Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Maximum data rate	D_{MAX}			400	Kbps	Fast mode
				100	Kbps	Standard mode
Pulse width of spikes which must be suppressed by the input filter	T_{FILT}		50		ns	Fast mode

- These values are provided for MSIO Bank–LVTTL 8 mA Low Drive at 25 °C, typical conditions. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
- These maximum values are provided for information only. Minimum output buffer resistance values depend on V_{DDIX} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
- $R(PULL-DOWN-MAX) = (VOL_{spec})/IOL_{spec}$.
- $R(PULL-UP-MAX) = (VDDImax - VOH_{spec})/IOH_{spec}$.

The following table lists the I²C switching characteristics in worst-case industrial conditions when $T_J = 100\text{ °C}$, $V_{DD} = 1.14\text{ V}$

Table 304 • I2C Switching Characteristics

Parameter	Symbol	–1	Std	Unit
		Min	Min	
Low period of I2C_x_SCL	T_{LOW}	1	1	PCLK cycles
High period of I2C_x_SCL	T_{HIGH}	1	1	PCLK cycles
START hold time	$T_{HD;STA}$	1	1	PCLK cycles
START setup time	$T_{SU;STA}$	1	1	PCLK cycles
DATA hold time	$T_{HD;DAT}$	1	1	PCLK cycles
DATA setup time	$T_{SU;DAT}$	1	1	PCLK cycles
STOP setup time	$T_{SU;STO}$	1	1	PCLK cycles

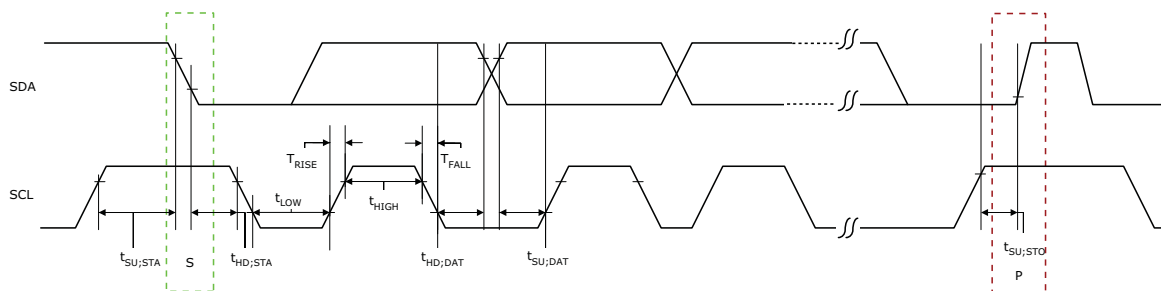
Figure 21 • I²C Timing Parameter Definition

Table 310 • SPI Characteristics for All Devices (continued)

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp2	SPI_[0 1]_CLK minimum pulse width high					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			µs	
	SPI_[0 1]_CLK = PCLK/32	0.095			µs	
	SPI_[0 1]_CLK = PCLK/64	0.195			µs	
	SPI_[0 1]_CLK = PCLK/128	0.385			µs	
sp3	SPI_[0 1]_CLK minimum pulse width low					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			µs	
	SPI_[0 1]_CLK = PCLK/32	0.095			µs	
	SPI_[0 1]_CLK = PCLK/64	0.195			µs	
	SPI_[0 1]_CLK = PCLK/128	0.385			µs	
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) ¹		2.77		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%–90%) ¹		2.906		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0 1]_DI setup time ²	12			ns	
sp9m	SPI_[0 1]_DI hold time ²	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0 1]_DI setup time ²	2			ns	
sp9s	SPI_[0 1]_DI hold time ²	7			ns	