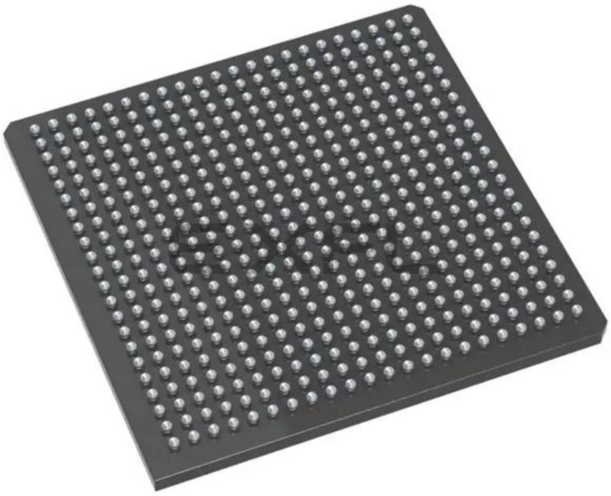
Microchip Technology - M2GL150TS-FCVG484 Datasheet



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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	146124
Total RAM Bits	5120000
Number of I/O	248
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BFBGA
Supplier Device Package	484-BGA
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl150ts-fcvg484

Figures

1.9 Revision 3.0

In revision 3.0 of this document, the Theta B/C columns and FCS325 package was updated. For more information, see Table 9, page 10 (SAR 62002).

1.10 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Table 1, page 4 was updated (SAR 59056).
- Table 7, page 8 temperature and data retention information was updated SAR (61363).
- Storage Operating Table was updated and split into three tables – Table 5, page 7, Table 7, page 8 (SAR 58725).
- Updated Theta B/C columns and FCS325 package in Table 9, page 10 (SAR 62002).
- Added 090-FCS325 thermal resistance to Table 9, page 10 (SAR 59384).
- TQ144 package was added to Table 9, page 10 (SAR 57708).
- Added PLL jitter data for the VF400 package (SAR 53162).
- Added Additional Worst Case IDD to Table 11, page 12 and Table 12, page 13 (SAR 59077).
- Table 13, page 13, Table 14, page 13, and Table 15, page 14 were added to verify Inrush currents (SAR 56348).
- Table 18, page 19 and Table 21, page 20 – I/O speeds were replaced.
- Max speed was changed in Table 41, page 26 (SAR 57221) and in Table 52, page 29 (SAR 57113).
- Minimum and Maximum DC/AC Input and Output Levels Specification, page 29 and Table 49, page 29–Table 57, page 31 were added.
- Added Cload to Table 89, page 39 (SAR 56238).
- Removed "Rs" information in DDR Timing Measurement Table 123, page 47, Table 133, page 49, and Table 144, page 52.
- Updated drive programming for M/B-LVDS outputs (SAR 58154).
- Added an inverter bubble to DDR_IN latch in Figure 10, page 70 (SAR 61418).
- QF waveform in Figure 11, page 71 was updated (SAR 59816).
- uSRAM Write Clock minimum values were updated in Table 237, page 86–Table 243, page 93 (SAR 55236).
- Fixed typo in the 32 kHz Crystal (XTAL) oscillator accuracy data section (SAR 59669).
- The "On-Chip Oscillator" section was split, and the Embedded NVM (eNVM) Characteristics, page 104 was added. Table 277, page 107–Table 281, page 109 were revised.(SARs 57898 and 59669).
- PLL VCP Frequency and conditions were added to Table 282, page 110 (SAR 57416).
- Fixed typo for PLL jitter data in the 100-400 MHz range (SAR 60727).
- Updated FCCC information in Table 282, page 110 and Table 283, page 111 (SAR 60799).
- Device 025 specifications were added to Table 283, page 111 (SAR 51625).
- JTAG Table 284, page 112 was replaced (SAR 51188).
- Flash*Freeze Table 293, page 119 was replaced (SAR 57828).
- Added support for HCSL I/O Standard for SERDES reference clocks in Table 300, page 123 and Table 301, page 123 (SAR 50748).
- Tir and Tif parameters were added to Table 303, page 124 (SAR 52203).
- Speed grade consistency was fixed in tables throughout the datasheet (SAR 50722).
- Added jitter attenuation information (SAR 59405).

1.11 Revision 1.0

The following is a summary of the changes in revision 1.0 of this document.

- The IGLOO2 v2 and the SmartFusion2 v5 datasheets are combined into this single product family datasheet.

Table 19 • **Maximum Data Rate Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
LPDDR			400	Mbps
HSTL1.5 V			400	Mbps
SSTL 2.5 V	510	700	400	Mbps
SSTL 1.8 V			667	Mbps
SSTL 1.5 V			667	Mbps

Table 20 • **Maximum Data Rate Summary Table for Differential I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	Unit
LVPECL (input only)	900		Mbps
LVDS 3.3 V	535		Mbps
LVDS 2.5 V	535	700	Mbps
RSDS	520	700	Mbps
BLVDS	500		Mbps
MLVDS	500		Mbps
Mini-LVDS	520	700	Mbps

Table 21 • **Maximum Frequency Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	315			MHz
LVTTL 3.3 V	300			MHz
LVCMOS 3.3 V	300			MHz
LVCMOS 2.5 V	205	210	200	MHz
LVCMOS 1.8 V	147.5	200	200	MHz
LVCMOS 1.5 V	80	110	118	MHz
LVCMOS 1.2 V	60	80	100	MHz
LPDDR– LVCMOS 1.8 V mode			200	MHz

2.3.5.5 Detailed I/O Characteristics

Table 24 • **Input Capacitance, Leakage Current, and Ramp Time**

Symbol	Description	Maximum	Unit	Conditions
C_{IN}	Input capacitance	10	pF	
I_{IL} (dc)	Input current low (Applicable to HSTL/SSTL inputs only)	400	µA	V_{DDI} = 2.5 V
		500	µA	V_{DDI} = 1.8 V
		600	µA	V_{DDI} = 1.5 V[1]
	Input current low (Applicable to all other digital inputs)	10	µA	
I_{IH} (dc)	Input current high (Applicable to HSTL/SSTL inputs only)	400	µA	V_{DDI} = 2.5 V
		500	µA	V_{DDI} = 1.8 V
		600	µA	V_{DDI} = 1.5 V[1]
	Input current high (Applicable to all other digital inputs)	10	µA	
T_{RAMPIN}[2]	Input ramp time (Applicable to all digital inputs)	50	ns	

1. Applicable when I/O pair is programmed with an HSTL/SSTL I/O type on IOP and an un-terminated I/O type (LVCMOS, for example) on ION pad.
2. Voltage ramp must be monotonic.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of DDRIO I/O bank at V_{OH}/V_{OL} Level.

Table 25 • **I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank**

	R(WEAK PULL-UP) at V_{OH} (Ω)		R(WEAK PULL-DOWN) at V_{OL} (Ω)	
V_{DDI} Domain	**Min**	**Max**	**Min**	**Max**
2.5 V[1, 2]	10K	17.8K	9.98K	18K
1.8 V[1, 2]	10.3K	19.1K	10.3K	19.5K
1.5 V[1, 2]	10.6K	20.2K	10.6K	21.1K
1.2 V[1, 2]	11.1K	22.7K	11.2K	24.6K

1. R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX).
2. R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN).

2.3.5.6 Single-Ended I/O Standards

2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 29 • **LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

Table 30 • **LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC input logic high	V_{IH} (DC)	2.0	3.45	V
DC input logic low	V_{IL} (DC)	–0.3	0.8	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

1. See Table 24, page 22.

Table 31 • **LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC output logic high[1]	V_{OH}	V_{DDI} – 0.4		V
DC output logic low[1]	V_{OL}		0.4	V

1. The V_{OH}/V_{OL} test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

Table 32 • **LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	2.4		V
DC output logic low	V_{OL}		0.4	V

Table 33 • **LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	600	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 53 • **LVCMOS 1.8 V AC Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	Rodt_cal	75, 60, 50, 33, 25, 20	Ω

Table 54 • **LVCMOS 1.8 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.9	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2k	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 55 • **LVCMOS 1.8 V Transmitter Drive Strength Specifications**

Output Drive Selection			V_{OH} (V)	V_{OL} (V)	IOH (at V_{OH}) mA	IOL (at V_{OL}) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max		
2 mA	2 mA	2 mA	V_{DDI} – 0.45	0.45	2	2
4 mA	4 mA	4 mA	V_{DDI} – 0.45	0.45	4	4
6 mA	6 mA	6 mA	V_{DDI} – 0.45	0.45	6	6
8 mA	8 mA	8 mA	V_{DDI} – 0.45	0.45	8	8
10 mA	10 mA	10 mA	V_{DDI} – 0.45	0.45	10	10
12 mA		12 mA	V_{DDI} – 0.45	0.45	12	12
		16 mA[1]	V_{DDI} – 0.45	0.45	16	16

[1] 16 mA drive strengths, all slews, meets LPDDR JEDEC electrical compliance.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 1.71 V

Table 56 • **LVCMOS 1.8 V Receiver Characteristics (Input Buffers)**

	On-Die Termination (ODT)	T_{PY}		T_{PYS}		
		–1	–Std	–1	–Std	Unit
LVCMOS 1.8 V (for DDRIO I/O bank with Fixed Codes)	None	1.968	2.315	2.099	2.47	ns
LVCMOS 1.8 V (for MSIO I/O bank)	None	2.898	3.411	2.883	3.393	ns
	50	3.05	3.59	3.044	3.583	ns
	75	2.999	3.53	2.987	3.516	ns
	150	2.947	3.469	2.933	3.452	ns
LVCMOS 1.8 V (for MSIOD I/O bank)	None	2.611	3.071	2.598	3.057	ns
	50	2.775	3.264	2.775	3.265	ns
	75	2.72	3.2	2.712	3.19	ns
	150	2.666	3.137	2.655	3.123	ns

Table 118 • DDR1/SSTL2 Class II Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
	–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	Unit
Single-ended	2.29	2.693	1.988	2.338	1.978	2.326	1.989	2.34	1.979	2.328	ns
Differential	2.418	2.846	2.304	2.711	2.297	2.702	2.131	2.506	2.124	2.499	ns

2.3.6.4 Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double date rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 119 • SSTL18 DC Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.71	1.8	1.89	V
Termination voltage	V_{TT}	0.838	0.900	0.964	V
Input reference voltage	V_{REF}	0.838	0.900	0.964	V

Table 120 • SSTL18 DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input logic high	V_{IH} (DC)	V_{REF} + 0.125	1.89	V
DC input logic low	V_{IL} (DC)	–0.3	V_{REF} – 0.125	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

[1] See Table 24, page 22.

Table 121 • SSTL18 DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
SSTL18 Class I (DDR2 Reduced Drive)				
DC output logic high	V_{OH}	V_{TT} + 0.603		V
DC output logic low	V_{OL}		V_{TT}– 0.603	V
Output minimum source DC current (DDRIO I/O bank only)	I_{OH} at V_{OH}	6.5		mA
Output minimum sink current (DDRIO I/O bank only)	I_{OL} at V_{OL}	–6.5		mA
SSTL18 Class II (DDR2 Full Drive)[1]				
DC output logic high	V_{OH}	V_{TT} + 0.603		V
DC output logic low	V_{OL}		V_{TT}– 0.603	V
Output minimum source DC current (DDRIO I/O bank only)	I_{OH} at V_{OH}	13.4		mA
Output minimum sink current (DDRIO I/O bank only)	I_{OL} at V_{OL}	–13.4		mA

[1] To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.

Table 150 • **LPDDR Full Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

	T_{DP}		T_{ENZL}		T_{ENZH}		T_{ENHZ}		T_{ENLZ}		
	–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.171	2.555	2.17	2.554	ns
Differential	2.298	2.703	2.288	2.692	2.288	2.692	2.593	3.051	2.593	3.051	ns

Minimum and Maximum DC/AC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode

Table 151 • **LPDDR-LVCMOS 1.8 V Mode Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.710	1.8	1.89	V

Table 152 • **LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	V_{IH} (DC)	0.65 × V_{DDI}	1.89	V
DC input logic high (for MSIO I/O bank)	V_{IH} (DC)	0.65 × V_{DDI}	3.45	V
DC input logic low	V_{IL} (DC)	–0.3	0.35 × V_{DDI}	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

1. See Table 24, page 22.

Table 153 • **LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	V_{DDI} – 0.45		V
DC output logic low	V_{OL}		0.45	V

Table 154 • **LPDDR-LVCMOS 1.8 V Minimum and Maximum AC Switching Speeds**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	400	Mbps	AC loading: 17pf load, 8 ma drive and above/all slew

Table 155 • **LPDDR-LVCMOS 1.8 V Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CAL	75, 60, 50, 33, 25, 20	Ω

2.3.7.5 RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

Minimum and Maximum Input and Output Levels

Table 203 • **RSDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V

Table 204 • **RSDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	2.925	V

Table 205 • **RSDS DC Output Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 206 • **RSDS Differential Voltage Specification**

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing	V_{OD}	100	600	mV
Output common mode voltage	V_{OCM}	0.5	1.5	V
Input common mode voltage	V_{ICM}	0.3	1.5	V
Input differential voltage	V_{ID}	100	600	mV

Table 207 • **RSDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	520	Mbps	AC loading: 2 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	700	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 208 • **RSDS AC Impedance Specifications**

Parameter	Symbol	Typ	Unit
Termination resistance	RT	100	Ω

Table 209 • **RSDS AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF

Table 221* •   Input DDR Propagation Delays *(continued)

Symbol	**Description**	**Measuring Nodes (from, to)**	**–1**	**–Std**	**Unit**
$T_{DDRIWAL}$	Asynchronous load minimum pulse width for input DDR	F, F	0.304	0.357	ns
$T_{DDRICKMPWH}$	Clock minimum pulse width high for input DDR	B, B	0.075	0.088	ns
$T_{DDRICKMPWL}$	Clock minimum pulse width low for input DDR	B, B	0.159	0.187	ns

2.3.9.4 Output DDR Module

Figure 12 • **Output DDR Module**

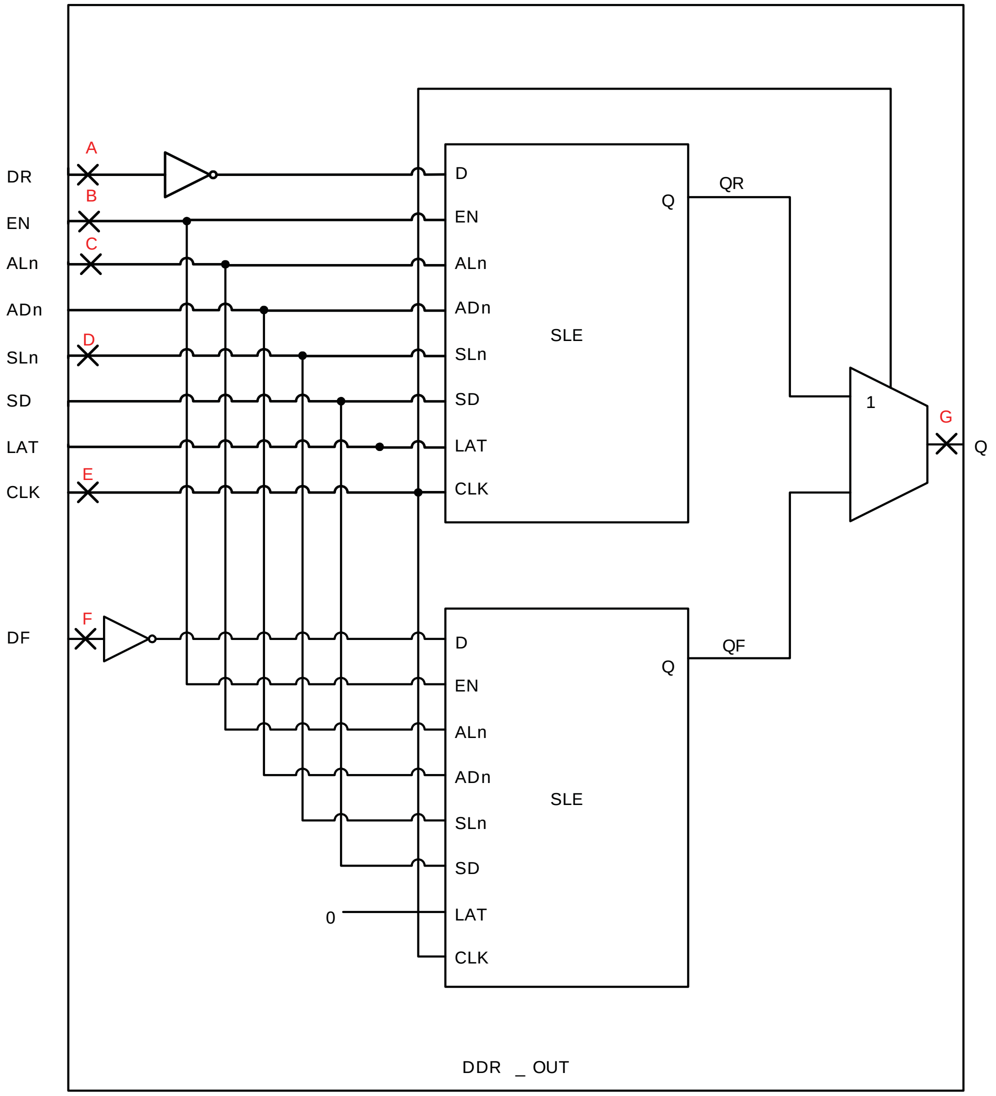
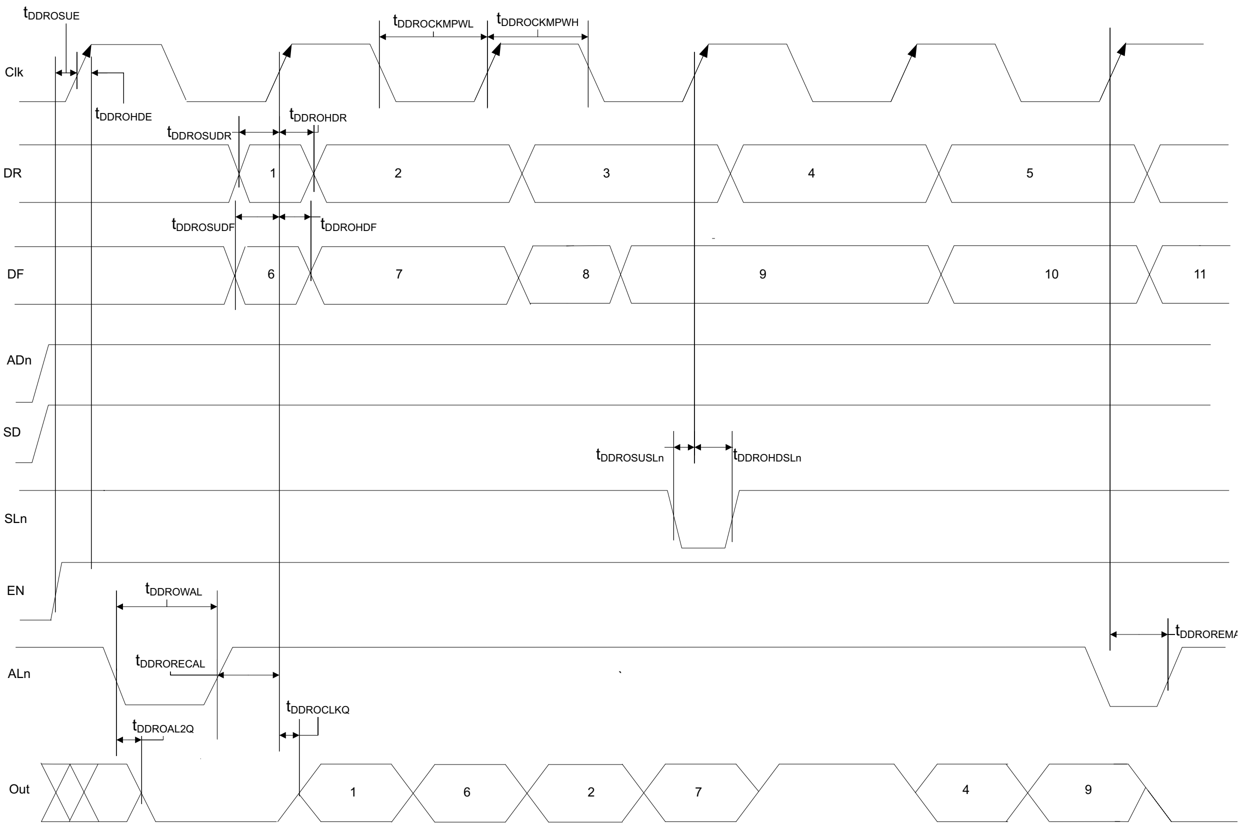


Figure 13 • Output DDR Timing Diagram



2.3.9.5 Timing Characteristics

The following table lists the output DDR propagation delays in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 222 • Output DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	–1	–Std	Unit
$T_{DDROCLKQ}$	Clock-to-out of DDR for output DDR	E, G	0.263	0.309	ns
$T_{DDROSUDF}$	Data_F data setup for output DDR	F, E	0.143	0.168	ns
$T_{DDROSUDR}$	Data_R data setup for output DDR	A, E	0.19	0.223	ns
$T_{DDROHDF}$	Data_F data hold for output DDR	F, E	0	0	ns
$T_{DDROHDR}$	Data_R data hold for output DDR	A, E	0	0	ns
$T_{DDROSUE}$	Enable setup for input DDR	B, E	0.419	0.493	ns
T_{DDROHE}	Enable hold for input DDR	B, E	0	0	ns
$T_{DDROSUSLN}$	Synchronous load setup for input DDR	D, E	0.196	0.231	ns
$T_{DDROHSLN}$	Synchronous load hold for input DDR	D, E	0	0	ns
$T_{DDROAL2Q}$	Asynchronous load-to-out for output DDR	C, G	0.528	0.621	ns
$T_{DDROREMAL}$	Asynchronous load removal time for output DDR	C, E	0	0	ns
$T_{DDRORECAL}$	Asynchronous load recovery time for output DDR	C, E	0.034	0.04	ns

2.3.12.2 FPGA Fabric Micro SRAM (μSRAM)

The following table lists the μSRAM in 64 × 18 mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 237 • **μSRAM (RAM64x18) in 64 × 18 Mode**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		–0.778		–0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.839		0.987	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns

Table 237 • **μSRAM (RAM64x18) in 64 × 18 Mode *(continued)***

Parameter	Symbol	–1 Min	–1 Max	–Std Min	–Std Max	Unit
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μSRAM in 64 × 16 mode in worst commercial-case conditions when $T_J = 85$ °C, $V_{DD} = 1.14$ V.

Table 238 • **μSRAM (RAM64x16) in 64 × 16 Mode**

Parameter	Symbol	–1 Min	–1 Max	–Std Min	–Std Max	Unit
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		–0.778		–0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.983	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns

Table 248 • **2 Step IAP Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	137536	2	37	5	Sec
010	274816	4	76	11	Sec
025	274816	4	78	10	Sec
050	278528	3	85	9	Sec
060	268480	5	76	22	Sec
090	544496	10	152	43	Sec
150	544496	10	153	44	Sec

Table 249 • **2 Step IAP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	6	56	11	Sec
010	842688	11	100	21	Sec
025	1497408	19	113	32	Sec
050	2695168	32	136	48	Sec
060	2686464	43	137	70	Sec
090	4190208	68	236	115	Sec
150	6682768	109	286	162	Sec

Table 250 • **SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	302672	6	19	8	Sec
010	568784	10	26	14	Sec
025	1223504	21	39	29	Sec
050	2424832	39	60	50	Sec
060	2418896	44	65	54	Sec
090	3645968	66	90	79	Sec
150	6139184	108	140	128	Sec

Table 251 • **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	137536	3	42	4	Sec
010	274816	4	82	7	Sec
025	274816	4	82	8	Sec
050	278528	4	80	8	Sec
060	268480	6	80	8	Sec
090	544496	10	157	15	Sec

2.3.14 Math Block Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC math block supports 18×18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently. The following table lists the math blocks with all registers used in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 268 **• Math Blocks with all Registers Used**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input, control register setup time	T_{MISU}	0.149		0.176		ns
Input, control register hold time	T_{MIHD}	1.68		1.976		ns
CDIN input setup time	$T_{MOCDINSU}$	0.185		0.218		ns
CDIN input hold time	$T_{MOCDINHD}$	0.08		0.094		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	–0.419		–0.493		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	0.011		0.013		ns
Asynchronous reset removal time	$T_{MARSTREM}$	0		0		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.088		0.104		ns
Output register clock to out delay	T_{MOCQ}		0.232		0.273	ns
CLK minimum period	T_{MCLKMP}	2.245		2.641		ns

The following table lists the math blocks with input bypassed and output registers used in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 269 **• Math Block with Input Bypassed and Output Registers Used**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Output register setup time	T_{MOSU}	2.294		2.699		ns
Output register hold time	T_{MOHD}	1.68		1.976		ns
CDIN input setup time	$T_{MOCDINSU}$	0.115		0.136		ns
CDIN input hold time	$T_{MOCDINHD}$	–0.444		–0.522		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	–0.419		–0.493		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	0.011		0.013		ns
Asynchronous reset removal time	$T_{MARSTREM}$	0		0		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.014		0.017		ns
Output register clock to out delay	T_{MOCQ}		0.232		0.273	ns
CLK minimum period	T_{MCLKMP}	2.179		2.563		ns

2.3.20 On-Chip Oscillator

The following tables describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

Table 280 • **Electrical Characteristics of the 50 MHz RC Oscillator**

Parameter	Symbol	Typ	Max	Unit	Condition
Operating frequency	F50RC	50		MHz	
Accuracy	ACC50RC	1	4	%	050 devices
		1	5	%	005, 025, and 060 devices
		1	6.3	%	090 devices
		1	7.1	%	010 and 150 devices
Output duty cycle	CYC50RC	49–51	46.5–53.5	%	
Output jitter (peak to peak)	JIT50RC				Period Jitter
		200	300	ps	005, 010, 050, and 060 devices
		200	400	ps	150 devices
		300	500	ps	025 and 090 devices
					Cycle-to-Cycle Jitter
		200	300	ps	005 and 050 devices
		320	420	ps	010, 060, and 150 devices
		320	850	ps	025 and 090 devices
Operating current	IDYN50RC	6.5		mA	

Table 281 • **Electrical Characteristics of the 1 MHz RC Oscillator**

Parameter	Symbol	Typ	Max	Unit	Condition
Operating frequency	F1RC	1		MHz	
Accuracy	ACC1RC	1	3	%	005, 010, 025, and 050 devices
		1	4.5	%	060, and 150 devices
		1	5.6	%	090 devices
Output duty cycle	CYC1RC	49–51	46.5–53.5	%	005, 010, 025, 050, 090 and 150 devices
		49-51	46.0-54.0	%	060 devices
Output jitter (peak to peak)	JIT1RC				Period Jitter
		10	20	ns	005, 010, 025, and 050 devices
		10	28	ns	060, 090 and 150 devices
					Cycle-to-Cycle Jitter
		10	20	ns	005, 010, and 050 devices
		10	35	ns	025, 060, and 150 devices
		10	45	ns	090 devices
Operating current	IDYN1RC	0.1		mA	
Startup time	SU1RC		17	µs	050, 090, and 150 devices
			18	µs	005, 010, and 025 devices

2.3.24 Power-up to Functional Times

The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 288 • **Power-up to Functional Times for SmartFusion2**

				Maximum Power-up to Functional Time for SmartFusion2 (uS)						
Symbol	**From**	**To**	**Description**	**005**	**010**	**025**	**050**	**060**	**090**	**150**
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	647	500	531	483	474	524	647
$T_{POR2MSSRST}$	POWER_ON_RESET_N	MSS_RESET_N_M2F	Fabric to MSS	644	497	528	480	468	518	641
$T_{MSSRST2OUT}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.6	3.6	3.6	3.4	4.9	4.8	4.8
$T_{VDD2OUT}$	V_{DD}	Output available at I/O	V_{DD} at its minimum threshold level to output	3096	2975	3012	2959	2869	2992	3225
$T_{VDD2POR}$	V_{DD}	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	2476	2487	2496	2486	2406	2563	2602
$T_{VDD2MSSRST}$	V_{DD}	MSS_RESET_N_M2F	V_{DD} at its minimum threshold level to MSS	3093	2972	3008	2956	2864	2987	3220
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

2.3.31.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, see Figure 22, page 128.

The following table lists the SPI characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V

Table 305 • **SPI Characteristics for All Devices**

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPIFMAX	Maximum operating frequency of SPI interface			20	MHz	
sp1	SPI_[0|1]_CLK minimum period					
	SPI_[0|1]_CLK = PCLK/2	12			ns	
	SPI_[0|1]_CLK = PCLK/4	24.1			ns	
	SPI_[0|1]_CLK = PCLK/8	48.2			ns	
	SPI_[0|1]_CLK = PCLK/16	0.1			µs	
	SPI_[0|1]_CLK = PCLK/32	0.19			µs	
	SPI_[0|1]_CLK = PCLK/64	0.39			µs	
	SPI_[0|1]_CLK = PCLK/128	0.77			µs	
sp2	SPI_[0|1]_CLK minimum pulse width high					
	SPI_[0|1]_CLK = PCLK/2	6			ns	
	SPI_[0|1]_CLK = PCLK/4	12.05			ns	
	SPI_[0|1]_CLK = PCLK/8	24.1			ns	
	SPI_[0|1]_CLK = PCLK/16	0.05			µs	
	SPI_[0|1]_CLK = PCLK/32	0.095			µs	
	SPI_[0|1]_CLK = PCLK/64	0.195			µs	
	SPI_[0|1]_CLK = PCLK/128	0.385			µs	
sp3	SPI_[0|1]_CLK minimum pulse width low					
	SPI_[0|1]_CLK = PCLK/2	6			ns	
	SPI_[0|1]_CLK = PCLK/4	12.05			ns	
	SPI_[0|1]_CLK = PCLK/8	24.1			ns	
	SPI_[0|1]_CLK = PCLK/16	0.05			µs	
	SPI_[0|1]_CLK = PCLK/32	0.095			µs	
	SPI_[0|1]_CLK = PCLK/64	0.195			µs	
	SPI_[0|1]_CLK = PCLK/128	0.385			µs	
sp4	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS rise time (10%–90%)[1]		2.77		ns	I/O Configuration: LVCMOS 2.5 V–8 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C

Table 305 • SPI Characteristics for All Devices *(continued)*

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp5	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS fall time (10%–90%)[1]		2.906		ns	IO Configuration: LVCMOS 2.5 V-8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0|1]_DI setup time[2]	12			ns	
sp9m	SPI_[0|1]_DI hold time[2]	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0|1]_DI setup time[2]	2			ns	
sp9s	SPI_[0|1]_DI hold time[2]	7			ns	
SPI master configuration (applicable for 060, 090, and 150 devices)						
sp6m	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 7.0			ns	
sp7m	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) – 9.5			ns	
sp8m	SPI_[0|1]_DI setup time[2]	15			ns	
sp9m	SPI_[0|1]_DI hold time[2]	—2.5			ns	
SPI slave configuration (applicable for 060, 090, and 150 devices)						
sp6s	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 16.0			ns	
sp7s	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) - 3.5			ns	
sp8s	SPI_[0|1]_DI setup time[2]	3			ns	
sp9s	SPI_[0|1]_DI hold time[2]	2.5			ns	

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. For allowable pclk configurations, see Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.