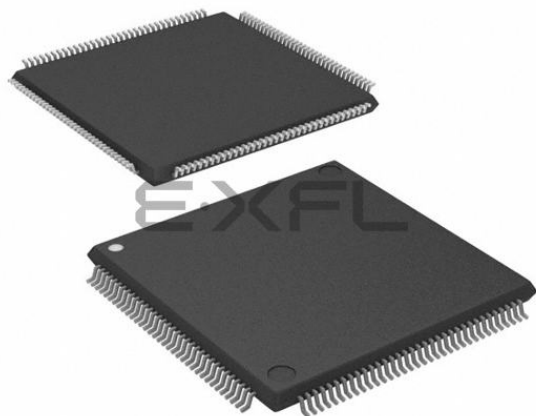




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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	64KB
Peripherals	-
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 5K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s005-1tq144

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- Updated Table 24, page 22 with minimum and maximum values for input current low and high (SAR 73114 and 80314).
- Added Non-Deterministic Random Bit Generator (NRBG) Characteristics, page 106 (SAR 73114 and 79517).
- Added 060 device in Table 282, page 110 (SAR 79860).
- Added DEVRST_N to Functional Times, page 116 (SAR 73114).
- Added Cryptographic Block Characteristics, page 106 (SAR 73114 and 79516).
- Update Table 296, page 121 with VTX-AMP details (SAR 81756).
- Update note in Table 297, page 122 (SAR 74570 and 80677).
- Update Table 298, page 122 with generic EPCS details (SAR 75307).
- Added Table 308, page 129 (SAR 50424).

1.2 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- The Surge Current on VDD during DEVRST_B Assertion and Surge Current on VDD during Digest Check using System Services tables were deleted and added reference to *AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note*. (SAR 76865 and 76623).
- Added 060 device in Table 4, page 6 (SAR 76383).
- Updated Table 24, page 22 for ramp time input (SAR 72103).
- Added 060 device details in Table 284, page 112 (SAR 74927).
- Updated Table 290, page 116 for name change (SAR 74925).
- Updated Table 283, page 111 for 060 FG676 Package details (SAR 78849).
- Updated Table 305, page 126 for SmartFusion2 and Table 310, page 129 for IGLOO2 for SPI timing and Fmax (SAR 56645, 75331).
- Updated Table 293, page 119 for Flash*Freeze entry and exit times (SAR 75329, 75330).
- Updated Table 297, page 122 for RX-CID information (SAR 78271).
- Added Table 8, page 8 and Figure 1, page 9 (SAR 78932).
- Updated Table 223, page 76 for timing characteristics and Table 224, page 77 (SAR 75998).
- Added SRAM PUF, page 105 (SAR 64406).
- Added a footnote on digest cycle in Table 5, page 7 (SAR 79812).

1.3 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document.

- Added a note in Table 5, page 7 (SAR 71506).
- Added a note in Table 6, page 8 (SAR 74616).
- Added a note in Figure 3, page 17 (SAR 71506).
- Updated Quiescent Supply Current for 060 in Table 11, page 12 and Table 12, page 13 (SAR 74483).
- Updated programming currents for 060 in Table 13, page 13, Table 14, page 13, and Table 15, page 14.
- Added DEVRST_B assertion tables (SAR 74708).
- Updated I/O speeds for LVDS 3.3 V in Table 18, page 19 and Table 21, page 20 (SAR 69829).
- Updated Table 24, page 22 (SAR 69418).
- Updated Table 25, page 22, Table 26, page 23, Table 27, page 23 (SAR 74570).
- Updated all AC/DC table to link to the Input Capacitance, Leakage Current, and Ramp Time, page 22 for reference (SAR 69418).

The following table lists the embedded operating flash limits.

Table 6 • Embedded Operating Flash Limits

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Commercial	Embedded flash	Min $T_J = 0\text{ }^{\circ}\text{C}$ Max $T_J = 85\text{ }^{\circ}\text{C}$	Min $T_J = 0\text{ }^{\circ}\text{C}$ Max $T_J = 85\text{ }^{\circ}\text{C}$	< 1000 cycles per page, up to two million cycles per eNVM array	20 years
			Min $T_J = 0\text{ }^{\circ}\text{C}$ Max $T_J = 85\text{ }^{\circ}\text{C}$	< 10000 cycles per page, up to 20 million cycles per eNVM array	10 years
Industrial	Embedded flash	Min $T_J = -40\text{ }^{\circ}\text{C}$ Max $T_J = 100\text{ }^{\circ}\text{C}$	Min $T_J = -40\text{ }^{\circ}\text{C}$ Max $T_J = 100\text{ }^{\circ}\text{C}$	< 1000 cycles per page, up to two million cycles per eNVM array	20 years
			Min $T_J = -40\text{ }^{\circ}\text{C}$ Max $T_J = 100\text{ }^{\circ}\text{C}$	< 10000 cycles per page, up to 20 million cycles per eNVM array	10 years

Note: If your product qualification requires accelerated programming cycles, see *Microsemi SoC Products Quality and Reliability Report* about recommended methodologies.

Table 7 • Device Storage Temperature and Retention

Product Grade	Storage Temperature (T_{stg})	Retention
Commercial	Min $T_J = 0\text{ }^{\circ}\text{C}$ Max $T_J = 85\text{ }^{\circ}\text{C}$	20 years
Industrial	Min $T_J = -40\text{ }^{\circ}\text{C}$ Max $T_J = 100\text{ }^{\circ}\text{C}$	20 years

Table 8 • High Temperature Data Retention (HTR) Lifetime

T_J (C)	HTR Lifetime ¹ (yrs)
90	20.5
95	20.5
100	20.5
105	17.0
110	15.0
115	13.0
120	11.5
125	10.0
130	8.0
135	6.0
140	4.5
145	3.0
150	1.5

1. HTR Lifetime is the period during which a verify failure is not expected due to flash leakage.

2.3.2 Power Consumption

The following sections describe the power consumptions of the devices.

2.3.2.1 Quiescent Supply Current

Table 10 • Quiescent Supply Current Characteristics

Power Supplies/Blocks	Modes and Configurations	
	Non-Flash*Freeze	Flash*Freeze
FPGA Core	On	Off
V _{DD} /SERDES_[01]_VDD ¹	On	On
V _{PP} /V _{PPNVM}	On	On
HPMS_MDDR_PLL_VDDA/FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA/PLL0_PLL1_HPMS_MDDR_VDD A	0 V	0 V
SERDES_[01]_PLL_VDDA ²	0 V	0 V
SERDES_[01]_L[0123]_VDDAPLL/VDD_2V5 ²	On	On
SERDES_[01]_L[0123]_VDDAIIO ²	On	On
V _{DDI_x} ^{3, 4}	On	On
V _{REFx}	On	On
MSSDDR CLK	32 kHz	32 kHz
RAM	On	Sleep state
System controller	50 MHz	50 MHz
50 MHz oscillator (enable/disable)	Enable	Disabled
1 MHz oscillator (enable/disable)	Disabled	Disabled
Crystal oscillator (enable/disable)	Disabled	Disabled

1. SERDES_[01]_VDD Power Supply is shorted to V_{DD}.
2. SerDes and DDR blocks to be unused.
3. V_{DDI_x} has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate V_{DDI} bank supplies. For details on bank power supplies, see "Recommendation for Unused Bank Supplies" table in the AC393: *SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.
4. No Differential (that is to say, LVDS) I/Os or ODT attributes to be used.

Table 11 • SmartFusion2 and IGLOO2 Quiescent Supply Current (V_{DD} = 1.2 V) – Typical Process

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC1	Non-Flash*Freeze	6.2	6.9	8.9	13.1	15.3	15.4	27.5	mA	Typical (T _J = 25 °C)
		24.0	28.4	40.6	67.8	80.6	81.4	144.7	mA	Commercial (T _J = 85 °C)
		35.2	41.9	60.5	102.1	121.4	122.6	219.1	mA	Industrial (T _J = 100 °C)

Table 34 • LVTTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.4	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 35 • LVTTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank

Output Drive Selection	V_{OH} (V)	V_{OL} (V)	IOH (at V_{OH}) mA	IOL (at V_{OL}) mA
2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	$V_{DDI} - 0.4$	0.4	4	4
8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA	$V_{DDI} - 0.4$	0.4	16	16
20 mA	$V_{DDI} - 0.4$	0.4	20	20

Note: For a detailed I/V curve, use the corresponding IBIS models:
www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.0\text{ V}$

Table 36 • LVTTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	2.262	2.663	2.289	2.695	ns

Table 37 • LVTTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.192	3.755	3.47	4.083	2.969	3.494	1.856	2.183	3.337	3.926	ns
4 mA	Slow	2.331	2.742	2.673	3.145	2.526	2.973	3.034	3.569	4.451	5.236	ns
8 mA	Slow	2.135	2.511	2.33	2.741	2.297	2.703	4.532	5.331	4.825	5.676	ns
12 mA	Slow	2.052	2.414	2.107	2.479	2.162	2.544	5.75	6.764	5.445	6.406	ns
16 mA	Slow	2.062	2.425	2.072	2.438	2.145	2.525	5.993	7.05	5.625	6.618	ns
20 mA	Slow	2.148	2.527	1.999	2.353	2.088	2.458	6.262	7.367	5.876	6.913	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 43 • LVCMOS 2.5 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.2	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	$\Omega\sigma$
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 44 • LVCMOS 2.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (With Software Default Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	4 mA	4 mA	$V_{DDI} - 0.4$	0.4	4	4
6 mA	6 mA	6 mA	$V_{DDI} - 0.4$	0.4	6	6
8 mA	8 mA	8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	12 mA	12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA		16 mA	$V_{DDI} - 0.4$	0.4	16	16

Note: For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at:
www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 45 • LVCMOS 2.5 V Receiver Characteristics (Input Buffers)

	On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
		-1	-Std	-1	-Std	
LVCMOS 2.5 V (for DDRIO I/O bank)	None	1.823	2.145	1.932	2.274	ns
LVCMOS 2.5 V (for MSIO I/O bank)	None	2.486	2.925	2.495	2.935	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	None	2.29	2.694	2.305	2.712	ns

Table 46 • LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.657	4.302	3.393	3.991	3.675	4.323	3.894	4.582	3.552	4.18	ns
	Medium	3.374	3.97	3.139	3.693	3.396	3.995	3.635	4.277	3.253	3.828	ns
	Medium fast	3.239	3.811	3.036	3.572	3.261	3.836	3.519	4.141	3.128	3.681	ns
	Fast	3.224	3.793	3.029	3.563	3.246	3.818	3.512	4.132	3.119	3.67	ns

Table 57 • LVCMOS 1.8 V Transmitter Characteristics for DDRIO I/O Bank with Fixed Code (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	Medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	Medium fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	Fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4 mA	Slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	Medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	Medium fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	Fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6 mA	Slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	Medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	Medium fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	Fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns
8 mA	Slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns
	Medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	Medium fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	Fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10 mA	Slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	Medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	Medium fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	Fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12 mA	Slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	Medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	Medium fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	Fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16 mA	Slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	Medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	Medium fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	Fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 100 • HSTL AC Test Parameter Specification

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.75	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for HSTL15 Class I (T_{DP})	RTT_TEST	50	Ω
Reference resistance for data test path for HSTL15 Class II (T_{DP})	RTT_TEST	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst-case commercial conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, worst-case V_{DDI} .

Table 101 • HSTL Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)

		T_{PY}		Unit
On-Die Termination (ODT)		-1	-Std	
Pseudo differential	None	1.605	1.888	ns
	47.8	1.614	1.898	ns
True differential	None	1.622	1.909	ns
	47.8	1.628	1.916	ns

Table 102 • HSTL Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ}		T _{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
HSTL Class I											
Single-ended	2.6	3.059	2.514	2.958	2.514	2.958	2.431	2.86	2.431	2.86	ns
Differential	2.621	3.083	2.648	3.115	2.647	3.113	2.925	3.442	2.923	3.44	ns
HSTL Class II											
Single-ended	2.511	2.954	2.488	2.927	2.49	2.93	2.409	2.833	2.411	2.836	ns
Differential	2.528	2.974	2.552	3.003	2.551	3.001	2.897	3.409	2.896	3.408	ns

2.3.6.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

Table 168 • LVDS25 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.554	3.004	ns
100	2.549	2.999	ns

Table 169 • LVDS25 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.136	2.513	2.416	2.842	2.402	2.825	2.423	2.85	2.409	2.833	ns

Table 170 • LVDS25 Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
No pre-emphasis	1.61	1.893	1.749	2.058	1.735	2.041	1.897	2.231	1.866	2.195	ns
Min pre-emphasis	1.527	1.796	1.757	2.067	1.744	2.052	1.905	2.241	1.876	2.207	ns
Med pre-emphasis	1.496	1.76	1.765	2.077	1.751	2.06	1.914	2.252	1.884	2.216	ns

LVDS33 AC Switching Characteristics**Table 171 • LVDS33 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

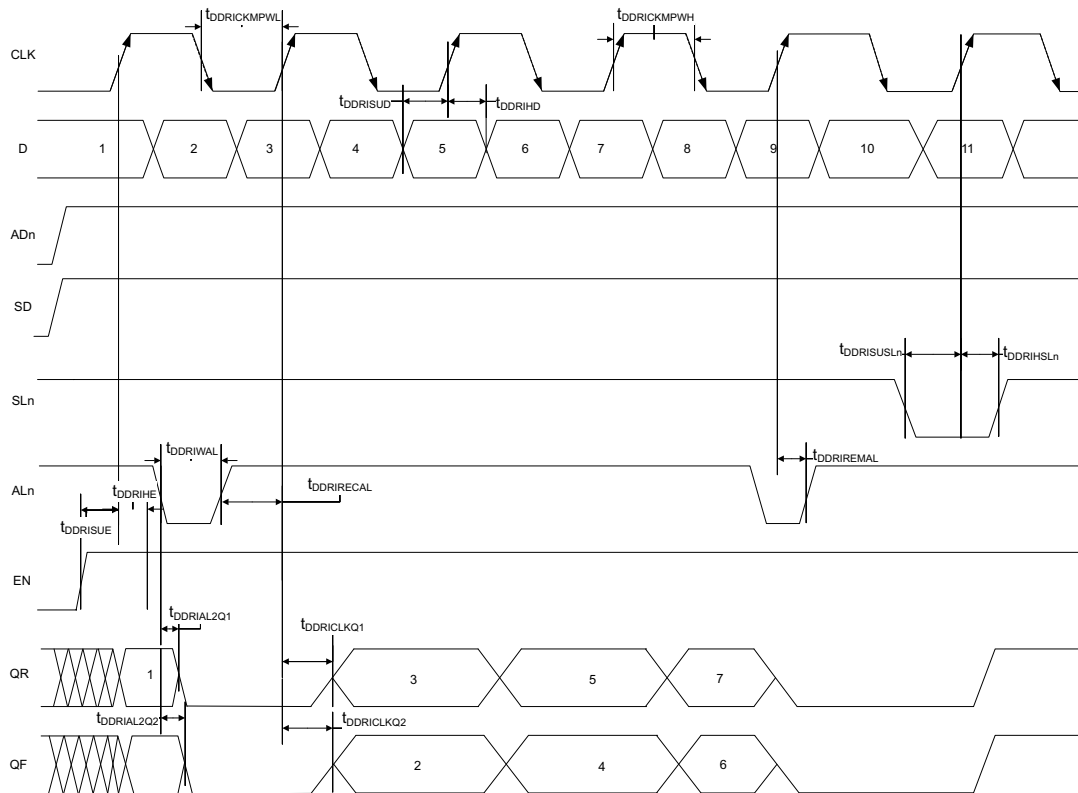
On Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.572	3.025	ns
100	2.569	3.023	ns

Table 172 • LVDS33 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
1.942	2.284	1.98	2.33	1.97	2.318	1.953	2.298	1.96	2.307	ns

2.3.9.2 Input DDR Timing Diagram

Figure 11 • Input DDR Timing Diagram



2.3.9.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 221 • Input DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDRICKQ1}$	Clock-to-Out Out_QR for input DDR	B, C	0.16	0.188	ns
$T_{DDRICKQ2}$	Clock-to-Out Out_QF for input DDR	B, D	0.166	0.195	ns
$T_{DDRISUD}$	Data setup for input DDR	A, B	0.357	0.421	ns
T_{DDRIHD}	Data hold for input DDR	A, B	0	0	ns
$T_{DDRISUE}$	Enable setup for input DDR	E, B	0.46	0.542	ns
T_{DDRIHE}	Enable hold for input DDR	E, B	0	0	ns
$T_{DDRISUSLn}$	Synchronous load setup for input DDR	G, B	0.46	0.542	ns
$T_{DDRIHSLn}$	Synchronous load hold for input DDR	G, B	0	0	ns
$T_{DDRIAL2Q1}$	Asynchronous load-to-out QR for input DDR	F, C	0.587	0.69	ns
$T_{DDRIAL2Q2}$	Asynchronous load-to-out QF for input DDR	F, D	0.541	0.636	ns
$T_{DDRIREMAL}$	Asynchronous load removal time for input DDR	F, B	0	0	ns
$T_{DDRIRECAL}$	Asynchronous load recovery time for input DDR	F, B	0.074	0.087	ns

The following table lists the 010 device global resources in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 229 • 010 Device Global Resource

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.626	0.669	0.627	0.668	ns
Input high delay for global clock	T_{RCKH}	1.112	1.182	1.308	1.393	ns
Maximum skew for global clock	T_{RCKSW}		0.07		0.085	ns

The following table lists the 005 device global resources in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 230 • 005 Device Global Resource

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.625	0.66	0.628	0.66	ns
Input high delay for global clock	T_{RCKH}	1.126	1.187	1.325	1.397	ns
Maximum skew for global clock	T_{RCKSW}		0.061		0.072	ns

2.3.12 FPGA Fabric SRAM

See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for more information.

2.3.12.1 FPGA Fabric Large SRAM (LSRAM)

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 1K × 18 in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 231 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register			0.334		0.393	ns
Read access time without pipeline register	T_{CLK2Q}		2.273		2.674	ns
Access time with feed-through write timing			1.529		1.799	ns
Address setup time	T_{ADDRSU}	0.441		0.519		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.341		0.401		ns
Data hold time	T_{DHD}	0.107		0.126		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 16K × 1 in worst commercial-case conditions when $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 235 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register			0.32		0.377	ns
Read access time without pipeline register	T_{CLK2Q}		2.269		2.669	ns
Access time with feed-through write timing			1.51		1.777	ns
Address setup time	T_{ADDRSU}	0.626		0.737		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.322		0.378		ns
Data hold time	T_{DHD}	0.082		0.096		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		1.51		1.777	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.53		0.624		ns
Read enable hold time	T_{RDEHD}	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}		1.547		1.82	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.454		0.534		ns
Write enable hold time	T_{WEHD}	0.048		0.057		ns
Maximum frequency	F_{MAX}		400		340	MHz

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 270 • Math Block with Input Register Used and Output in Bypass Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input register setup time	T_{MISU}	0.149		0.176		ns
Input register hold time	T_{MIHD}	0.185		0.218		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	0.08		0.094		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	-0.012		-0.014		ns
Asynchronous reset removal time	$T_{MARSTREM}$	-0.005		-0.005		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.088		0.104		ns
Input register clock to output delay	T_{MICQ}		2.52		2.964	ns
CDIN to output delay	$T_{MCDIN2Q}$		1.951		2.295	ns

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 271 • Math Block with Input and Output in Bypass Mode

Parameter	Symbol	-1	-Std	Unit
		Max	Max	
Input to output delay	T_{MIQ}	2.568	3.022	ns
CDIN to output delay	$T_{MCDIN2Q}$	1.951	2.295	ns

2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when $V_{DD} = 1.14\text{ V}$, $V_{PPNVM} = V_{PP} = 2.375\text{ V}$.

Table 272 • eNVM Read Performance

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
T_J	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$F_{MAXREAD}$	eNVM maximum read frequency	25	25	25	25	25	25	MHz

The following table lists the eNVM page programming in worst-case conditions when $V_{DD} = 1.14\text{ V}$, $V_{PPNVM} = V_{PP} = 2.375\text{ V}$.

Table 273 • eNVM Page Programming

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
T_J	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$T_{PAGEPGM}$	eNVM page programming time	40	40	40	40	40	40	ms

2.3.20 On-Chip Oscillator

The following tables describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

Table 280 • Electrical Characteristics of the 50 MHz RC Oscillator

Parameter	Symbol	Typ	Max	Unit	Condition
Operating frequency	F50RC	50		MHz	
Accuracy	ACC50RC	1	4	%	050 devices
		1	5	%	005, 025, and 060 devices
		1	6.3	%	090 devices
		1	7.1	%	010 and 150 devices
Output duty cycle	CYC50RC	49–51	46.5–53.5	%	
Output jitter (peak to peak)	JIT50RC				Period Jitter
		200	300	ps	005, 010, 050, and 060 devices
		200	400	ps	150 devices
		300	500	ps	025 and 090 devices
					Cycle-to-Cycle Jitter
		200	300	ps	005 and 050 devices
		320	420	ps	010, 060, and 150 devices
		320	850	ps	025 and 090 devices
Operating current	IDYN50RC	6.5		mA	

Table 281 • Electrical Characteristics of the 1 MHz RC Oscillator

Parameter	Symbol	Typ	Max	Unit	Condition
Operating frequency	F1RC	1		MHz	
Accuracy	ACC1RC	1	3	%	005, 010, 025, and 050 devices
		1	4.5	%	060, and 150 devices
		1	5.6	%	090 devices
Output duty cycle	CYC1RC	49–51	46.5–53.5	%	005, 010, 025, 050, 090 and 150 devices
		49–51	46.0–54.0	%	060 devices
Output jitter (peak to peak)	JIT1RC				Period Jitter
		10	20	ns	005, 010, 025, and 050 devices
		10	28	ns	060, 090 and 150 devices
					Cycle-to-Cycle Jitter
		10	20	ns	005, 010, and 050 devices
		10	35	ns	025, 060, and 150 devices
		10	45	ns	090 devices
Operating current	IDYN1RC	0.1		mA	
Startup time	SU1RC		17	μs	050, 090, and 150 devices
			18	μs	005, 010, and 025 devices

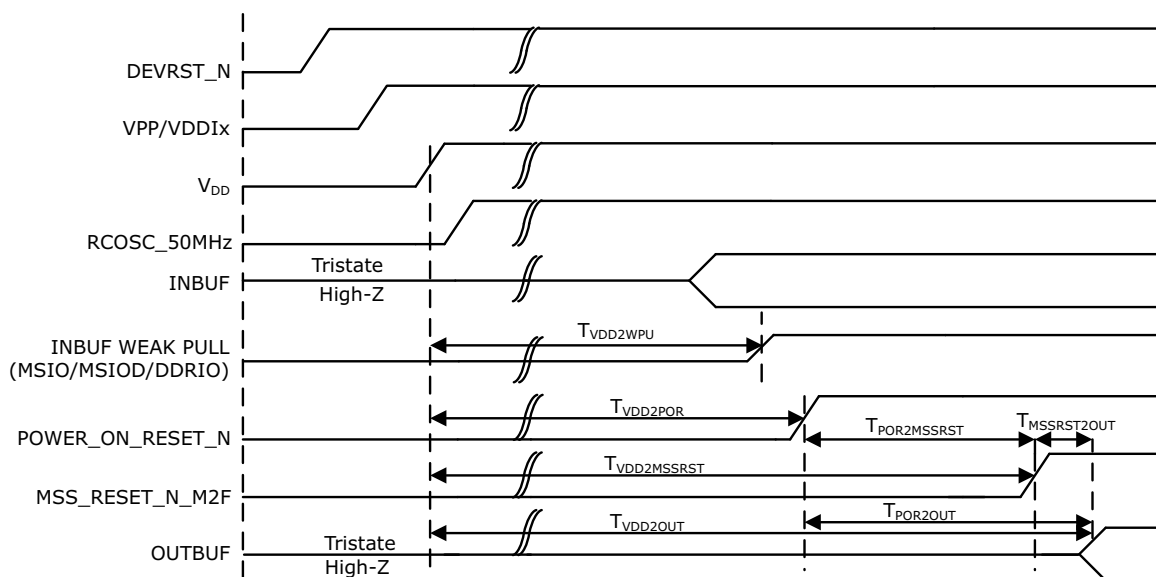
1. The minimum output clock frequency is limited by the PLL. For more information, see *UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide*.
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance is limited by the CCC output frequency.

The following table lists the CCC/PLL jitter specifications in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 283 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications

CCC Output Maximum Peak-to-Peak Period Jitter F _{OUT_CCC}						
Parameter		Conditions/Package Combinations				Unit
10 FG484, 050 FG896/FG484/FCS325 Packages ¹	SSO = 0	0 < SSO <= 2	SSO <= 4	SSO <= 8	SSO <= 16	
20 MHz to 100 MHz	Max(110, ± 1% x (1/F _{OUT_CCC}))	Max(150, ± 1% x (1/F _{OUT_CCC}))				ps
100 MHz to 400 MHz	Max(120, ± 1% x (1/F _{OUT_CCC}))	Max(150, ± 1% x (1/F _{OUT_CCC}))			Max(170, ± 1% x (1/F _{OUT_CCC}))	ps
025 FG484/FCS325 Package ¹	0 < SSO <=16					
20 MHz to 74 MHz	± 1% x (1/F _{OUT_CCC}))					ps
74 MHz to 400 MHz	210					ps
005 FG484 Package ¹	0 < SSO <=16					
20 MHz to 53 MHz	± 1% x (1/F _{OUT_CCC}))					ps
53 MHz to 400 MHz	270					ps
090 FG676 and FC325 Package ¹	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x (1/F _{OUT_CCC}))					ps
100 MHz to 400 MHz	150					ps
060 FG676 Package ¹	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x (1/F _{OUT_CCC})					ps
100 MHz to 400 MHz	150					
150 FC1152 Package ¹	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x (1/F _{OUT_CCC}))					ps
100 MHz to 400 MHz	120					ps

1. SSO data is based on LVCMOS 2.5 V MSIO and/or MSIOD bank I/Os.

Figure 17 • Power-up to Functional Timing Diagram for SmartFusion2

The following table lists the IGLOO2 power-up to functional times in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 289 • Power-up to Functional Times for IGLOO2

				Maximum Power-up to Functional Time for IGLOO2 (uS)						
Symbol	From	To	Description	005	010	025	050	060	090	150
T _{POR2OUT}	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	114	114	113	114	114	114
T _{VDD2OUT}	V _{DD}	Output available at I/O	V _{DD} at its minimum threshold level to output	2587	2600	2607	2558	2591	2600	2699
T _{VDD2POR}	V _{DD}	POWER_ON_RESET_N	V _{DD} at its minimum threshold level to fabric	2474	2486	2493	2445	2477	2486	2585
T _{VDD2WPU}	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide*.

Table 303 • I2C Characteristics (continued)

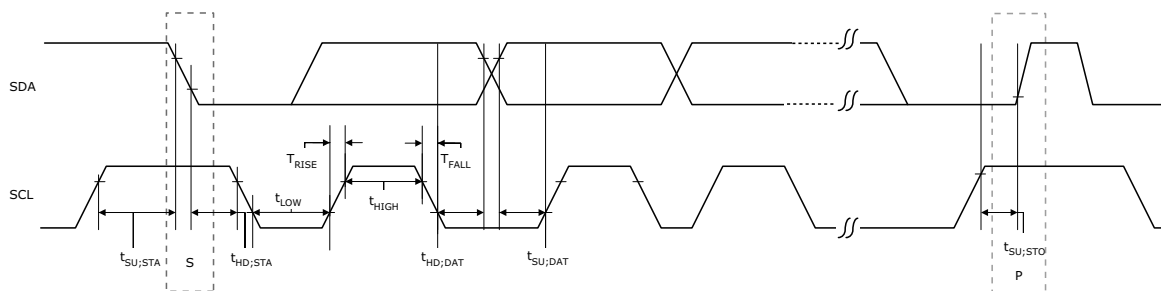
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Maximum data rate	D_{MAX}			400	Kbps	Fast mode
				100	Kbps	Standard mode
Pulse width of spikes which must be suppressed by the input filter	T_{FILT}		50		ns	Fast mode

1. These values are provided for MSIO Bank–LVTTL 8 mA Low Drive at 25 °C, typical conditions. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on V_{DDIX} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
3. $R(PULL-DOWN-MAX) = (VOL_{spec})/IOL_{spec}$.
4. $R(PULL-UP-MAX) = (VDDImax - VOH_{spec})/IOH_{spec}$.

The following table lists the I²C switching characteristics in worst-case industrial conditions when $T_J = 100\text{ °C}$, $V_{DD} = 1.14\text{ V}$

Table 304 • I2C Switching Characteristics

Parameter	Symbol	–1	Std	Unit
		Min	Min	
Low period of I2C_x_SCL	T_{LOW}	1	1	PCLK cycles
High period of I2C_x_SCL	T_{HIGH}	1	1	PCLK cycles
START hold time	$T_{HD;STA}$	1	1	PCLK cycles
START setup time	$T_{SU;STA}$	1	1	PCLK cycles
DATA hold time	$T_{HD;DAT}$	1	1	PCLK cycles
DATA setup time	$T_{SU;DAT}$	1	1	PCLK cycles
STOP setup time	$T_{SU;STO}$	1	1	PCLK cycles

Figure 21 • I²C Timing Parameter Definition

2.3.31.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, see Figure 22, page 128.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Table 305 • SPI Characteristics for All Devices

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPIFMAX	Maximum operating frequency of SPI interface			20	MHz	
sp1	SPI_[0 1]_CLK minimum period					
	SPI_[0 1]_CLK = PCLK/2	12			ns	
	SPI_[0 1]_CLK = PCLK/4	24.1			ns	
	SPI_[0 1]_CLK = PCLK/8	48.2			ns	
	SPI_[0 1]_CLK = PCLK/16	0.1			μs	
	SPI_[0 1]_CLK = PCLK/32	0.19			μs	
	SPI_[0 1]_CLK = PCLK/64	0.39			μs	
	SPI_[0 1]_CLK = PCLK/128	0.77			μs	
sp2	SPI_[0 1]_CLK minimum pulse width high					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			μs	
	SPI_[0 1]_CLK = PCLK/32	0.095			μs	
	SPI_[0 1]_CLK = PCLK/64	0.195			μs	
	SPI_[0 1]_CLK = PCLK/128	0.385			μs	
sp3	SPI_[0 1]_CLK minimum pulse width low					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			μs	
	SPI_[0 1]_CLK = PCLK/32	0.095			μs	
	SPI_[0 1]_CLK = PCLK/64	0.195			μs	
	SPI_[0 1]_CLK = PCLK/128	0.385			μs	
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) ¹		2.77		ns	I/O Configuration: LVCMOS 2.5 V– 8 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C