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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

| | |
|-------------------------|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | ARM® Cortex®-M3 |
| Flash Size | 128KB |
| RAM Size | 64KB |
| Peripherals | DDR |
| Connectivity | CANbus, Ethernet, I ² C, SPI, UART/USART, USB |
| Speed | 166MHz |
| Primary Attributes | FPGA - 5K Logic Modules |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 400-LFBGA |
| Supplier Device Package | 400-VFBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2s005-1vfg400i |

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2 IGLOO2 FPGA and SmartFusion2 SoC FPGA

Microsemi's mainstream SmartFusion[®]2 SoC and IGLOO[®]2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated math blocks, multiple embedded memory blocks, and high-performance SerDes communication interfaces on a single chip. Both families benefit from low-power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to 5 MBs of embedded RAM, up to 16 SerDes lanes, and up to four PCI Express Gen 2 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 devices integrate an entire low-power, real-time microcontroller subsystem (MSS) with a rich set of industry-standard peripherals including Ethernet, USB, and CAN, while IGLOO2 devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

2.1 Device Status

The following table shows the design security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

Table 1 • IGLOO2 and SmartFusion2 Design Security Densities

| Design Security Device Densities | Status |
|----------------------------------|------------|
| 005 | Production |
| 010, 010T | Production |
| 025, 025T | Production |
| 050, 050T | Production |
| 060, 060T | Production |
| 090, 090T | Production |
| 150, 150T | Production |

The following table shows the data security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

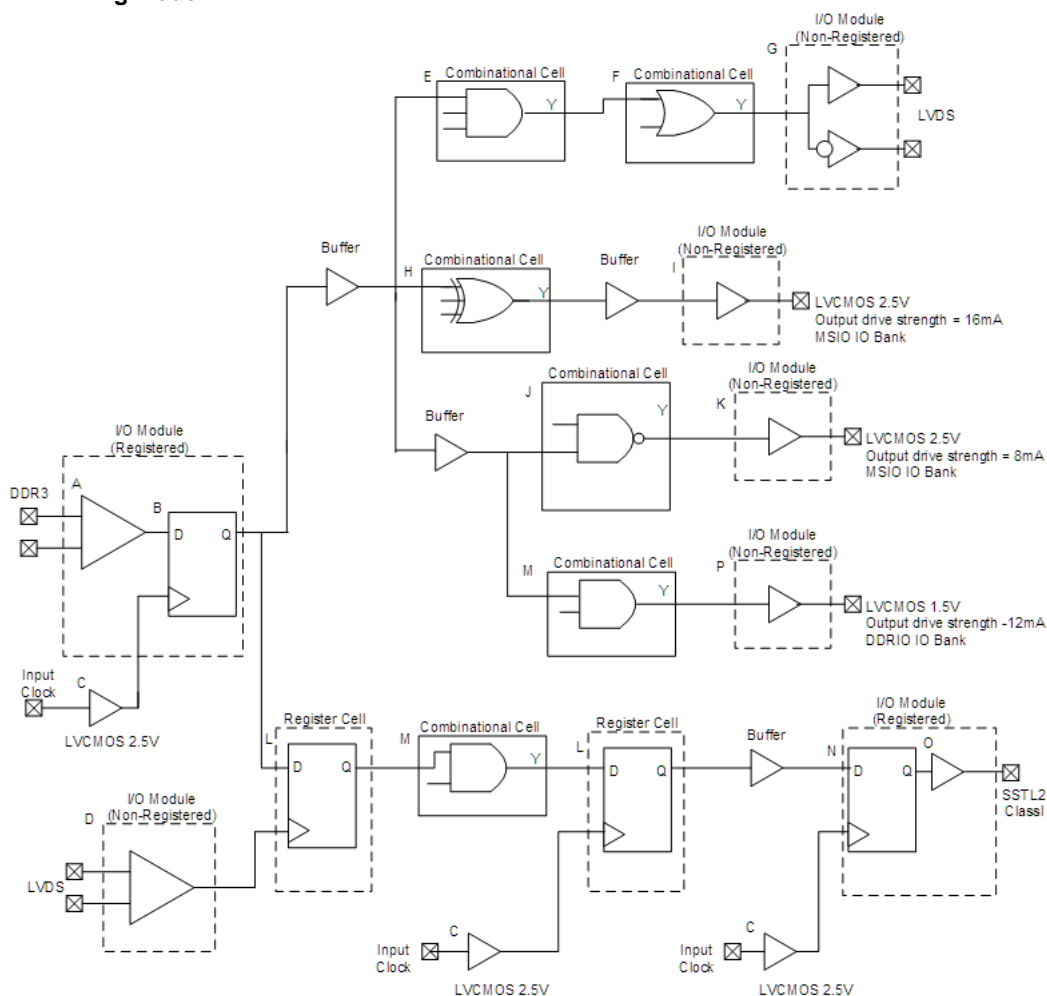
Table 2 • IGLOO2 and SmartFusion2 Data Security Densities

| Data Security Device Densities | Status |
|--------------------------------|------------|
| 005S | Production |
| 010TS | Production |
| 025TS | Production |
| 050TS | Production |
| 060TS | Production |
| 090TS | Production |
| 150TS | Production |

2.3.4 Timing Model

This section describes timing model and timing parameters.

Figure 2 • Timing Model



The following table lists the timing model parameters in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

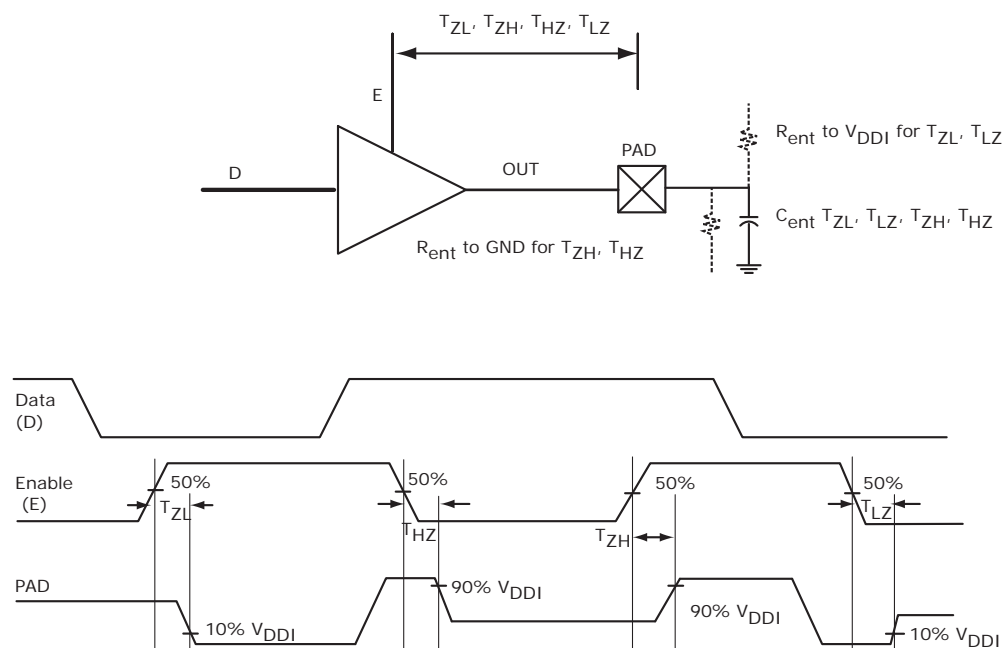
Table 17 • Timing Model Parameters

| Index | Symbol | Description | -1 | Unit | For More Information |
|-------|-------------|---|-------|------|------------------------|
| A | T_{PY} | Propagation delay of DDR3 receiver | 1.605 | ns | See Table 137, page 50 |
| B | T_{ICLKQ} | Clock-to-Q of the input data register | 0.16 | ns | See Table 221, page 71 |
| | T_{ISUD} | Setup time of the input data register | 0.357 | ns | See Table 221, page 71 |
| C | T_{RCKH} | Input high delay for global clock | 1.53 | ns | See Table 227, page 78 |
| | T_{RCKL} | Input low delay for global clock | 0.897 | ns | See Table 227, page 78 |
| D | T_{PY} | Input propagation delay of LVDS receiver | 2.774 | ns | See Table 167, page 56 |
| E | T_{DP} | Propagation delay of a three-input AND gate | 0.198 | ns | See Table 223, page 76 |

2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

Figure 5 • Tristate Buffer for Enable Path Test Point



2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

Table 18 • Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions

| I/O | MSIO | MSIOD | DDRIO | Unit |
|--------------------------|------|-------|-------|------|
| PCI 3.3 V | 630 | | | Mbps |
| LVTTL 3.3 V | 600 | | | Mbps |
| LVC MOS 3.3 V | 600 | | | Mbps |
| LVC MOS 2.5 V | 410 | 420 | 400 | Mbps |
| LVC MOS 1.8 V | 295 | 400 | 400 | Mbps |
| LVC MOS 1.5 V | 160 | 220 | 235 | Mbps |
| LVC MOS 1.2 V | 120 | 160 | 200 | Mbps |
| LPDDR-LVC MOS 1.8 V mode | | | 400 | Mbps |

Table 19 • Maximum Data Rate Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions

| I/O | MSIO | MSIOD | DDRIO | Unit |
|------------|------|-------|-------|------|
| LPDDR | | | 400 | Mbps |
| HSTL1.5 V | | | 400 | Mbps |
| SSTL 2.5 V | 510 | 700 | 400 | Mbps |
| SSTL 1.8 V | | | 667 | Mbps |
| SSTL 1.5 V | | | 667 | Mbps |

Table 20 • Maximum Data Rate Summary Table for Differential I/O in Worst-Case Industrial Conditions

| I/O | MSIO | MSIOD | Unit |
|---------------------|------|-------|------|
| LVPECL (input only) | 900 | | Mbps |
| LVDS 3.3 V | 535 | | Mbps |
| LVDS 2.5 V | 535 | 700 | Mbps |
| RSDS | 520 | 700 | Mbps |
| BLVDS | 500 | | Mbps |
| MLVDS | 500 | | Mbps |
| Mini-LVDS | 520 | 700 | Mbps |

Table 21 • Maximum Frequency Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---------------------------|-------|-------|-------|------|
| PCI 3.3 V | 315 | | | MHz |
| LVTTTL 3.3 V | 300 | | | MHz |
| LVC MOS 3.3 V | 300 | | | MHz |
| LVC MOS 2.5 V | 205 | 210 | 200 | MHz |
| LVC MOS 1.8 V | 147.5 | 200 | 200 | MHz |
| LVC MOS 1.5 V | 80 | 110 | 118 | MHz |
| LVC MOS 1.2 V | 60 | 80 | 100 | MHz |
| LPDDR– LVC MOS 1.8 V mode | | | 200 | MHz |

Table 107 • SSTL2 AC Differential Voltage Specifications

| Parameter | Symbol | Min | Max | Unit |
|-------------------------------------|-----------------|----------------------------|----------------------------|------|
| AC input differential voltage | $V_{DIFF} (AC)$ | 0.7 | | V |
| AC differential cross point voltage | $V_x (AC)$ | $0.5 \times V_{DDI} - 0.2$ | $0.5 \times V_{DDI} + 0.2$ | V |

Table 108 • SSTL2 Minimum and Maximum AC Switching Speeds

| Parameter | Symbol | Max | Unit | Conditions |
|--|-----------|-----|------|--------------------------------------|
| Maximum data rate (for DDRIO I/O bank) | D_{MAX} | 400 | Mbps | AC loading: per JEDEC specifications |
| Maximum data rate (for MSIO I/O bank) | D_{MAX} | 575 | Mbps | AC loading: 17pF load |
| Maximum data rate (for MSIOD I/O bank) | D_{MAX} | 700 | Mbps | AC loading: 3 pF / 50 Ω load |
| | | 510 | Mbps | AC loading: 17pF load |

Table 109 • SSTL2 AC Impedance Specifications

| Parameter | Typ | Unit | Conditions |
|---|--------|----------|-----------------------------------|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | 20, 42 | Ω | Reference resistor = 150 Ω |

Table 110 • DDR1/SSTL2 AC Test Parameter Specifications

| Parameter | Symbol | Typ | Unit |
|--|----------------|------|----------|
| Measuring/trip point for data path | V_{TRIP} | 1.25 | V |
| Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ}) | R_{ENT} | 2K | Ω |
| Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ}) | C_{ENT} | 5 | pF |
| Reference resistance for data test path for SSTL2 Class I (T_{DP}) | R_{TT_TEST} | 50 | Ω |
| Reference resistance for data test path for SSTL2 Class II (T_{DP}) | R_{TT_TEST} | 25 | Ω |
| Capacitive loading for data path (T_{DP}) | C_{LOAD} | 5 | pF |

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 111 • SSTL2 Receiver Characteristics for DDRIO I/O Bank (Input Buffers)

| | On-Die Termination (ODT) | T_{PY} | | Unit |
|---------------------|--------------------------|----------|-------|------|
| | | -1 | -Std | |
| Pseudo differential | None | 1.549 | 1.821 | ns |
| True differential | None | 1.589 | 1.87 | ns |

Table 122 • SSTL18 DC Differential Voltage Specification

| Parameter | Symbol | Min | Unit |
|-------------------------------|---------------|-----|------|
| DC input differential voltage | V_{ID} (DC) | 0.3 | V |

Table 123 • SSTL18 AC Differential Voltage Specifications (Applicable to DDRIO Bank Only)

| Parameter | Symbol | Min | Max | Unit |
|-------------------------------------|-----------------|------------------------------|------------------------------|------|
| AC input differential voltage | V_{DIFF} (AC) | 0.5 | | V |
| AC differential cross point voltage | V_x (AC) | $0.5 \times V_{DDI} - 0.175$ | $0.5 \times V_{DDI} + 0.175$ | V |

Table 124 • SSTL18 Minimum and Maximum AC Switching Speed (Applicable to DDRIO Bank Only)

| Parameter | Symbol | Max | Unit | Conditions |
|--|-----------|-----|------|-------------------------------------|
| Maximum data rate (for DDRIO I/O bank) | D_{MAX} | 667 | Mbps | AC loading: per JEDEC specification |

Table 125 • SSTL18 AC Impedance Specifications (Applicable to DDRIO Bank Only)

| Parameter | Symbol | Typ | Unit | Conditions |
|---|-----------|-------------|----------|-----------------------------------|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | R_{REF} | 20, 42 | Ω | Reference resistor = 150 Ω |
| Effective impedance value (ODT) | R_{TT} | 50, 75, 150 | Ω | Reference resistor = 150 Ω |

Table 126 • SSTL18 AC Test Parameter Specifications (Applicable to DDRIO Bank Only)

| Parameter | Symbol | Typ | Unit |
|--|----------------|-----|----------|
| Measuring/trip point for data path | V_{TRIP} | 0.9 | V |
| Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ}) | R_{ENT} | 2K | Ω |
| Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ}) | C_{ENT} | 5 | pF |
| Reference resistance for data test path for SSTL18 Class I (T_{DP}) | R_{TT_TEST} | 50 | Ω |
| Reference resistance for data test path for SSTL18 Class II (T_{DP}) | R_{TT_TEST} | 25 | Ω |
| Capacitive loading for data path (T_{DP}) | C_{LOAD} | 5 | pF |

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

Table 127 • DDR2/SSTL18 Receiver Characteristics for DDRIO I/O Bank with Fixed Code

| | On-Die Termination (ODT) | T_{PY} | | Unit |
|---------------------|--------------------------|----------|-------|------|
| | | -1 | -Std | |
| Pseudo differential | None | 1.567 | 1.844 | ns |
| True differential | None | 1.588 | 1.869 | ns |

Table 191 • M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)

| On-Die Termination (ODT) | T_{PY} | | Unit |
|--------------------------|----------|-------|------|
| | -1 | -Std | |
| None | 2.495 | 2.934 | ns |
| 100 | 2.495 | 2.935 | ns |

Table 192 • M-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)

| T_{DP} | | T_{ZL} | | T_{ZH} | | T_{HZ} | | T_{LZ} | | Unit |
|----------|-------|----------|-------|----------|-------|----------|-------|----------|------|------|
| -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | |
| 2.258 | 2.656 | 2.348 | 2.762 | 2.334 | 2.746 | 2.123 | 2.497 | 2.125 | 2.5 | ns |

2.3.7.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

Mini-LVDS Minimum and Maximum Input and Output Levels

Table 193 • Mini-LVDS Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------|-----------|-------|-----|-------|------|
| Supply voltage | V_{DDI} | 2.375 | 2.5 | 2.625 | V |

Table 194 • Mini-LVDS DC Input Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|------------------|--------|-----|-------|------|
| DC Input voltage | V_I | 0 | 2.925 | V |

Table 195 • Mini-LVDS DC Output Voltage Specification

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------------|----------|------|-------|------|------|
| DC output logic high | V_{OH} | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | V_{OL} | 0.9 | 1.075 | 1.25 | V |

Table 196 • Mini-LVDS DC Differential Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|-----------------------------------|-----------|-----|-----|------|
| Differential output voltage swing | V_{OD} | 300 | 600 | mV |
| Output common mode voltage | V_{OCM} | 1 | 1.4 | V |
| Input common mode voltage | V_{ICM} | 0.3 | 1.2 | V |
| Input differential voltage | V_{ID} | 100 | 600 | mV |

Table 197 • Mini-LVDS Minimum and Maximum AC Switching Speed

| Parameter | Symbol | Max | Unit | Conditions |
|--|-----------|-----|------|---|
| Maximum data rate (for MSIO I/O bank) | D_{MAX} | 520 | Mbps | AC loading: 2 pF / 100 Ω differential load |
| Maximum data rate (for MSIOD I/O bank) | D_{MAX} | 700 | Mbps | AC loading: 2 pF / 100 Ω differential load |

Table 222 • Output DDR Propagation Delays (continued)

| Symbol | Description | Measuring Nodes (from, to) | -1 | -Std | Unit |
|------------------|--|----------------------------|-------|-------|------|
| $T_{DDROWAL}$ | Asynchronous load minimum pulse width for output DDR | C, C | 0.304 | 0.357 | ns |
| $T_{DDROCKMPWH}$ | Clock minimum pulse width high for the output DDR | E, E | 0.075 | 0.088 | ns |
| $T_{DDROCKMPWL}$ | Clock minimum pulse width low for the output DDR | E, E | 0.159 | 0.187 | ns |

2.3.10 Logic Element Specifications

2.3.10.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, see [SmartFusion2 and IGLOO2 Macro Library Guide](#).

Figure 14 • LUT-4

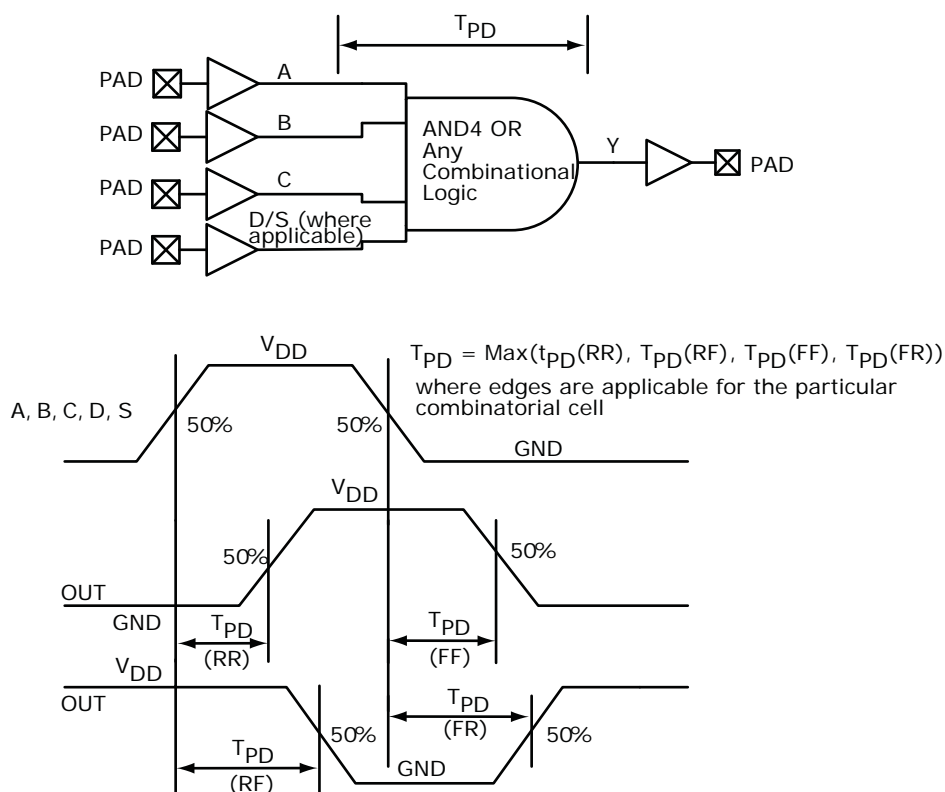


Table 232 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 (continued)

| Parameter | Symbol | –1 | | –Std | | Unit |
|--|----------------|--------|-------|--------|-------|------|
| | | Min | Max | Min | Max | |
| Address setup time | T_{ADDRSU} | 0.475 | | 0.559 | | ns |
| Address hold time | T_{ADDRHD} | 0.274 | | 0.322 | | ns |
| Data setup time | T_{DSU} | 0.336 | | 0.395 | | ns |
| Data hold time | T_{DHD} | 0.082 | | 0.096 | | ns |
| Block select setup time | T_{BLKSU} | 0.207 | | 0.244 | | ns |
| Block select hold time | T_{BLKHD} | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | T_{BLK2Q} | | 1.529 | | 1.799 | ns |
| Block select minimum pulse width | T_{BLKMPW} | 0.186 | | 0.219 | | ns |
| Read enable setup time | T_{RDESU} | 0.485 | | 0.57 | | ns |
| Read enable hold time | T_{RDEHD} | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | T_{R2Q} | | 1.514 | | 1.781 | ns |
| Asynchronous reset removal time | T_{RSTREM} | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | T_{RSTREC} | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | T_{RSTMPW} | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | T_{SRSTSU} | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | T_{SRSTHD} | 0.036 | | 0.043 | | ns |
| Write enable setup time | T_{WESU} | 0.415 | | 0.488 | | ns |
| Write enable hold time | T_{WEHD} | 0.048 | | 0.057 | | ns |
| Maximum frequency | F_{MAX} | | 400 | | 340 | MHz |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 233 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4

| Parameter | Symbol | –1 | | –Std | | Unit |
|--|-----------------|-------|-----|-------|-----|------|
| | | Min | Max | Min | Max | |
| Clock period | T_{CY} | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | T_{PLCY} | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |

Table 248 • 2 Step IAP Programming (eNVM Only)

| M2S/M2GL | | | | | |
|-----------------|-------------------------|---------------------|----------------|---------------|-------------|
| Device | Image size Bytes | Authenticate | Program | Verify | Unit |
| 005 | 137536 | 2 | 37 | 5 | Sec |
| 010 | 274816 | 4 | 76 | 11 | Sec |
| 025 | 274816 | 4 | 78 | 10 | Sec |
| 050 | 278528 | 3 | 85 | 9 | Sec |
| 060 | 268480 | 5 | 76 | 22 | Sec |
| 090 | 544496 | 10 | 152 | 43 | Sec |
| 150 | 544496 | 10 | 153 | 44 | Sec |

Table 249 • 2 Step IAP Programming (Fabric and eNVM)

| M2S/M2GL | | | | | |
|-----------------|-------------------------|---------------------|----------------|---------------|-------------|
| Device | Image size Bytes | Authenticate | Program | Verify | Unit |
| 005 | 439296 | 6 | 56 | 11 | Sec |
| 010 | 842688 | 11 | 100 | 21 | Sec |
| 025 | 1497408 | 19 | 113 | 32 | Sec |
| 050 | 2695168 | 32 | 136 | 48 | Sec |
| 060 | 2686464 | 43 | 137 | 70 | Sec |
| 090 | 4190208 | 68 | 236 | 115 | Sec |
| 150 | 6682768 | 109 | 286 | 162 | Sec |

Table 250 • SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)

| M2S/M2GL | | | | | |
|-----------------|-------------------------|---------------------|----------------|---------------|-------------|
| Device | Image size Bytes | Authenticate | Program | Verify | Unit |
| 005 | 302672 | 6 | 19 | 8 | Sec |
| 010 | 568784 | 10 | 26 | 14 | Sec |
| 025 | 1223504 | 21 | 39 | 29 | Sec |
| 050 | 2424832 | 39 | 60 | 50 | Sec |
| 060 | 2418896 | 44 | 65 | 54 | Sec |
| 090 | 3645968 | 66 | 90 | 79 | Sec |
| 150 | 6139184 | 108 | 140 | 128 | Sec |

Table 251 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)

| M2S/M2GL | | | | | |
|-----------------|-------------------------|---------------------|----------------|---------------|-------------|
| Device | Image size Bytes | Authenticate | Program | Verify | Unit |
| 005 | 137536 | 3 | 42 | 4 | Sec |
| 010 | 274816 | 4 | 82 | 7 | Sec |
| 025 | 274816 | 4 | 82 | 8 | Sec |
| 050 | 278528 | 4 | 80 | 8 | Sec |
| 060 | 268480 | 6 | 80 | 8 | Sec |
| 090 | 544496 | 10 | 157 | 15 | Sec |

The following table lists the programming times in worst-case conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 256 • JTAG Programming (Fabric Only)

| M2S/M2GL Device | Image size | | Verify | Unit |
|-----------------|------------|---------|--------|------|
| | Bytes | Program | | |
| 005 | 302672 | 44 | 10 | Sec |
| 010 | 568784 | 50 | 18 | Sec |
| 025 | 1223504 | 73 | 26 | Sec |
| 050 | 2424832 | 88 | 54 | Sec |
| 060 | 2418896 | 99 | 54 | Sec |
| 090 | 3645968 | 135 | 126 | Sec |
| 150 | 6139184 | 177 | 193 | Sec |

Table 257 • JTAG Programming (eNVM Only)

| M2S/M2GL Device | Image size | | Verify | Unit |
|-----------------|------------|---------|--------|------|
| | Bytes | Program | | |
| 005 | 137536 | 61 | 4 | Sec |
| 010 | 274816 | 100 | 9 | Sec |
| 025 | 274816 | 100 | 9 | Sec |
| 050 | 2,78,528 | 106 | 8 | Sec |
| 060 | 268480 | 98 | 8 | Sec |
| 090 | 544496 | 176 | 15 | Sec |
| 150 | 544496 | 177 | 15 | Sec |

Table 258 • JTAG Programming (Fabric and eNVM)

| M2S/M2GL Device | Image size | | Verify | Unit |
|-----------------|------------|---------|--------|------|
| | Bytes | Program | | |
| 005 | 439296 | 71 | 11 | Sec |
| 010 | 842688 | 129 | 20 | Sec |
| 025 | 1497408 | 142 | 35 | Sec |
| 050 | 2695168 | 184 | 59 | Sec |
| 060 | 2686464 | 180 | 70 | Sec |
| 090 | 4190208 | 288 | 147 | Sec |
| 150 | 6682768 | 338 | 231 | Sec |

2.3.14 Math Block Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC math block supports 18×18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently. The following table lists the math blocks with all registers used in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 268 • Math Blocks with all Registers Used

| Parameter | Symbol | -1 | | -Std | | Unit |
|-------------------------------------|-----------------|--------|-------|--------|-------|------|
| | | Min | Max | Min | Max | |
| Input, control register setup time | T_{MISU} | 0.149 | | 0.176 | | ns |
| Input, control register hold time | T_{MIHD} | 1.68 | | 1.976 | | ns |
| CDIN input setup time | $T_{MOCDINSU}$ | 0.185 | | 0.218 | | ns |
| CDIN input hold time | $T_{MOCDINHHD}$ | 0.08 | | 0.094 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | -0.419 | | -0.493 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | 0.011 | | 0.013 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | 0 | | 0 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.088 | | 0.104 | | ns |
| Output register clock to out delay | T_{MOCQ} | | 0.232 | | 0.273 | ns |
| CLK minimum period | T_{MCLKMP} | 2.245 | | 2.641 | | ns |

The following table lists the math blocks with input bypassed and output registers used in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 269 • Math Block with Input Bypassed and Output Registers Used

| Parameter | Symbol | -1 | | -Std | | Unit |
|-------------------------------------|-----------------|--------|-------|--------|-------|------|
| | | Min | Max | Min | Max | |
| Output register setup time | T_{MOSU} | 2.294 | | 2.699 | | ns |
| Output register hold time | T_{MOHD} | 1.68 | | 1.976 | | ns |
| CDIN input setup time | $T_{MOCDINSU}$ | 0.115 | | 0.136 | | ns |
| CDIN input hold time | $T_{MOCDINHHD}$ | -0.444 | | -0.522 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | -0.419 | | -0.493 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | 0.011 | | 0.013 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | 0 | | 0 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.014 | | 0.017 | | ns |
| Output register clock to out delay | T_{MOCQ} | | 0.232 | | 0.273 | ns |
| CLK minimum period | T_{MCLKMP} | 2.179 | | 2.563 | | ns |

Table 276 • Cryptographic Block Characteristics (continued)

| Service | Conditions | Timing | Unit |
|--------------------------|------------|--------|------|
| SHA256 | 512 bits | 540 | kbps |
| | 1024 bits | 780 | kbps |
| | 2048 bits | 950 | kbps |
| | 24 kbits | 1140 | kbps |
| HMAC | 512 bytes | 820 | kbps |
| | 1024 bytes | 890 | kbps |
| | 2048 bytes | 930 | kbps |
| | 24 kbytes | 980 | kbps |
| KeyTree | | 1.8 | ms |
| Challenge-response | PUF = OFF | 25 | ms |
| | PUF = ON | 7 | ms |
| ECC point multiplication | | 590 | ms |
| ECC point addition | | 8 | ms |

1. Using cypher block chaining (CBC) mode.

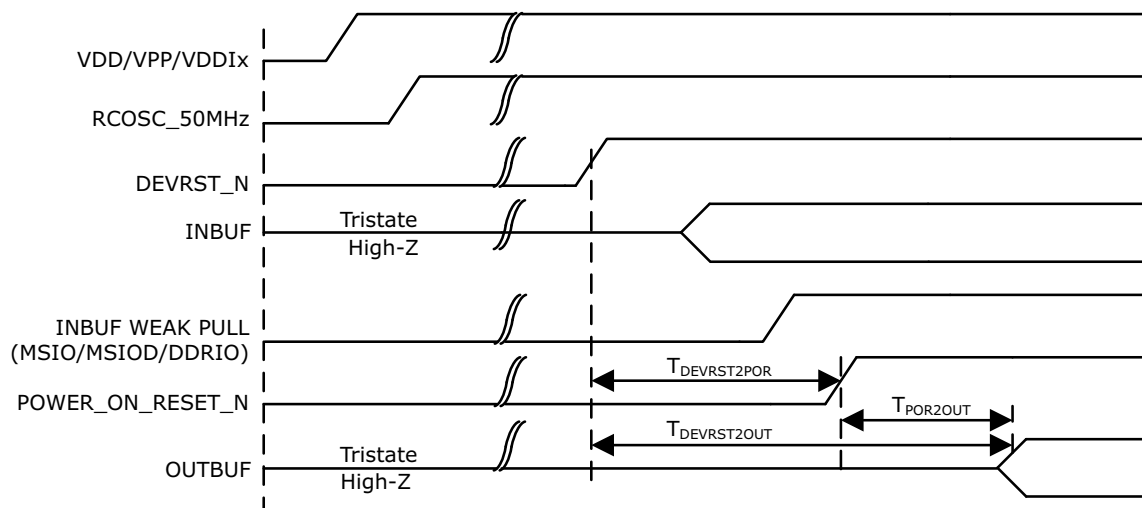
2.3.19 Crystal Oscillator

The following table describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

Table 277 • Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|------------|---------------------|-------|---------------------|------|--|
| Operating frequency | FXTAL | | 20 | | MHz | |
| Accuracy | ACCXTAL | | | 0.0047 | % | 005, 010, 025, 050, 060, and 090 devices |
| | | | | 0.0058 | % | 150 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 200 | 300 | ps | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 200 | 300 | ps | 010, 025, 050, and 060 devices |
| | | | 250 | 410 | ps | 150 devices |
| | | | 250 | 550 | ps | 005 and 090 devices |
| Operating current | IDYNXTAL | | 1.5 | | mA | 010, 050, and 060 devices |
| | | | 1.65 | | mA | 005, 025, 090, and 150 devices |
| Input logic level high | VIHXTAL | 0.9 V _{PP} | | | V | |
| Input logic level low | VILXTAL | | | 0.1 V _{PP} | V | |

Figure 20 • DEVRST_N to Functional Timing Diagram for IGLOO2



2.3.27 Flash*Freeze Timing Characteristics

The following table lists the Flash*Freeze entry and exit times in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 293 • Flash*Freeze Entry and Exit Times

| Parameter | Symbol | Entry/Exit Timing | | | Unit | Conditions |
|--|-----------|----------------------------------|-----|--------------|---------------|---|
| | | FCLK = 100MHz | | FCLK = 3 MHz | | |
| | | 005, 010, 025, 060, 090, and 150 | 050 | All Devices | | |
| Entry time | TFF_ENTRY | 160 | 150 | 320 | μs | eNVM and MSS/HPMS PLL = ON |
| | | 215 | 200 | 430 | μs | eNVM and MSS/HPMS PLL= OFF |
| Exit time with respect to the MSS PLL Lock | TFF_EXIT | 100 | 100 | 140 | μs | eNVM and MSS/HPMS PLL = ON during F*F |
| | | 136 | 120 | 190 | μs | eNVM = ON and MSS/HPMS PLL = OFF during F*F and MSS/HPMS PLL turned back on at exit |
| | | 200 | 200 | 285 | μs | eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit |
| | | 200 | 200 | 285 | μs | eNVM = OFF and MSS/HPMS PLL = ON during F*F and eNVM turned back on at exit |

2.3.30 SerDes Electrical and Timing AC and DC Characteristics

PCIe is a high-speed, packet-based, point-to-point, low-pin-count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block.

The following table lists the transmitter parameters in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 296 • Transmitter Parameters

| Symbol | Description | Min | Max | Unit |
|---------------|--|-------|---------------|---------------|
| VTX-DIFF-PP | Differential swing (2.5 Gbps, 5.0 Gbps) | 0.8 | 1.2 | V |
| VTX-CM-AC-P | Output common mode voltage (2.5 Gbps) | | 20 | mV |
| VTX-CM-AC-PP | Output common mode voltage (5.0 Gbps) | | 100 | mV |
| VTX-RISE-FALL | Rise and fall time (20% to 80%, 2.5 Gbps) | 0.125 | | UI |
| | Rise and fall time (20% to 80%, 5.0 Gbps) | 0.15 | | UI |
| ZTX-DIFF-DC | Output impedance–differential | 80 | 120 | Ω |
| LTX-SKEW | Lane-to-lane TX skew within a SerDes block (2.5 Gbps) | | 500 ps + 2 UI | ps |
| | Lane-to-lane TX skew within a SerDes block (5.0 Gbps) | | 500 ps + 4 UI | ps |
| RLTX-DIFF | Return loss differential mode (2.5 Gbps) | –10 | | dB |
| | Return loss differential mode (5.0 Gbps) 0.05 GHz to 1.25 GHz | –10 | | dB |
| | 1.25 GHz to 2.5 GHz | –8 | | dB |
| RLTX-CM | Return loss common mode (2.5 Gbps, 5.0 Gbps) | –6 | | dB |
| TX-LOCK-RST | Transmit PLL lock time from reset | | 10 | μs |
| VTX-AMP | 100 mV setting | 90 | 150 | mV |
| | 400 mV setting | 320 | 480 | mV |
| | 800 mV setting | 660 | 940 | mV |
| | 1200 mV setting | 950 | 1400 | mV |

The following table lists the receiver pa in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 297 • Receiver Parameters

| Symbol | Description | Min | Typ | Max | Unit |
|----------------------|---|-------|-------|-------|---------------|
| VRX-IN-PP-CC | Differential input peak-to-peak sensitivity (2.5 Gbps) | 0.238 | | 1.2 | V |
| | Differential input peak-to-peak sensitivity (2.5 Gbps, de-emphasized) | 0.219 | | 1.2 | V |
| | Differential input peak-to-peak sensitivity (5.0 Gbps) | 0.300 | | 1.2 | V |
| | Differential input peak-to-peak sensitivity (5.0 Gbps, de-emphasized) | 0.300 | | 1.2 | V |
| VRX-CM-AC-P | Input common mode range (AC coupled) | | | 150 | mV |
| ZRX-DIFF-DC | Differential input termination | 80 | 100 | 120 | Ω |
| REXT | External calibration resistor | 1,188 | 1,200 | 1,212 | Ω |
| CDR-LOCK-RST | CDR relock time from reset | | | 15 | μs |
| RLRX-DIFF | Return loss differential mode (2.5 Gbps) | -10 | | | dB |
| | Return loss differential mode (5.0 Gbps) | | | | |
| | 0.05 GHz to 1.25 GHz | -10 | | | dB |
| | 1.25 GHz to 2.5 GHz | -8 | | | dB |
| RLRX-CM | Return loss common mode (2.5 Gbps, 5.0 Gbps) | -6 | | | dB |
| RX-CID ¹ | CID limit PCIe Gen1/2 | | | 200 | UI |
| VRX-IDLE-DET-DIFF-PP | Signal detect limit | 65 | | 175 | mV |

1. AC-coupled, BER = e^{-12} , using synchronous clock.

Table 298 • SerDes Protocol Compliance

| Protocol | Maximum Data Rate (Gbps) | -1 | -Std |
|--------------|--------------------------|-----|------|
| PCIe Gen 1 | 2.5 | Yes | Yes |
| PCIe Gen 2 | 5.0 | Yes | |
| XAUI | 3.125 | Yes | |
| Generic EPCS | 3.2 | Yes | |
| Generic EPCS | 2.5 | Yes | Yes |

2.3.31.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, see [Figure 22](#), page 128.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Table 305 • SPI Characteristics for All Devices

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---------|--|-------|------|-----|---------------|---|
| SPIFMAX | Maximum operating frequency of SPI interface | | | 20 | MHz | |
| sp1 | SPI_[0 1]_CLK minimum period | | | | | |
| | SPI_[0 1]_CLK = PCLK/2 | 12 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/4 | 24.1 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/8 | 48.2 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/16 | 0.1 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/32 | 0.19 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/64 | 0.39 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/128 | 0.77 | | | μs | |
| sp2 | SPI_[0 1]_CLK minimum pulse width high | | | | | |
| | SPI_[0 1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/16 | 0.05 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/32 | 0.095 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/64 | 0.195 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/128 | 0.385 | | | μs | |
| sp3 | SPI_[0 1]_CLK minimum pulse width low | | | | | |
| | SPI_[0 1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/16 | 0.05 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/32 | 0.095 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/64 | 0.195 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/128 | 0.385 | | | μs | |
| sp4 | SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) ¹ | | 2.77 | | ns | I/O Configuration: LVCMOS 2.5 V– 8 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C |