

Welcome to [E-XFL.COM](https://www.e-xfl.com)

### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	64KB
Peripherals	-
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 5K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s005-tqg144">https://www.e-xfl.com/product-detail/microchip-technology/m2s005-tqg144</a>

**Table 19 • Maximum Data Rate Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
LPDDR			400	Mbps
HSTL1.5 V			400	Mbps
SSTL 2.5 V	510	700	400	Mbps
SSTL 1.8 V			667	Mbps
SSTL 1.5 V			667	Mbps

**Table 20 • Maximum Data Rate Summary Table for Differential I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	Unit
LVPECL (input only)	900		Mbps
LVDS 3.3 V	535		Mbps
LVDS 2.5 V	535	700	Mbps
RSDS	520	700	Mbps
BLVDS	500		Mbps
MLVDS	500		Mbps
Mini-LVDS	520	700	Mbps

**Table 21 • Maximum Frequency Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	315			MHz
LVTTTL 3.3 V	300			MHz
LVC MOS 3.3 V	300			MHz
LVC MOS 2.5 V	205	210	200	MHz
LVC MOS 1.8 V	147.5	200	200	MHz
LVC MOS 1.5 V	80	110	118	MHz
LVC MOS 1.2 V	60	80	100	MHz
LPDDR– LVC MOS 1.8 V mode			200	MHz

**Table 22 • Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
LPDDR			200	MHz
HSTL1.5 V			200	MHz
SSTL 2.5 V	255	350	200	MHz
SSTL 1.8 V			334	MHz
SSTL 1.5 V			334	MHz

**Table 23 • Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	Unit
LVPECL (input only)	450		MHz
LVDS 3.3 V	267.5		MHz
LVDS 2.5 V	267.5	350	MHz
RSDS	260	350	MHz
BLVDS	250		MHz
MLVDS	250		MHz
Mini-LVDS	260	350	MHz

**Table 48 • LVCMOS 2.5 V Transmitter Characteristics for MSIOD Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	2.206	2.596	2.678	3.15	2.64	3.106	4.935	5.805	4.74	5.576	ns
4 mA	Slow	1.835	2.159	2.242	2.637	2.256	2.654	5.413	6.368	5.15	6.059	ns
6 mA	Slow	1.709	2.01	2.132	2.508	2.167	2.549	5.813	6.838	5.499	6.469	ns
8 mA	Slow	1.63	1.918	1.958	2.303	2.012	2.367	6.226	7.324	5.816	6.842	ns
12 mA	Slow	1.648	1.939	1.86	2.187	1.921	2.259	6.519	7.669	6.027	7.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.8 1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 49 • LVCMOS 1.8 V DC Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
<b>LVCMOS 1.8 V DC Recommended Operating Conditions</b>					
Supply voltage	$V_{DDI}$	1.710	1.8	1.89	V

**Table 50 • LVCMOS 1.8 V DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	$V_{IH}$ (DC)	$0.65 \times V_{DDI}$	1.89	V
DC input logic high (for MSIO I/O bank)	$V_{IH}$ (DC)	$0.65 \times V_{DDI}$	3.45	V
DC input logic low	$V_{IL}$ (DC)	-0.3	$0.35 \times V_{DDI}$	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			-
Input current low <sup>1</sup>	$I_{IL}$ (DC)			-

1. See Table 24, page 22.

**Table 51 • LVCMOS 1.8 V DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	$V_{OH}$	$V_{DDI} - 0.45$		V
DC output logic low	$V_{OL}$		0.45	V

**Table 52 • LVCMOS 1.8 V Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank) <sup>1</sup>	$D_{MAX}$	400	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	295	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank) <sup>1</sup>	$D_{MAX}$	400	Mbps	AC loading: 17 pF load, maximum drive/slew

1. Maximum Data Rate applies for Drive Strength 8 mA and above, All Slews.

**Table 53 • LVCMOS 1.8 V AC Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	Rodt_cal	75, 60, 50, 33, 25, 20	Ω

**Table 54 • LVCMOS 1.8 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V <sub>TRIP</sub>	0.9	V
Resistance for enable path (T <sub>ZH</sub> , T <sub>ZL</sub> , T <sub>HZ</sub> , T <sub>LZ</sub> )	R <sub>ENT</sub>	2k	Ω
Capacitive loading for enable path (T <sub>ZH</sub> , T <sub>ZL</sub> , T <sub>HZ</sub> , T <sub>LZ</sub> )	C <sub>ENT</sub>	5	pF
Capacitive loading for data path (T <sub>DP</sub> )	C <sub>LOAD</sub>	5	pF

**Table 55 • LVCMOS 1.8 V Transmitter Drive Strength Specifications**

Output Drive Selection			V <sub>OH</sub> (V)	V <sub>OL</sub> (V)	IOH (at V <sub>OH</sub> )	IOL (at V <sub>OL</sub> )
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max	mA	mA
2 mA	2 mA	2 mA	V <sub>DDI</sub> - 0.45	0.45	2	2
4 mA	4 mA	4 mA	V <sub>DDI</sub> - 0.45	0.45	4	4
6 mA	6 mA	6 mA	V <sub>DDI</sub> - 0.45	0.45	6	6
8 mA	8 mA	8 mA	V <sub>DDI</sub> - 0.45	0.45	8	8
10 mA	10 mA	10 mA	V <sub>DDI</sub> - 0.45	0.45	10	10
12 mA		12 mA	V <sub>DDI</sub> - 0.45	0.45	12	12
		16 mA <sup>1</sup>	V <sub>DDI</sub> - 0.45	0.45	16	16

1. 16 mA drive strengths, all slews, meets LPDDR JEDEC electrical compliance.

**AC Switching Characteristics**

Worst commercial-case conditions: T<sub>J</sub> = 85 °C, V<sub>DD</sub> = 1.14 V, V<sub>DDI</sub> = 1.71 V

**Table 56 • LVCMOS 1.8 V Receiver Characteristics (Input Buffers)**

	On-Die Termination (ODT)	T <sub>Py</sub>		T <sub>Pys</sub>		Unit
		-1	-Std	-1	-Std	
<b>LVCMOS 1.8 V (for DDRIO I/O bank with Fixed Codes)</b>	None	1.968	2.315	2.099	2.47	ns
	None	2.898	3.411	2.883	3.393	ns
	50	3.05	3.59	3.044	3.583	ns
	75	2.999	3.53	2.987	3.516	ns
<b>LVCMOS 1.8 V (for MSIO I/O bank)</b>	150	2.947	3.469	2.933	3.452	ns
	None	2.611	3.071	2.598	3.057	ns
	50	2.775	3.264	2.775	3.265	ns
	75	2.72	3.2	2.712	3.19	ns
<b>LVCMOS 1.8 V (for MSIOD I/O bank)</b>	150	2.666	3.137	2.655	3.123	ns

**Table 57 • LVCMOS 1.8 V Transmitter Characteristics for DDRIO I/O Bank with Fixed Code (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub> <sup>1</sup>		T <sub>LZ</sub> <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	Medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	Medium fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	Fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4 mA	Slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	Medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	Medium fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	Fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6 mA	Slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	Medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	Medium fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	Fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns
8 mA	Slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns
	Medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	Medium fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	Fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10 mA	Slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	Medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	Medium fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	Fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12 mA	Slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	Medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	Medium fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	Fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16 mA	Slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	Medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	Medium fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	Fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 122 • SSTL18 DC Differential Voltage Specification**

Parameter	Symbol	Min	Unit
DC input differential voltage	$V_{ID}$ (DC)	0.3	V

**Table 123 • SSTL18 AC Differential Voltage Specifications (Applicable to DDRIO Bank Only)**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	$V_{DIFF}$ (AC)	0.5		V
AC differential cross point voltage	$V_x$ (AC)	$0.5 \times V_{DDI} - 0.175$	$0.5 \times V_{DDI} + 0.175$	V

**Table 124 • SSTL18 Minimum and Maximum AC Switching Speed (Applicable to DDRIO Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	$D_{MAX}$	667	Mbps	AC loading: per JEDEC specification

**Table 125 • SSTL18 AC Impedance Specifications (Applicable to DDRIO Bank Only)**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	$R_{REF}$	20, 42	$\Omega$	Reference resistor = 150 $\Omega$
Effective impedance value (ODT)	$R_{TT}$	50, 75, 150	$\Omega$	Reference resistor = 150 $\Omega$

**Table 126 • SSTL18 AC Test Parameter Specifications (Applicable to DDRIO Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	0.9	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Reference resistance for data test path for SSTL18 Class I ( $T_{DP}$ )	$R_{TT\_TEST}$	50	$\Omega$
Reference resistance for data test path for SSTL18 Class II ( $T_{DP}$ )	$R_{TT\_TEST}$	25	$\Omega$
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

#### AC Switching Characteristics

Worst commercial-case conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 1.71\text{ V}$

**Table 127 • DDR2/SSTL18 Receiver Characteristics for DDRIO I/O Bank with Fixed Code**

	On-Die Termination (ODT)	$T_{PY}$		Unit
		-1	-Std	
Pseudo differential	None	1.567	1.844	ns
True differential	None	1.588	1.869	ns

**Table 144 • LPDDR AC Differential Voltage Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	$V_{DIFF}$	$0.6 \times V_{DDI}$		V
AC differential cross point voltage	$V_x$	$0.4 \times V_{DDI}$	$0.6 \times V_{DDI}$	V

**Table 145 • LPDDR AC Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	$D_{MAX}$	400	Mbps	AC loading: per JEDEC specifications

**Table 146 • LPDDR AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	$R_{REF}$	20, 42	$\Omega$	Reference resistor = 150 $\Omega$
Effective impedance value (ODT)	$R_{TT}$	50, 70, 150	$\Omega$	Reference resistor = 150 $\Omega$

**Table 147 • LPDDR AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	0.9	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Reference resistance for data test path for LPDDR ( $T_{DP}$ )	$R_{TT\_TEST}$	50	$\Omega$
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	$\Omega$

#### AC Switching Characteristics

Worst-case commercial conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ , worst-case  $V_{DDI}$ .

**Table 148 • LPDDR Receiver Characteristics for DDRIO I/O Bank with Fixed Codes**

		$T_{PY}$		Unit
		On-Die Termination (ODT) -1	-Std	
Pseudo differential	None	1.568	1.845	ns
True differential	None	1.588	1.869	ns

**Table 149 • LPDDR Reduced Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ENZL}$		$T_{ENZH}$		$T_{ENHZ}$		$T_{ENLZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.383	2.804	2.23	2.623	2.229	2.622	2.202	2.591	2.201	2.59	ns
Differential	2.396	2.819	2.764	3.252	2.764	3.252	2.255	2.653	2.255	2.653	ns



**Table 150 • LPDDR Full Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ENZL}$		$T_{ENZH}$		$T_{ENHZ}$		$T_{ENLZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.171	2.555	2.17	2.554	ns
Differential	2.298	2.703	2.288	2.692	2.288	2.692	2.593	3.051	2.593	3.051	ns

**Minimum and Maximum DC/AC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode**

**Table 151 • LPDDR-LVCMOS 1.8 V Mode Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	1.710	1.8	1.89	V

**Table 152 • LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	$V_{IH}$ (DC)	$0.65 \times V_{DDI}$	1.89	V
DC input logic high (for MSIO I/O bank)	$V_{IH}$ (DC)	$0.65 \times V_{DDI}$	3.45	V
DC input logic low	$V_{IL}$ (DC)	-0.3	$0.35 \times V_{DDI}$	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 153 • LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	$V_{OH}$	$V_{DDI} - 0.45$		V
DC output logic low	$V_{OL}$		0.45	V

**Table 154 • LPDDR-LVCMOS 1.8 V Minimum and Maximum AC Switching Speeds**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	$D_{MAX}$	400	Mbps	AC loading: 17pf load, 8 ma drive and above/all slew

**Table 155 • LPDDR-LVCMOS 1.8 V Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CAL	75, 60, 50, 33, 25, 20	$\Omega$

**Table 156 • LPDDR-LVCMOS 1.8 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	0.9	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**Table 157 • LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification for DDRIO Bank**

Output Drive Selection	$V_{OH}$ (V) Min	$V_{OL}$ (V) Max	$I_{OH}$ (at $V_{OH}$ ) mA	$I_{OL}$ (at $V_{OL}$ ) mA
2 mA	$V_{DDI} - 0.45$	0.45	2	2
4 mA	$V_{DDI} - 0.45$	0.45	4	4
6 mA	$V_{DDI} - 0.45$	0.45	6	6
8 mA	$V_{DDI} - 0.45$	0.45	8	8
10 mA	$V_{DDI} - 0.45$	0.45	10	10
12 mA	$V_{DDI} - 0.45$	0.45	12	12
16 mA <sup>1</sup>	$V_{DDI} - 0.45$	0.45	16	16

1. 16 mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance.

**Table 158 • LPDDR-LVCMOS 1.8V AC Switching Characteristics for Receiver (for DDRIO I/O Bank with Fixed Code - Input Buffers)**

ODT (On Die Termination)	-1	-Std	-1	-Std	Unit
None	1.968	2.315	2.099	2.47	ns

**Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$ <sup>1</sup>		$T_{LZ}$ <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	medium_fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4 mA	slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	medium_fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6 mA	slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	medium_fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns
8 mA	slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns

**Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers) (continued)**

	medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	medium_fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10 mA	slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	medium_fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12 mA	slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	medium_fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16 mA	slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	medium_fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO management).

### 2.3.7 Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

#### 2.3.7.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

##### Minimum and Maximum Input and Output Levels

**Table 160 • LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V	2.5 V range
Supply voltage	$V_{DDI}$	3.15	3.3	3.45	V	3.3 V range

**Table 161 • LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit	Conditions
DC Input voltage	$V_I$	0	2.925	V	2.5 V range
DC input voltage	$V_I$	0	3.45	V	3.3 V range
Input current high <sup>1</sup>	$I_{IH}$ (DC)				
Input current low <sup>1</sup>	$I_{IL}$ (DC)				

1. See Table 24, page 22.

**Table 162 • LVDS DC Output Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	$V_{OH}$	1.25	1.425	1.6	V
DC output logic low	$V_{OL}$	0.9	1.075	1.25	V

**Table 163 • LVDS DC Differential Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
Differential output voltage swing	$V_{OD}$	250	350	450	mV
Output common mode voltage	$V_{OCM}$	1.125	1.25	1.375	V
Input common mode voltage	$V_{ICM}$	0.05	1.25	2.35	V
Input differential voltage	$V_{ID}$	100	350	600	mV

**Table 164 • LVDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	535	Mbps	AC loading: 12 pF / 100 $\Omega$ differential load
Maximum data rate (for MSIOD I/O bank) no pre-emphasis	$D_{MAX}$	620	Mbps	AC loading: 10 pF / 100 $\Omega$ differential load
		700	Mbps	AC loading: 2 pF / 100 $\Omega$ differential load

**Table 165 • LVDS AC Impedance Specifications**

Parameter	Symbol	Typ	Max	Unit
Termination resistance	$R_T$	100		$\Omega$

**Table 166 • LVDS AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	Cross point	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF

**LVDS25 AC Switching Characteristics**

 Worst commercial-case conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$ 
**Table 167 • LVDS25 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.774	3.263	ns
100	2.775	3.264	ns

**Table 191 • M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

On-Die Termination (ODT)	T <sub>PY</sub>		Unit
	-1	-Std	
None	2.495	2.934	ns
100	2.495	2.935	ns

**Table 192 • M-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub>		T <sub>LZ</sub>		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.258	2.656	2.348	2.762	2.334	2.746	2.123	2.497	2.125	2.5	ns

### 2.3.7.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

#### Mini-LVDS Minimum and Maximum Input and Output Levels

**Table 193 • Mini-LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>DDI</sub>	2.375	2.5	2.625	V

**Table 194 • Mini-LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC Input voltage	V <sub>I</sub>	0	2.925	V

**Table 195 • Mini-LVDS DC Output Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V <sub>OH</sub>	1.25	1.425	1.6	V
DC output logic low	V <sub>OL</sub>	0.9	1.075	1.25	V

**Table 196 • Mini-LVDS DC Differential Voltage Specification**

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing	V <sub>OD</sub>	300	600	mV
Output common mode voltage	V <sub>OCM</sub>	1	1.4	V
Input common mode voltage	V <sub>ICM</sub>	0.3	1.2	V
Input differential voltage	V <sub>ID</sub>	100	600	mV

**Table 197 • Mini-LVDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D <sub>MAX</sub>	520	Mbps	AC loading: 2 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank)	D <sub>MAX</sub>	700	Mbps	AC loading: 2 pF / 100 Ω differential load

### AC Switching Characteristics

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$ .

**Table 210 • RSDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.855	3.359	ns
100	2.85	3.353	ns

**Table 211 • RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.602	3.061	ns
100	2.597	3.055	ns

**Table 212 • RSDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.097	2.467	2.303	2.709	2.291	2.695	1.961	2.307	1.947	2.29	ns

**Table 213 • RSDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
No pre-emphasis	1.614	1.899	1.559	1.834	1.55	1.823	1.59	1.87	1.575	1.852	ns
Min pre-emphasis	1.604	1.887	1.742	2.05	1.728	2.032	1.889	2.222	1.858	2.185	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

#### 2.3.7.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

#### Minimum and Maximum Input and Output Levels (Applicable to MSIO I/O Bank Only)

**Table 214 • LVPECL Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	3.15	3.3	3.45	V

**Table 215 • LVPECL DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	$V_I$	0	3.45	V

**Table 216 • LVPECL DC Differential Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
Input common mode voltage	$V_{ICM}$	0.3		2.8	V
Input differential voltage	$V_{IDIFF}$	100	300	1,000	mV

**Table 217 • LVPECL Minimum and Maximum AC Switching Speeds**

Parameter	Symbol	Max	Unit
Maximum data rate	$D_{MAX}$	900	Mbps

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$ .

**Table 218 • LVPECL Receiver Characteristics for MSIO I/O Bank**

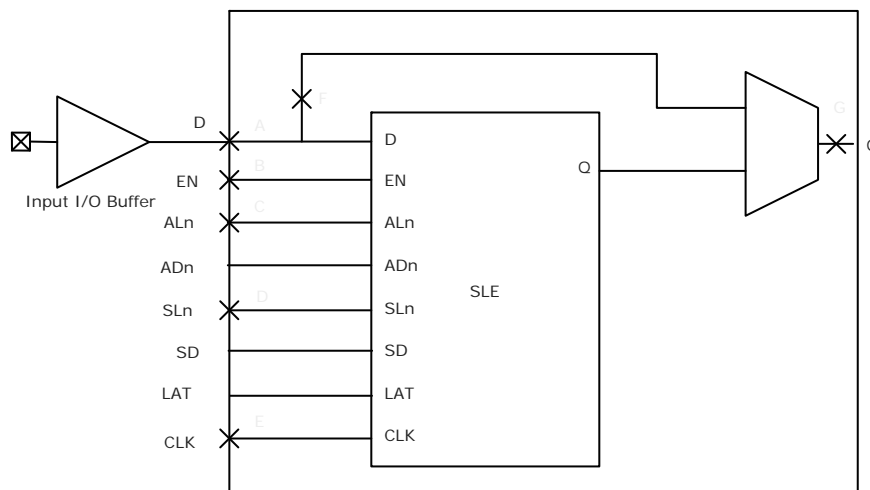
On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.572	3.025	ns
100	2.569	3.023	ns

**2.3.8 I/O Register Specifications**

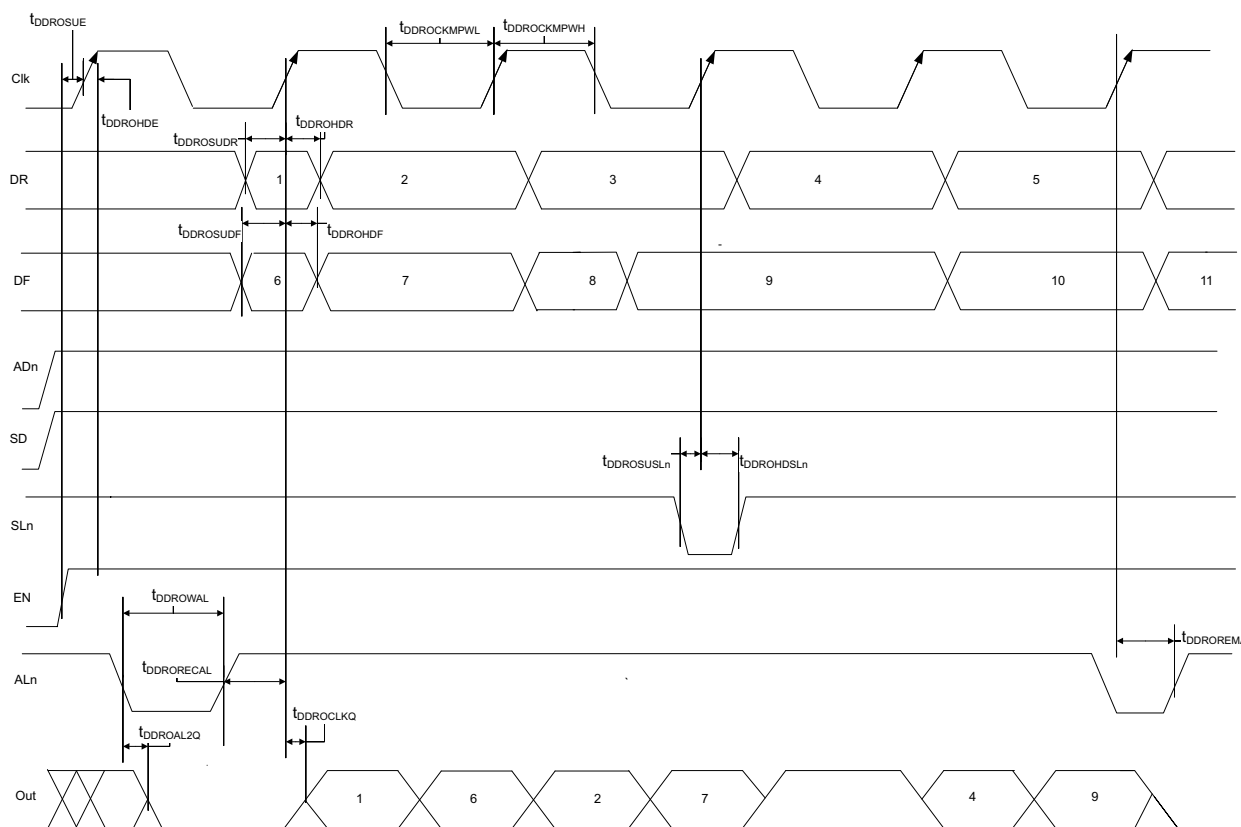
This section describes input and output register specifications.

**2.3.8.1 Input Register**

**Figure 6 • Timing Model for Input Register**



**Figure 13 • Output DDR Timing Diagram**



**2.3.9.5 Timing Characteristics**

The following table lists the output DDR propagation delays in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 222 • Output DDR Propagation Delays**

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDROCLKQ}$	Clock-to-out of DDR for output DDR	E, G	0.263	0.309	ns
$T_{DDROSUDF}$	Data_F data setup for output DDR	F, E	0.143	0.168	ns
$T_{DDROSUDR}$	Data_R data setup for output DDR	A, E	0.19	0.223	ns
$T_{DDROHDF}$	Data_F data hold for output DDR	F, E	0	0	ns
$T_{DDROHDR}$	Data_R data hold for output DDR	A, E	0	0	ns
$T_{DDROSUE}$	Enable setup for input DDR	B, E	0.419	0.493	ns
$T_{DDROHE}$	Enable hold for input DDR	B, E	0	0	ns
$T_{DDROSUSLN}$	Synchronous load setup for input DDR	D, E	0.196	0.231	ns
$T_{DDROHSLN}$	Synchronous load hold for input DDR	D, E	0	0	ns
$T_{DDROAL2Q}$	Asynchronous load-to-out for output DDR	C, G	0.528	0.621	ns
$T_{DDRORECAL}$	Asynchronous load recovery time for output DDR	C, E	0	0	ns
$T_{DDROREEM}$	Asynchronous load removal time for output DDR	C, E	0	0	ns
$T_{DDRORECAL}$	Asynchronous load recovery time for output DDR	C, E	0.034	0.04	ns



## 2.3.11 Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for the positions of various global routing resources.

The following table lists the 150 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 225 • 150 Device Global Resource**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	$T_{RCKL}$	0.83	0.911	0.831	0.913	ns
Input high delay for global clock	$T_{RCKH}$	1.457	1.588	1.715	1.869	ns
Maximum skew for global clock	$T_{RCKSW}$		0.131		0.154	ns

The following table lists the 090 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 226 • 090 Device Global Resource**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	$T_{RCKL}$	0.835	0.888	0.833	0.886	ns
Input high delay for global clock	$T_{RCKH}$	1.405	1.489	1.654	1.752	ns
Maximum skew for global clock	$T_{RCKSW}$		0.084		0.098	ns

The following table lists the 050 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 227 • 050 Device Global Resource**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	$T_{RCKL}$	0.827	0.897	0.826	0.896	ns
Input high delay for global clock	$T_{RCKH}$	1.419	1.53	1.671	1.8	ns
Maximum skew for global clock	$T_{RCKSW}$		0.111		0.129	ns

The following table lists the 025 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 228 • 025 Device Global Resource**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	$T_{RCKL}$	0.747	0.799	0.745	0.797	ns
Input high delay for global clock	$T_{RCKH}$	1.294	1.378	1.522	1.621	ns
Maximum skew for global clock	$T_{RCKSW}$		0.084		0.099	ns

**Table 232 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 (continued)**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Address setup time	$T_{ADDRSU}$	0.475		0.559		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.336		0.395		ns
Data hold time	$T_{DHD}$	0.082		0.096		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns
Block select hold time	$T_{BLKHD}$	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		1.529		1.799	ns
Block select minimum pulse width	$T_{BLKMPW}$	0.186		0.219		ns
Read enable setup time	$T_{RDESU}$	0.485		0.57		ns
Read enable hold time	$T_{RDEHD}$	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	$T_{R2Q}$		1.514		1.781	ns
Asynchronous reset removal time	$T_{RSTREM}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTREC}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	$T_{RSTMPW}$	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTSU}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTHD}$	0.036		0.043		ns
Write enable setup time	$T_{WESU}$	0.415		0.488		ns
Write enable hold time	$T_{WEHD}$	0.048		0.057		ns
Maximum frequency	$F_{MAX}$		400		340	MHz

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 233 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	$T_{CY}$	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	$T_{PLCY}$	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns

**Table 238 •  $\mu$ SRAM (RAM64x16) in 64 x 16 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read synchronous reset hold time	$T_{SRSTHD}$	0.061		0.071		ns
Write clock period	$T_{CCY}$	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	$T_{BLKCSU}$	0.404		0.476		ns
Write block hold time	$T_{BLKCHD}$	0.007		0.008		ns
Write input data setup time	$T_{DINCSU}$	0.115		0.135		ns
Write input data hold time	$T_{DINCHD}$	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.026		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

The following table lists the  $\mu$ SRAM in 128 x 9 mode in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 239 •  $\mu$ SRAM (RAM128x9) in 128 x 9 Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	$T_{CY}$	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	$T_{PLCY}$	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	$T_{CLK2Q}$		0.266		0.313	ns
Read access time without pipeline register				1.677		1.973
Read address setup time in synchronous mode	$T_{ADDRSU}$	0.301		0.354		ns
Read address setup time in asynchronous mode			1.856		2.184	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.091		0.107		ns
Read address hold time in asynchronous mode			-0.778		-0.915	
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHD}$	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.036		2.396	ns

**Table 241 •  $\mu$ SRAM (RAM256x4) in 256 x 4 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Write address hold time	$T_{ADDRCHD}$	0.245		0.288		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.03		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

The following table lists the  $\mu$ SRAM in 512 x 2 mode in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 242 •  $\mu$ SRAM (RAM512x2) in 512 x 2 Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	$T_{CY}$	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	$T_{PLCY}$	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	$T_{CLK2Q}$		0.27		0.31	ns
Read access time without pipeline register				1.76		2.08
Read address setup time in synchronous mode	$T_{ADDRSU}$	0.301		0.354		ns
Read address setup time in asynchronous mode			1.96		2.306	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.137		0.161		ns
Read address hold time in asynchronous mode			-0.58		-0.68	
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHD}$	-0.65		-0.77		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.14		2.52	ns
Read asynchronous reset removal time (pipelined clock)	$T_{RSTREM}$	-0.02		-0.03		ns
Read asynchronous reset removal time (non-pipelined clock)			0.046		0.054	
Read asynchronous reset recovery time (pipelined clock)	$T_{RSTREC}$	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)			0.236		0.278	
Read asynchronous reset to output propagation delay (with pipelined register enabled)	$T_{R2Q}$		0.83		0.98	ns
Read synchronous reset setup time	$T_{SRSTSU}$	0.271		0.319		ns
Read synchronous reset hold time	$T_{SRSTHD}$	0.061		0.071		ns

**Table 251 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only) (continued)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
150	544496	10	158	15	Sec

**Table 252 • SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	9	61	11	Sec
010	842688	15	107	21	Sec
025	1497408	26	121	35	Sec
050	2695168	43	141	55	Sec
060	2686464	48	143	60	Sec
090	4190208	75	244	91	Sec
150	6682768	117	296	141	Sec

**Table 253 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	Unit
	100 kHz	25 MHz	12.5 MHz	
005	47	27	28	Sec
010	77	35	35	Sec
025	150	42	41	Sec
050	33 <sup>1</sup>	Not Supported	Not Supported	Sec
060	291	83	82	Sec
090	427	109	108	Sec
150	708	157	160	Sec

1. Auto Programming in 050 device is done through SC\_SPI, and SPI CLK is set to 6.25 MHz.

**Table 254 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	Unit
	100 kHz	25 MHz	12.5 MHz	
005	41	48	49	Sec
010	86	87	87	Sec
025	87	85	86	Sec
050	85	Not Supported	Not Supported	Sec
060	78	86	86	Sec
090	154	162	162	Sec