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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 10K Logic Modules
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s010-1fgg484i">https://www.e-xfl.com/product-detail/microchip-technology/m2s010-1fgg484i</a>



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## 2.2 References

The following documents are recommended references:

- *PB0121: IGLOO2 Product Brief*
- *DS0124: IGLOO2 Pin Descriptions*
- *PB0115: SmartFusion2 SoC FPGA Product Brief*
- *DS0115: SmartFusion2 Pin Descriptions*

All product documentation for IGLOO2 and SmartFusion2 is available at:

<http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga>

<http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#overview>

## 2.3 Electrical Specifications

### 2.3.1 Operating Conditions

The following table lists the stress limits. Stress applied above the specified limit may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table are not implied.

**Table 3 • Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Unit
DC core supply voltage. Must always power this pin.	$V_{DD}$	-0.3	1.32	V
Power supply for charge pumps (for normal operation and programming). Must always power this pin.	$V_{PP}$	-0.3	3.63	V
Analog power pad for MDDR PLL	MSS_MDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	HPMS_MDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for FDDR PLL	FDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_MSS_MDDR_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_HPMS_MDDR_VDDA	-0.3	3.63	V
Analog power pad for PLL0-5	CCC_XX[01]_PLL_VDDA	-0.3	3.63	V
High supply voltage for PLL SerDes[01]	SERDES_[01]_PLL_VDDA	-0.3	3.63	V
Analog power for SerDes[01] PLL lane0 to lane3. This is a 2.5 V SerDes internal PLL supply.	SERDES_[01]_L[0123]_VDDAPLL	-0.3	2.75	V
TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply.	SERDES_[01]_L[0123]_VDDAIO	-0.3	1.32	V
PCIe/PCS power supply	SERDES_[01]_VDD	-0.3	1.32	V
DC FPGA I/O buffer supply voltage for MSIO I/O bank	$V_{DDIx}$	-0.3	3.63	V
DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks	$V_{DDIx}$	-0.3	2.75	V
I/O Input voltage for MSIO I/O bank	$V_I$	-0.3	3.63	V
I/O Input voltage for MSIOD/DDRIO I/O bank	$V_I$	-0.3	2.75	V
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to $V_{PP}$ .	$V_{PPNVM}$	-0.3	3.63	V
Storage temperature <sup>1</sup>	$T_{STG}$	-65	150	°C
Junction temperature	$T_J$	-55	135	°C

**Table 4 • Recommended Operating Conditions (continued)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
3.3 V DC supply voltage	$V_{DDIX}$	3.15	3.3	3.45	V	
LVDS differential I/O	$V_{DDIX}$	2.375	2.5	3.45	V	
B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O	$V_{DDIX}$	2.375	2.5	2.625	V	
LVPECL differential I/O	$V_{DDIX}$	3.15	3.3	3.45	V	
Reference voltage supply for FDDR (Bank0) and MDDR (Bank5)	$V_{REFX}$	0.49 × $V_{DDIX}$	0.5 × $V_{DDIX}$	0.51 × $V_{DDIX}$	V	
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to $V_{PP}$ .	$V_{PPNVM}$	2.375 3.15	2.5 3.3	2.625 3.45	V	2.5 V range 3.3 V range

1. Programming at Industrial temperature range is available only with  $V_{PP} = 3.3$  V.

**Note:** Power supply ramps must all be strictly monotonic, without plateaus.

**Table 5 • FPGA Operating Limits**

Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Digest Temperature	Digest Cycles	Retention (Biased/Unbiased)
Commercial	FPGA	Min $T_J = 0$ °C Max $T_J = 85$ °C	Min $T_J = 0$ °C Max $T_J = 85$ °C	500	Min $T_J = 0$ °C Max $T_J = 85$ °C	2000	20 years
Industrial <sup>1</sup>	FPGA	Min $T_J = -40$ °C Max $T_J = 100$ °C	Min $T_J = -40$ °C Max $T_J = 100$ °C	500	Min $T_J = -40$ °C Max $T_J = 100$ °C	2000	20 years

1. Programming at Industrial temperature range is available only with  $V_{PP} = 3.3$  V.

**Note:** The retention specification is defined as the total number of programming and digest cycles. For example, 20 years of retention after 500 programming cycles.

**Note:** The digest cycle specification is 2000 digest cycles for every program cycle with a maximum of 500 programming cycles.

**Note:** If your product qualification requires accelerated programming cycles, see [Microsemi SoC Products Quality and Reliability Report](#) about recommended methodologies.

**Table 15 • Inrush Currents at Power up,  $-40\text{ }^{\circ}\text{C} \leq T_J \leq 100\text{ }^{\circ}\text{C}$  – Typical Process**

Power Supplies	Voltage (V)	005	010	025	050	060	090	150	Unit
$V_{DD}$	1.26	25	32	38	48	45	77	109	mA
$V_{PP}$	3.46	33	49	36	180	13	36	51	mA
$V_{DDI}$	2.62	134	141	161	187	93	272	388	mA
Number of banks		7	8	8	10	10	9	19	

### 2.3.3 Average Fabric Temperature and Voltage Derating Factors

The following table lists the average temperature and voltage derating factors for fabric timing delays normalized to  $T_J = 85\text{ }^{\circ}\text{C}$ , in worst-case  $V_{DD} = 1.14\text{ V}$ .

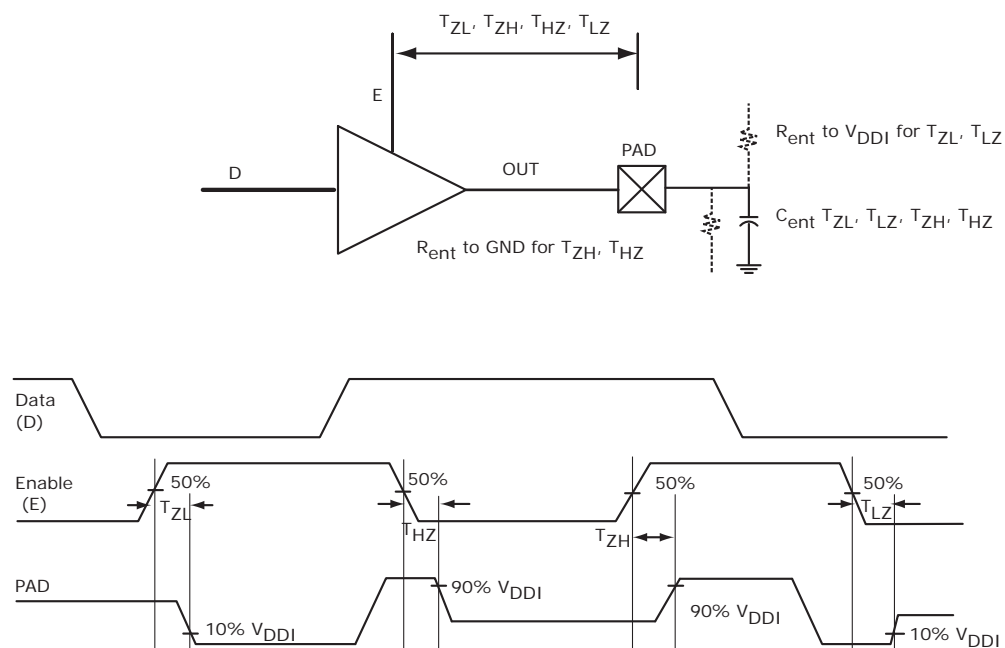
**Table 16 • Average Junction Temperature and Voltage Derating Factors for Fabric Timing Delays**

Array Voltage $V_{DD}$ (V)	$-40\text{ }^{\circ}\text{C}$	$0\text{ }^{\circ}\text{C}$	$25\text{ }^{\circ}\text{C}$	$70\text{ }^{\circ}\text{C}$	$85\text{ }^{\circ}\text{C}$	$100\text{ }^{\circ}\text{C}$
1.14	0.83	0.89	0.92	0.98	<b>1.00</b>	1.02
1.2	0.75	0.80	0.83	0.89	0.91	0.93
1.26	0.69	0.73	0.76	0.81	0.83	0.85

### 2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

**Figure 5 • Tristate Buffer for Enable Path Test Point**



### 2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

**Table 18 • Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	630			Mbps
LVTTL 3.3 V	600			Mbps
LVC MOS 3.3 V	600			Mbps
LVC MOS 2.5 V	410	420	400	Mbps
LVC MOS 1.8 V	295	400	400	Mbps
LVC MOS 1.5 V	160	220	235	Mbps
LVC MOS 1.2 V	120	160	200	Mbps
LPDDR-LVC MOS 1.8 V mode			400	Mbps



**Table 19 • Maximum Data Rate Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
LPDDR			400	Mbps
HSTL1.5 V			400	Mbps
SSTL 2.5 V	510	700	400	Mbps
SSTL 1.8 V			667	Mbps
SSTL 1.5 V			667	Mbps

**Table 20 • Maximum Data Rate Summary Table for Differential I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	Unit
LVPECL (input only)	900		Mbps
LVDS 3.3 V	535		Mbps
LVDS 2.5 V	535	700	Mbps
RSDS	520	700	Mbps
BLVDS	500		Mbps
MLVDS	500		Mbps
Mini-LVDS	520	700	Mbps

**Table 21 • Maximum Frequency Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	315			MHz
LVTTTL 3.3 V	300			MHz
LVC MOS 3.3 V	300			MHz
LVC MOS 2.5 V	205	210	200	MHz
LVC MOS 1.8 V	147.5	200	200	MHz
LVC MOS 1.5 V	80	110	118	MHz
LVC MOS 1.2 V	60	80	100	MHz
LPDDR– LVC MOS 1.8 V mode			200	MHz

**Table 22 • Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
LPDDR			200	MHz
HSTL1.5 V			200	MHz
SSTL 2.5 V	255	350	200	MHz
SSTL 1.8 V			334	MHz
SSTL 1.5 V			334	MHz

**Table 23 • Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	Unit
LVPECL (input only)	450		MHz
LVDS 3.3 V	267.5		MHz
LVDS 2.5 V	267.5	350	MHz
RSDS	260	350	MHz
BLVDS	250		MHz
MLVDS	250		MHz
Mini-LVDS	260	350	MHz

### 2.3.6.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 103 • DDR1/SSTL2 DC Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V
Termination voltage	$V_{TT}$	1.164	1.250	1.339	V
Input reference voltage	$V_{REF}$	1.164	1.250	1.339	V

**Table 104 • DDR1/SSTL2 DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}$ (DC)	$V_{REF} + 0.15$	2.625	V
DC input logic low	$V_{IL}$ (DC)	-0.3	$V_{REF} - 0.15$	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 105 • DDR1/SSTL2 DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
<b>SSTL2 Class I (DDR Reduced Drive)</b>				
DC output logic high	$V_{OH}$	$V_{TT} + 0.608$		V
DC output logic low	$V_{OL}$		$V_{TT} - 0.608$	V
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	8.1		mA
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-8.1		mA
<b>SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Bank Only</b>				
DC output logic high	$V_{OH}$	$V_{TT} + 0.81$		V
DC output logic low	$V_{OL}$		$V_{TT} - 0.81$	V
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	16.2		mA
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-16.2		mA

**Table 106 • DDR1/SSTL2 DC Differential Voltage Specification**

Parameter	Symbol	Min	Unit
DC input differential voltage	$V_{ID}$ (DC)	0.3	V

### 2.3.6.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 139 • LPDDR DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max
Supply voltage	$V_{DDI}$	1.71	1.8	1.89
Termination voltage	$V_{TT}$	0.838	0.900	0.964
Input reference voltage	$V_{REF}$	0.838	0.900	0.964

**Table 140 • LPDDR DC Input Voltage Specification**

Parameter	Symbol	Min	Max
DC input logic high	$V_{IH}$ (DC)	$0.7 \times V_{DDI}$	1.89
DC input logic low	$V_{IL}$ (DC)	-0.3	$0.3 \times V_{DDI}$
Input current high <sup>1</sup>	$I_{IH}$ (DC)		
Input current low <sup>1</sup>	$I_{IL}$ (DC)		

1. See Table 24, page 22.

**Table 141 • LPDDR DC Output Voltage Specification Reduced Drive**

Parameter	Symbol	Min	Max
DC output logic high	$V_{OH}$	$0.9 \times V_{DDI}$	
DC output logic low	$V_{OL}$		$0.1 \times V_{DDI}$
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	0.1	
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-0.1	

**Table 142 • LPDDR DC Output Voltage Specification Full Drive<sup>1</sup>**

Parameter	Symbol	Min	Max
DC output logic high	$V_{OH}$	$0.9 \times V_{DDI}$	
DC output logic low	$V_{OL}$		$0.1 \times V_{DDI}$
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	0.1	
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-0.1	

1. To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.

**Table 143 • LPDDR DC Differential Voltage Specification**

Parameter	Symbol	Min
DC input differential voltage	$V_{ID}$ (DC)	$0.4 \times V_{DDI}$

**Table 156 • LPDDR-LVCMOS 1.8 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	0.9	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**Table 157 • LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification for DDRIO Bank**

Output Drive Selection	$V_{OH}$ (V) Min	$V_{OL}$ (V) Max	$I_{OH}$ (at $V_{OH}$ ) mA	$I_{OL}$ (at $V_{OL}$ ) mA
2 mA	$V_{DDI} - 0.45$	0.45	2	2
4 mA	$V_{DDI} - 0.45$	0.45	4	4
6 mA	$V_{DDI} - 0.45$	0.45	6	6
8 mA	$V_{DDI} - 0.45$	0.45	8	8
10 mA	$V_{DDI} - 0.45$	0.45	10	10
12 mA	$V_{DDI} - 0.45$	0.45	12	12
16 mA <sup>1</sup>	$V_{DDI} - 0.45$	0.45	16	16

1. 16 mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance.

**Table 158 • LPDDR-LVCMOS 1.8V AC Switching Characteristics for Receiver (for DDRIO I/O Bank with Fixed Code - Input Buffers)**

ODT (On Die Termination)	-1	-Std	-1	-Std	Unit
None	1.968	2.315	2.099	2.47	ns

**Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	medium_fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4 mA	slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	medium_fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6 mA	slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	medium_fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns
8 mA	slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns

**Table 215 • LVPECL DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	$V_I$	0	3.45	V

**Table 216 • LVPECL DC Differential Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
Input common mode voltage	$V_{ICM}$	0.3		2.8	V
Input differential voltage	$V_{IDIFF}$	100	300	1,000	mV

**Table 217 • LVPECL Minimum and Maximum AC Switching Speeds**

Parameter	Symbol	Max	Unit
Maximum data rate	$D_{MAX}$	900	Mbps

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$ .

**Table 218 • LVPECL Receiver Characteristics for MSIO I/O Bank**

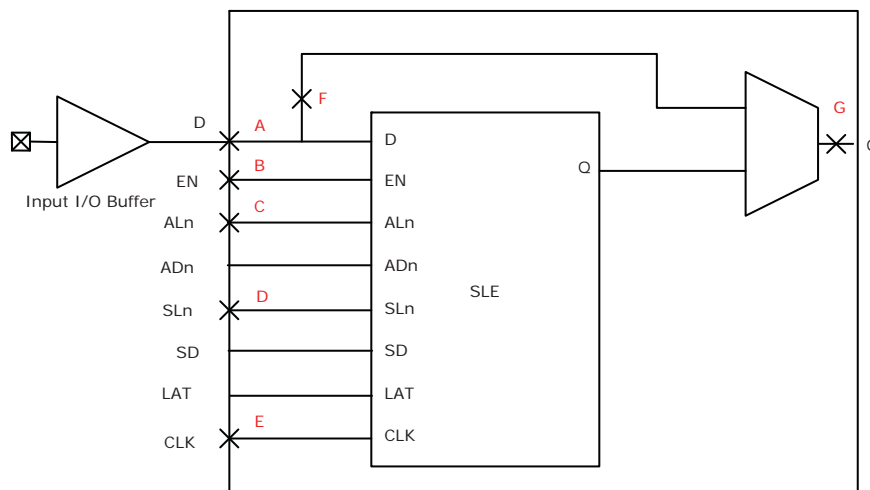
On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.572	3.025	ns
100	2.569	3.023	ns

**2.3.8 I/O Register Specifications**

This section describes input and output register specifications.

**2.3.8.1 Input Register**

**Figure 6 • Timing Model for Input Register**

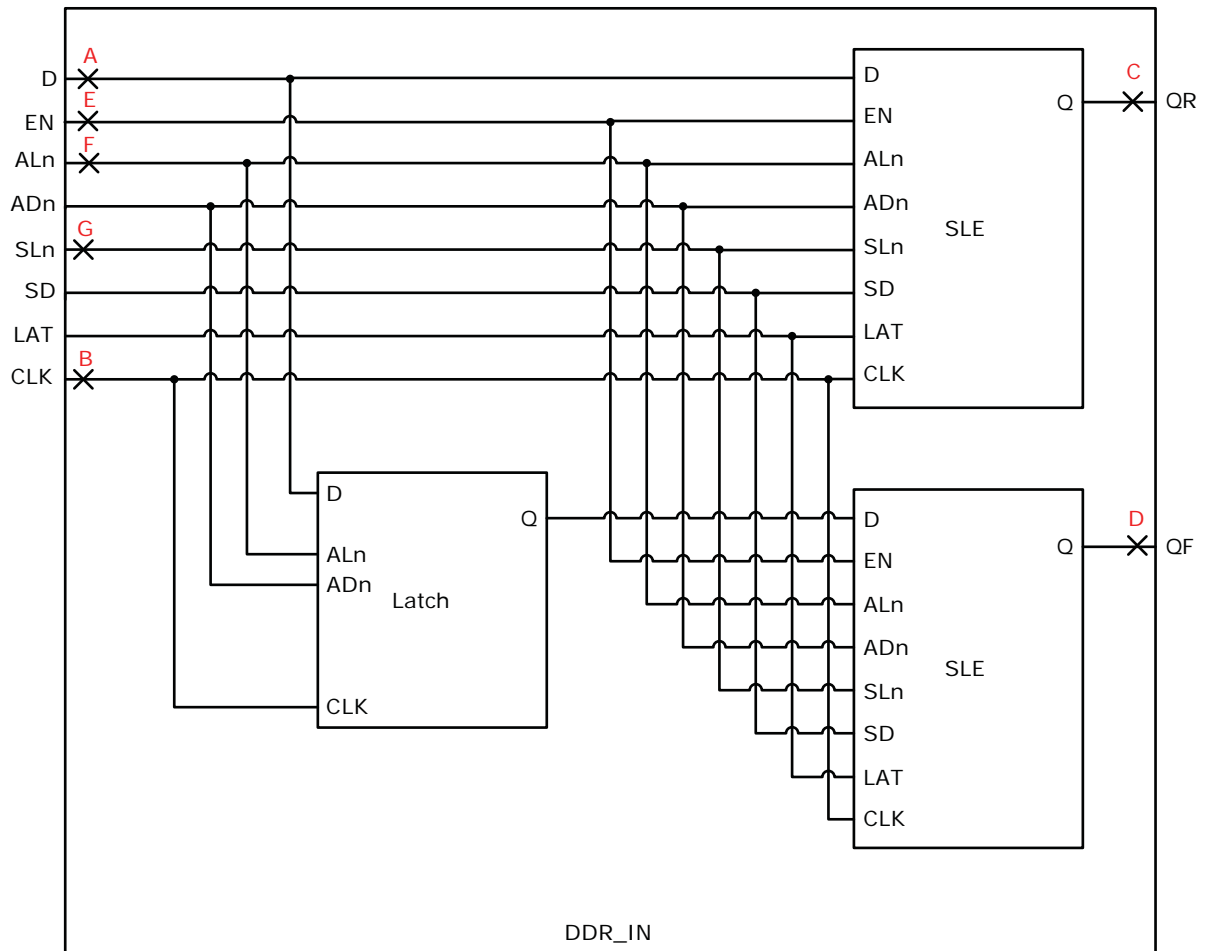


### 2.3.9 DDR Module Specification

This section describes input and output DDR module and timing specifications.

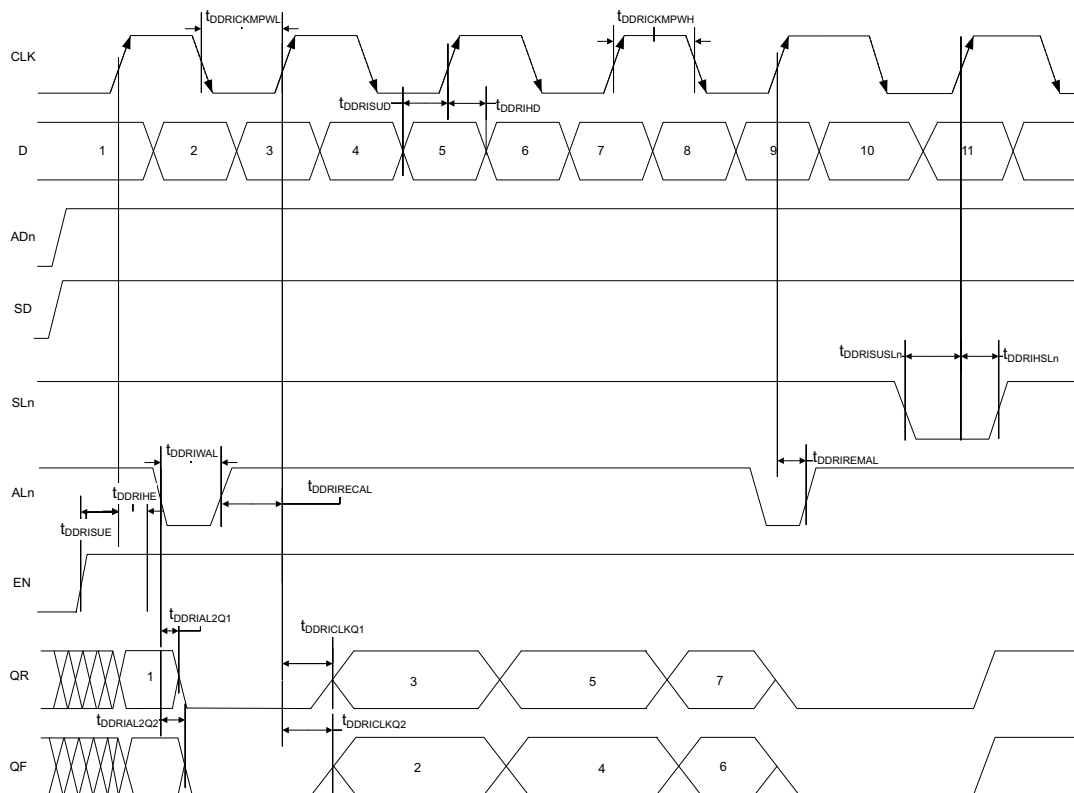
#### 2.3.9.1 Input DDR Module

Figure 10 • Input DDR Module



### 2.3.9.2 Input DDR Timing Diagram

Figure 11 • Input DDR Timing Diagram



### 2.3.9.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 221 • Input DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDRICKLQ1}$	Clock-to-Out Out_QR for input DDR	B, C	0.16	0.188	ns
$T_{DDRICKLQ2}$	Clock-to-Out Out_QF for input DDR	B, D	0.166	0.195	ns
$T_{DDRISUD}$	Data setup for input DDR	A, B	0.357	0.421	ns
$T_{DDRHD}$	Data hold for input DDR	A, B	0	0	ns
$T_{DDRISUE}$	Enable setup for input DDR	E, B	0.46	0.542	ns
$T_{DDRHE}$	Enable hold for input DDR	E, B	0	0	ns
$T_{DDRISUSLn}$	Synchronous load setup for input DDR	G, B	0.46	0.542	ns
$T_{DDRHSLn}$	Synchronous load hold for input DDR	G, B	0	0	ns
$T_{DDRIR2Q1}$	Asynchronous load-to-out QR for input DDR	F, C	0.587	0.69	ns
$T_{DDRIR2Q2}$	Asynchronous load-to-out QF for input DDR	F, D	0.541	0.636	ns
$T_{DDRIREMAL}$	Asynchronous load removal time for input DDR	F, B	0	0	ns
$T_{DDRIRECAL}$	Asynchronous load recovery time for input DDR	F, B	0.074	0.087	ns



**Table 276 • Cryptographic Block Characteristics (continued)**

Service	Conditions	Timing	Unit
SHA256	512 bits	540	kbps
	1024 bits	780	kbps
	2048 bits	950	kbps
	24 kbits	1140	kbps
HMAC	512 bytes	820	kbps
	1024 bytes	890	kbps
	2048 bytes	930	kbps
	24 kbytes	980	kbps
KeyTree		1.8	ms
Challenge-response	PUF = OFF	25	ms
	PUF = ON	7	ms
ECC point multiplication		590	ms
ECC point addition		8	ms

1. Using cypher block chaining (CBC) mode.

### 2.3.19 Crystal Oscillator

The following table describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

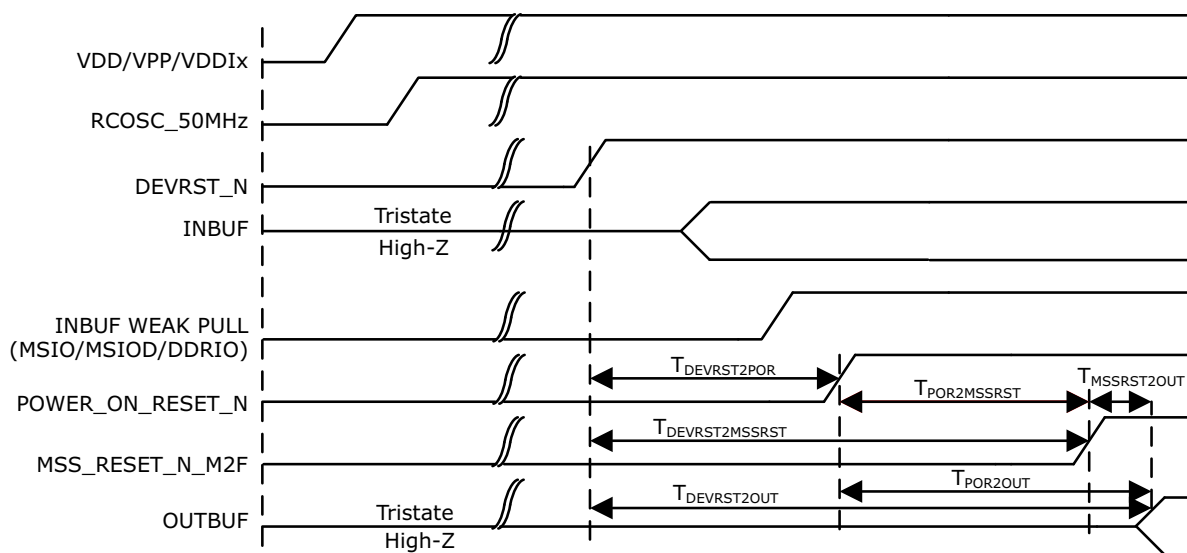
**Table 277 • Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)**

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		20		MHz	
Accuracy	ACCXTAL			0.0047	%	005, 010, 025, 050, 060, and 090 devices
				0.0058	%	150 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		200	300	ps	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		200	300	ps	010, 025, 050, and 060 devices
			250	410	ps	150 devices
			250	550	ps	005 and 090 devices
Operating current	IDYNXTAL		1.5		mA	010, 050, and 060 devices
			1.65		mA	005, 025, 090, and 150 devices
Input logic level high	VIHXTAL	0.9 V <sub>PP</sub>			V	
Input logic level low	VILXTAL			0.1 V <sub>PP</sub>	V	

**Table 291 • DEVRST\_N to Functional Times for SmartFusion2 (continued)**

Symbol	From	To	Description	Maximum Power-up to Functional Time for SmartFusion2 (uS)						
				005	010	025	050	060	090	150
$T_{DEVRST2POR}$	DEVRST_N	POWER_ON_RESET_N	$V_{DD}$ at its minimum threshold level to fabric	233	289	216	213	237	234	219
$T_{DEVRST2MSSRST}$	DEVRST_N	MSS_RESET_N_M2F	$V_{DD}$ at its minimum threshold level to MSS	702	765	712	688	636	630	866
$T_{DEVRST2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215

**Figure 19 • DEVRST\_N to Functional Timing Diagram for SmartFusion2**

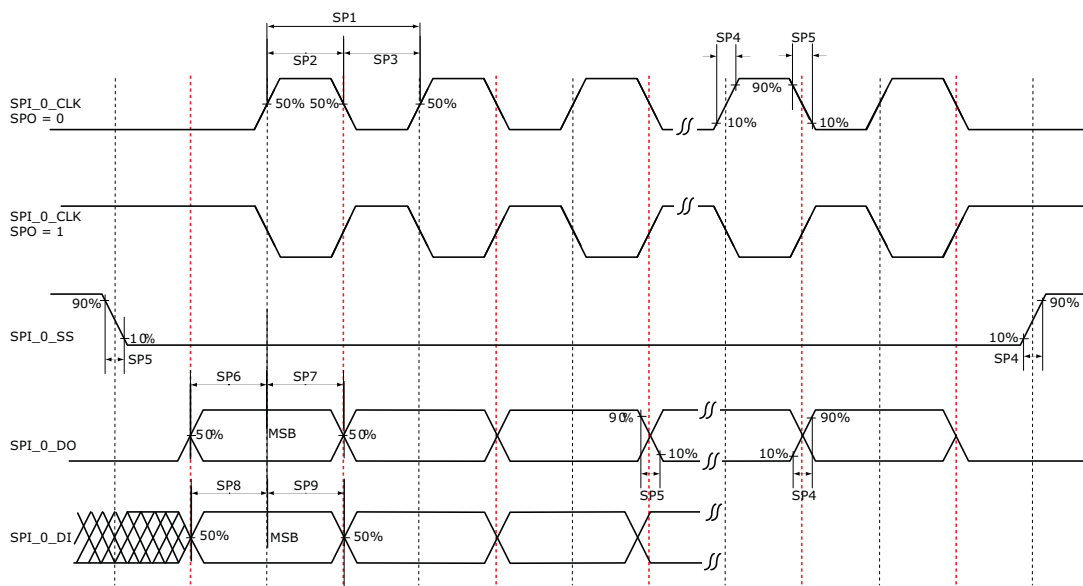


**Table 305 • SPI Characteristics for All Devices (continued)**

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%–90%) <sup>1</sup>		2.906		ns	IO Configuration: LVCMOS 2.5 V-8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0 1]_DI setup time <sup>2</sup>	12			ns	
sp9m	SPI_[0 1]_DI hold time <sup>2</sup>	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0 1]_DI setup time <sup>2</sup>	2			ns	
sp9s	SPI_[0 1]_DI hold time <sup>2</sup>	7			ns	
SPI master configuration (applicable for 060, 090, and 150 devices)						
sp6m	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 7.0			ns	
sp7m	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 9.5			ns	
sp8m	SPI_[0 1]_DI setup time <sup>2</sup>	15			ns	
sp9m	SPI_[0 1]_DI hold time <sup>2</sup>	–2.5			ns	
SPI slave configuration (applicable for 060, 090, and 150 devices)						
sp6s	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 16.0			ns	
sp7s	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 3.5			ns	
sp8s	SPI_[0 1]_DI setup time <sup>2</sup>	3			ns	
sp9s	SPI_[0 1]_DI hold time <sup>2</sup>	2.5			ns	

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. For allowable pclk configurations, see Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

Figure 22 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)



### 2.3.32 CAN Controller Characteristics

The following table lists the CAN controller characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 306 • CAN Controller Characteristics

Parameter	Description	-1	-Std	Unit
FCANREFCLK <sup>1</sup>	Internally sourced CAN reference clock frequency	160	136	MHz
BAUDCANMAX	Maximum CAN performance baud rate	1	1	Mbps
BAUDCANMIN	Minimum CAN performance baud rate	0.05	0.05	Mbps

1. PCLK to CAN controller must be a multiple of 8 MHz.

### 2.3.33 USB Characteristics

The following table lists the USB characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 307 • USB Characteristics

Parameter	Description	-1	-Std	Unit
FUSBREFCLK	Internally sourced USB reference clock frequency	166	142	MHz
TUSBCLK	USB clock period	16.66	16.66	ns
TUSBPD	Clock to USB data propagation delay	9.0	9.0	ns
TUSBSU	Setup time for USB data	6.0	6.0	ns
TUSBHD	Hold time for USB data	0	0	ns

## 2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 308 • MMUART Characteristics**

Parameter	Description	–1	–Std	Unit
FMMUART_REF_CLK	Internally sourced MMUART reference clock frequency.	166	142	MHz
BAUDMMUARTTx	Maximum transmit baud rate	10.375	8.875	Mbps
BAUDMMUARTRx	Maximum receive baud rate	10.375	8.875	Mbps

## 2.3.35 IGLOO2 Specifications

### 2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 309 • Maximum Frequency for HPMS Main Clock**

Symbol	Description	–1	–Std	Unit
HPMS_CLK	Maximum frequency for the HPMS main clock	166	142	MHz

### 2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI\_0\_CLK. For timing parameter definitions, see [Figure 23](#), page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 310 • SPI Characteristics for All Devices**

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPIFMAX	Maximum operating frequency of SPI interface			20	MHz	
sp1	SPI_[0 1]_CLK minimum period					
	SPI_[0 1]_CLK = PCLK/2	12			ns	
	SPI_[0 1]_CLK = PCLK/4	24.1			ns	
	SPI_[0 1]_CLK = PCLK/8	48.2			ns	
	SPI_[0 1]_CLK = PCLK/16	0.1			$\mu\text{s}$	
	SPI_[0 1]_CLK = PCLK/32	0.19			$\mu\text{s}$	
	SPI_[0 1]_CLK = PCLK/64	0.39			$\mu\text{s}$	
SPI_[0 1]_CLK = PCLK/128	0.77			$\mu\text{s}$		