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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 10K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s010-fg484">https://www.e-xfl.com/product-detail/microchip-technology/m2s010-fg484</a>

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- Added [Table 244](#), page 94 and [Table 256](#), page 99 (SAR 73971).
- Updated the [SerDes Electrical and Timing AC and DC Characteristics](#), page 121 (SAR 71171).
- Added the [DEVRST\\_N Characteristics](#), page 116 (SAR 64100, 72103).
- Added [Table 298](#), page 122 (SAR 71897).
- Updated [Table 25](#), page 22, [Table 26](#), page 23, and [Table 27](#), page 23 (SAR 74570).
- Added 060 devices in [Table 277](#), page 107, [Table 278](#), page 108, and [Table 279](#), page 108 (SAR 57898).
- Updated duty cycle parameter of crystal in [Table 280](#), page 109 and [Table 281](#), page 109 (SAR 57898).
- Added 32 KHz mode PLL acquisition time in [Table 282](#), page 110 (SAR 68281).
- Updated [Table 293](#), page 119 for 060 devices (SAR 57828).
- Updated [Table 297](#), page 122 for CID value (SAR 70878).

## 1.4 Revision 8.0

The following is a summary of the changes in revision 8.0 of this document.

- Updated [Table 11](#), page 12 (SAR 69218).
- Updated [Table 12](#), page 13 (SAR 69218).
- Updated [Table 283](#), page 111 (SAR 69000).

## 1.5 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Updated [Table 1](#), page 4(SAR 68620).

## 1.6 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- Updated [Table 5](#), page 7 (SAR 65949).
- Updated [Table 9](#), page 10 (SAR 62995).
- Updated [Table 123](#), page 47 and [Table 133](#), page 49 (SAR 67210).
- Added [Embedded NVM \(eNVM\) Characteristics](#), page 104 (SAR 52509).
- Updated [Table 277](#), page 107 (SAR 64855).
- Updated [Table 282](#), page 110 (SAR 65958 and SAR 56666).
- Added [DDR Memory Interface Characteristics](#), page 120 (SAR 66223).
- Added [SFP Transceiver Characteristics](#), page 120 (SAR 63105).
- Updated [Table 302](#), page 123 and [Table 309](#), page 129 (SAR 66314).

## 1.7 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Updated [Table 1](#), page 4.
- Updated [Table 4](#), page 6 for  $T_J$  symbol information.
- Updated [Table 5](#), page 7 (SAR 63109).
- Updated [Table 9](#), page 10.
- Updated [Table 282](#), page 110 (SAR 62012).
- Added [Table 290](#), page 116 (SAR 64100).
- Added [Table 306](#), page 128, [Table 307](#), page 128 (SAR 50424).

## 1.8 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document.

- Updated [Table 1](#), page 4. Changed the Status of 090 devices to "Production" (SAR 62750).
- Updated [Figure 10](#), page 70. Removed inverter bubble from DDR\_IN latch (SAR 61418).
- Updated [SerDes Electrical and Timing AC and DC Characteristics](#), page 121 (SAR 62836).

**Table 11 • SmartFusion2 and IGLOO2 Quiescent Supply Current ( $V_{DD} = 1.2\text{ V}$ ) – Typical Process**

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC2	Flash*Freeze	1.4	2.6	3.7	5.1	5.0	5.1	8.9	mA	Typical ( $T_J = 25\text{ }^\circ\text{C}$ )
		12.0	20.0	26.6	35.3	35.4	35.7	57.8	mA	Commercial ( $T_J = 85\text{ }^\circ\text{C}$ )
		18.5	30.8	41.0	54.5	54.5	55.0	89.0	mA	Industrial ( $T_J = 100\text{ }^\circ\text{C}$ )

**Table 12 • SmartFusion2 and IGLOO2 Quiescent Supply Current ( $V_{DD} = 1.26\text{ V}$ ) – Worst-Case Process**

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC1	Non-Flash*Freeze	43.8	57.0	84.6	132.3	161.4	163.0	242.5	mA	Commercial ( $T_J = 85\text{ }^\circ\text{C}$ )
		65.3	85.7	127.8	200.9	245.4	247.8	369.0	mA	Industrial ( $T_J = 100\text{ }^\circ\text{C}$ )
IDC2	Flash*Freeze	29.1	45.6	51.7	62.7	69.3	70.0	84.8	mA	Commercial ( $T_J = 85\text{ }^\circ\text{C}$ )
		44.9	70.3	79.7	96.5	106.8	107.8	130.6	mA	Industrial ( $T_J = 100\text{ }^\circ\text{C}$ )

### 2.3.2.2 Programming Currents

The following tables represent programming, verify and Inrush currents for SmartFusion2 SoC and IGLOO2 FPGA devices.

**Table 13 • Currents During Program Cycle,  $0\text{ }^\circ\text{C} \leq T_J \leq 85\text{ }^\circ\text{C}$  – Typical Process**

Power Supplies	Voltage (V)	005	010	025	050	060	090	150 <sup>1</sup>	Unit
$V_{DD}$	1.26	46	53	55	58	30	42	52	mA
$V_{PP}$	3.46	8	11	6	10	9	12	12	mA
$V_{PPNVM}$	3.46	1	2	2	3	3	3		mA
$V_{DDI}$	2.62	31	16	17	1	12	12	81	mA
	3.46	62	31	36	1	12	17	84	mA
Number of banks		7	8	8	10	10	9	19	

1.  $V_{PP}$  and  $V_{PPNVM}$  are internally shorted.

**Table 14 • Currents During Verify Cycle,  $0\text{ }^\circ\text{C} \leq T_J \leq 85\text{ }^\circ\text{C}$  – Typical Process**

Power Supplies	Voltage (V)	005	010	025	050	060	090	150 <sup>1</sup>	Unit
$V_{DD}$	1.26	44	53	55	58	33	41	51	mA
$V_{PP}$	3.46	6	5	3	15	8	11	12	mA
$V_{PPNVM}$	3.46	1	0	0	1	1	1		mA
$V_{DDI}$	2.62	31	16	17	1	12	11	81	mA
	3.46	61	32	36	1	12	17	84	mA
Number of banks		7	8	8	10	10	9	19	

1.  $V_{PP}$  and  $V_{PPNVM}$  are internally shorted.



**Table 15 • Inrush Currents at Power up,  $-40\text{ }^{\circ}\text{C} \leq T_J \leq 100\text{ }^{\circ}\text{C}$  – Typical Process**

Power Supplies	Voltage (V)	005	010	025	050	060	090	150	Unit
$V_{DD}$	1.26	25	32	38	48	45	77	109	mA
$V_{PP}$	3.46	33	49	36	180	13	36	51	mA
$V_{DDI}$	2.62	134	141	161	187	93	272	388	mA
Number of banks		7	8	8	10	10	9	19	

### 2.3.3 Average Fabric Temperature and Voltage Derating Factors

The following table lists the average temperature and voltage derating factors for fabric timing delays normalized to  $T_J = 85\text{ }^{\circ}\text{C}$ , in worst-case  $V_{DD} = 1.14\text{ V}$ .

**Table 16 • Average Junction Temperature and Voltage Derating Factors for Fabric Timing Delays**

Array Voltage $V_{DD}$ (V)	$-40\text{ }^{\circ}\text{C}$	$0\text{ }^{\circ}\text{C}$	$25\text{ }^{\circ}\text{C}$	$70\text{ }^{\circ}\text{C}$	$85\text{ }^{\circ}\text{C}$	$100\text{ }^{\circ}\text{C}$
1.14	0.83	0.89	0.92	0.98	<b>1.00</b>	1.02
1.2	0.75	0.80	0.83	0.89	0.91	0.93
1.26	0.69	0.73	0.76	0.81	0.83	0.85

## 2.3.5.6 Single-Ended I/O Standards

### 2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

### 2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 29 • LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	3.15	3.3	3.45	V

**Table 30 • LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}$ (DC)	2.0	3.45	V
DC input logic low	$V_{IL}$ (DC)	-0.3	0.8	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 31 • LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC output logic high <sup>1</sup>	$V_{OH}$	$V_{DDI} - 0.4$		V
DC output logic low <sup>1</sup>	$V_{OL}$		0.4	V

1. The  $V_{OH}/V_{OL}$  test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

**Table 32 • LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC output logic high	$V_{OH}$	2.4		V
DC output logic low	$V_{OL}$		0.4	V

**Table 33 • LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	600	Mbps	AC loading: 17 pF load, maximum drive/slew

**Table 82 • LVCMOS 1.2 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
	-1	-Std	-1	-Std	
None	4.154	4.887	4.114	4.84	ns
50	6.918	8.139	6.806	8.008	ns
75	5.613	6.603	5.533	6.509	ns
150	4.716	5.549	4.657	5.479	ns

**Table 83 • LVCMOS 1.2 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	6.713	7.897	5.362	6.308	6.723	7.909	7.233	8.51	6.375	7.499	ns
	Medium	5.912	6.955	4.616	5.43	5.915	6.959	6.887	8.102	6.009	7.069	ns
	Medium fast	5.5	6.469	4.231	4.978	5.5	6.471	6.672	7.849	5.835	6.865	ns
	Fast	5.462	6.426	4.194	4.935	5.463	6.427	6.646	7.819	5.828	6.857	ns
4 mA	Slow	6.109	7.186	4.708	5.539	6.098	7.174	8.005	9.418	7.033	8.274	ns
	Medium	5.355	6.299	4.034	4.746	5.338	6.28	7.637	8.985	6.672	7.849	ns
	Medium fast	4.953	5.826	3.685	4.336	4.932	5.802	7.44	8.752	6.499	7.646	ns
	Fast	4.911	5.777	3.658	4.303	4.89	5.754	7.427	8.737	6.488	7.632	ns
6 mA	Slow	5.89	6.929	4.506	5.301	5.874	6.911	8.337	9.808	7.315	8.605	ns
	Medium	5.176	6.089	3.862	4.543	5.155	6.065	7.986	9.394	6.943	8.168	ns
	Medium fast	4.792	5.637	3.523	4.145	4.765	5.606	7.808	9.186	6.775	7.97	ns
	Fast	4.754	5.593	3.486	4.101	4.728	5.563	7.777	9.149	6.769	7.963	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 84 • LVCMOS 1.2 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	6.746	7.937	7.458	8.774	8.172	9.614	9.867	11.608	8.393	9.874	ns
4 mA	Slow	7.068	8.315	6.678	7.857	7.474	8.793	10.986	12.924	9.043	10.638	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 85 • LVCMOS 1.2 V Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.883	4.568	4.868	5.726	5.329	6.269	7.994	9.404	7.527	8.855	ns
4 mA	Slow	3.774	4.44	4.188	4.926	4.613	5.426	8.972	10.555	8.315	9.782	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.11 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

#### Minimum and Maximum DC/AC Input and Output Levels Specification (Applicable to MSIO Bank Only)

**Table 86 • PCI/PCI-X DC Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	3.15	3.3	3.45	V

**Table 87 • PCI/PCI-X DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	$V_I$	0	3.45	V
Input current high <sup>1</sup>	$I_{IH}(DC)$			
Input current low <sup>1</sup>	$I_{IL}(DC)$			

1. See Table 24, page 22.

**Table 88 • PCI/PCI-X DC Output Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	$V_{OH}$		Per PCI specification		V
DC output logic low	$V_{OL}$		Per PCI specification		V

**Table 89 • PCI/PCI-X Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (MSIO I/O bank)	$D_{MAX}$	630	Mbps	AC Loading: per JEDEC specifications

**Table 90 • PCI/PCI-X AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path (falling edge)	$V_{TRIP}$	$0.615 \times V_{DDI}$	V
Measuring/trip point for data path (rising edge)	$V_{TRIP}$	$0.285 \times V_{DDI}$	V
Resistance for data test path	$R_{TT\_TEST}$	25	$\Omega$
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	10	pF

**Table 100 • HSTL AC Test Parameter Specification**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	0.75	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Reference resistance for data test path for HSTL15 Class I ( $T_{DP}$ )	$RTT\_TEST$	50	$\Omega$
Reference resistance for data test path for HSTL15 Class II ( $T_{DP}$ )	$RTT\_TEST$	25	$\Omega$
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**AC Switching Characteristics**

Worst-case commercial conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ , worst-case  $V_{DDI}$ .

**Table 101 • HSTL Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)**

		$T_{PY}$		
On-Die Termination (ODT)		-1	-Std	Unit
Pseudo differential	None	1.605	1.888	ns
	47.8	1.614	1.898	ns
True differential	None	1.622	1.909	ns
	47.8	1.628	1.916	ns

**Table 102 • HSTL Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
<b>HSTL Class I</b>											
Single-ended	2.6	3.059	2.514	2.958	2.514	2.958	2.431	2.86	2.431	2.86	ns
Differential	2.621	3.083	2.648	3.115	2.647	3.113	2.925	3.442	2.923	3.44	ns
<b>HSTL Class II</b>											
Single-ended	2.511	2.954	2.488	2.927	2.49	2.93	2.409	2.833	2.411	2.836	ns
Differential	2.528	2.974	2.552	3.003	2.551	3.001	2.897	3.409	2.896	3.408	ns

**2.3.6.2 Stub-Series Terminated Logic**

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$ .

**Table 210 • RSDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.855	3.359	ns
100	2.85	3.353	ns

**Table 211 • RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.602	3.061	ns
100	2.597	3.055	ns

**Table 212 • RSDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.097	2.467	2.303	2.709	2.291	2.695	1.961	2.307	1.947	2.29	ns

**Table 213 • RSDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
No pre-emphasis	1.614	1.899	1.559	1.834	1.55	1.823	1.59	1.87	1.575	1.852	ns
Min pre-emphasis	1.604	1.887	1.742	2.05	1.728	2.032	1.889	2.222	1.858	2.185	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

**2.3.7.6 LVPECL**

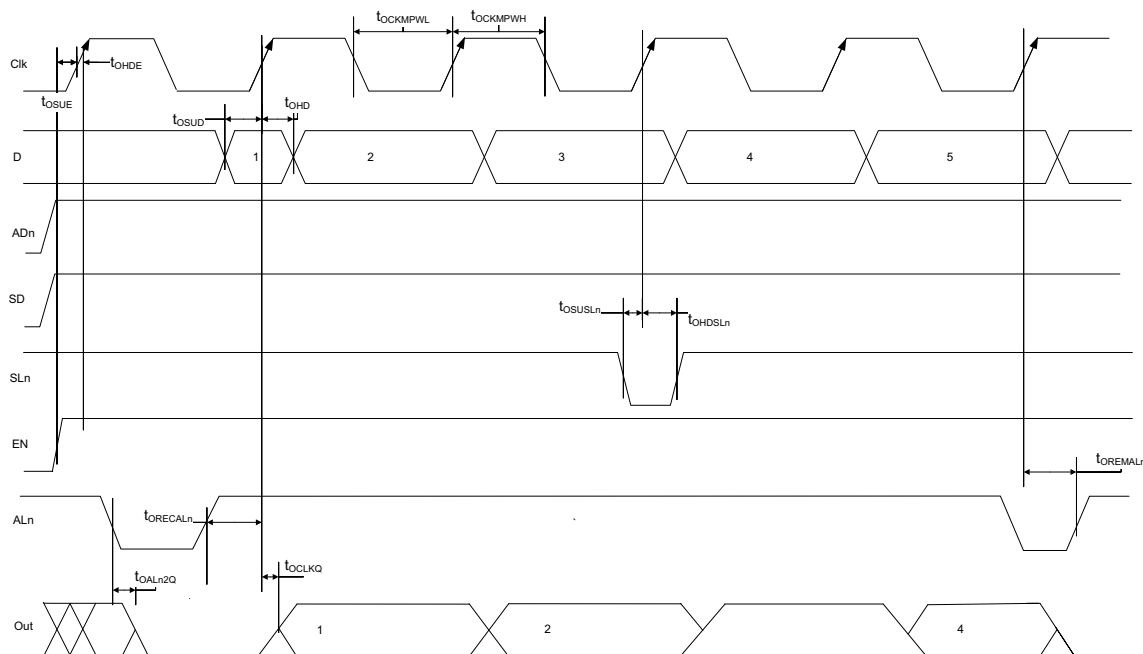
Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

**Minimum and Maximum Input and Output Levels (Applicable to MSIO I/O Bank Only)**

**Table 214 • LVPECL Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	3.15	3.3	3.45	V

**Figure 9 • I/O Register Output Timing Diagram**



The following table lists the output/enable propagation delays in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 220 • Output/Enable Data Register Propagation Delays**

Parameter	Symbol	Measuring Nodes (from, to) <sup>1</sup>	-1	-Std	Unit
Bypass delay of the output/enable register	T <sub>OBYB</sub>	F, G or H, I	0.353	0.415	ns
Clock-to-Q of the output/enable register	T <sub>OCLKQ</sub>	E, G or E, I	0.263	0.309	ns
Data setup time for the output/enable register	T <sub>OSUD</sub>	A, E or J, E	0.19	0.223	ns
Data hold time for the output/enable register	T <sub>OHD</sub>	A, E or J, E	0	0	ns
Enable setup time for the output/enable register	T <sub>OSUE</sub>	B, E	0.419	0.493	ns
Enable hold time for the output/enable register	T <sub>OHE</sub>	B, E	0	0	ns
Synchronous load setup time for the output/enable register	T <sub>OSUSL</sub>	D, E	0.196	0.231	ns
Synchronous load hold time for the output/enable register	T <sub>OHSL</sub>	D, E	0	0	ns
Asynchronous clear-to-q of the output/enable register (ADn = 1)	T <sub>OALN2Q</sub>	C, G or C, I	0.505	0.594	ns
Asynchronous preset-to-q of the output/enable register (ADn = 0)		C, G or C, I	0.528	0.621	ns
Asynchronous load removal time for the output/enable register	T <sub>OREMALN</sub>	C, E	0	0	ns
Asynchronous load recovery time for the output/enable register	T <sub>ORECALN</sub>	C, E	0.034	0.04	ns
Asynchronous load minimum pulse width for the output/enable register	T <sub>OWALN</sub>	C, C	0.304	0.357	ns
Clock minimum pulse width high for the output/enable register	T <sub>OACKMPWH</sub>	E, E	0.075	0.088	ns
Clock minimum pulse width low for the output/enable register	T <sub>OACKMPWL</sub>	E, E	0.159	0.187	ns

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

**Table 221 • Input DDR Propagation Delays (continued)**

<b>Symbol</b>	<b>Description</b>	<b>Measuring Nodes (from, to)</b>	<b>-1</b>	<b>-Std</b>	<b>Unit</b>
$T_{DDRIWAL}$	Asynchronous load minimum pulse width for input DDR	F, F	0.304	0.357	ns
$T_{DDRICKMPWH}$	Clock minimum pulse width high for input DDR	B, B	0.075	0.088	ns
$T_{DDRICKMPWL}$	Clock minimum pulse width low for input DDR	B, B	0.159	0.187	ns



**Table 254 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only) (continued)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	Unit
	100 kHz	25 MHz	12.5 MHz	
150	161	161	161	Sec

**Table 255 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	Unit
	100 kHz	25 MHz	12.5 MHz	
005	47	27	28	Sec
010	77	35	35	Sec
025	150	42	41	Sec
050	33 <sup>1</sup>	Not Supported	Not Supported	Sec
060	291	83	82	Sec
090	427	109	108	Sec
150	708	157	160	Sec
005	41	48	49	Sec
010	86	87	87	Sec
025	87	85	86	Sec
050	85	Not Supported	Not Supported	Sec
060	78	86	86	Sec
090	154	162	162	Sec
150	161	161	161	Sec
005	87	67	66	Sec
010	161	113	113	Sec
025	229	120	121	Sec
050	112	Not Supported	Not Supported	Sec
060	368	161	158	Sec
090	582	261	260	Sec
150	867	309	310	Sec

1. Auto Programming in 050 device is done through SC\_SPI, and SPI CLK is set to 6.25 MHz.

**Table 265 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	69	49	50	Sec
010	99	57	57	Sec
025	150	64	63	Sec
050	55 <sup>1</sup>	Not Supported	Not Supported	Sec
060	313	105	104	Sec
090	449	131	130	Sec
150	730	179	183	Sec

1. Auto programming in 050 device is done through SC\_SPI, and SPI CLK is set to 6.25 MHz.

**Table 266 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	63	70	71	Sec
010	108	109	109	Sec
025	109	107	108	Sec
050	107	Not Supported	Not Supported	Sec
060	100	108	108	Sec
090	176	184	184	Sec
150	183	183	183	Sec

**Table 267 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	109	89	88	Sec
010	183	135	135	Sec
025	251	142	143	Sec
050	134	Not Supported	Not Supported	Sec
060	390	183	180	Sec
090	604	283	282	Sec
150	889	331	332	Sec

## 2.3.21 Clock Conditioning Circuits (CCC)

The following table lists the CCC/PLL specifications in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 282 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**

Parameter	Min	Typ	Max	Unit	Conditions
Clock conditioning circuitry input frequency $F_{IN\_CCC}$	1		200	MHz	All CCC
	0.032		200	MHz	32 kHz capable CCC
Clock conditioning circuitry output frequency $F_{OUT\_CCC}^1$	0.078		400	MHz	
PLL VCO frequency <sup>2</sup>	500		1000	MHz	
Delay increments in programmable delay blocks		75	100	ps	
Number of programmable values in each programmable delay block			64		
Acquisition time		70	100	$\mu\text{s}$	$F_{IN} \geq 1\text{ MHz}$
		1	16	ms	$F_{IN} = 32\text{ kHz}$
Input duty cycle (reference clock)					Internal Feedback
	10		90	%	$1\text{ MHz} \leq F_{IN\_CCC} \leq 25\text{ MHz}$
	25		75	%	$25\text{ MHz} \leq F_{IN\_CCC} \leq 100\text{ MHz}$
	35		65	%	$100\text{ MHz} \leq F_{IN\_CCC} \leq 150\text{ MHz}$
	45		55	%	$150\text{ MHz} \leq F_{IN\_CCC} \leq 200\text{ MHz}$
					External Feedback (CCC, FPGA, Off-chip)
	25		75	%	$1\text{ MHz} \leq F_{IN\_CCC} \leq 25\text{ MHz}$
	35		65	%	$25\text{ MHz} \leq F_{IN\_CCC} \leq 35\text{ MHz}$
	45		55	%	$35\text{ MHz} \leq F_{IN\_CCC} \leq 50\text{ MHz}$
	Output duty cycle	48		52	%
48			52	%	005, 010, and 025 devices $F_{OUT} < 350\text{ MHz}$
46			54	%	005, 010, and 025 devices $350\text{ MHz} \leq F_{out} \leq 400\text{ MHz}$
48			52	%	060 and 090 devices $F_{OUT} \leq 100\text{ MHz}$
44			52	%	060 and 090 devices $100\text{ MHz} \leq F_{OUT} \leq 400\text{ MHz}$
48			52	%	150 devices $F_{OUT} \leq 120\text{ MHz}$
45			52	%	150 devices $120\text{ MHz} \leq F_{OUT} \leq 400\text{ MHz}$
<b>Spread Spectrum Characteristics</b>					
Modulation frequency range	25	35	50	k	
Modulation depth range	0		1.5	%	
Modulation depth control		0.5		%	

**Table 291 • DEVRST\_N to Functional Times for SmartFusion2 (continued)**

Symbol	From	To	Description	Maximum Power-up to Functional Time for SmartFusion2 (uS)						
				005	010	025	050	060	090	150
$T_{DEVRST2POR}$	DEVRST_N	POWER_ON_RESET_N	$V_{DD}$ at its minimum threshold level to fabric	233	289	216	213	237	234	219
$T_{DEVRST2MSSRST}$	DEVRST_N	MSS_RESET_N_M2F	$V_{DD}$ at its minimum threshold level to MSS	702	765	712	688	636	630	866
$T_{DEVRST2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215

**Figure 19 • DEVRST\_N to Functional Timing Diagram for SmartFusion2**

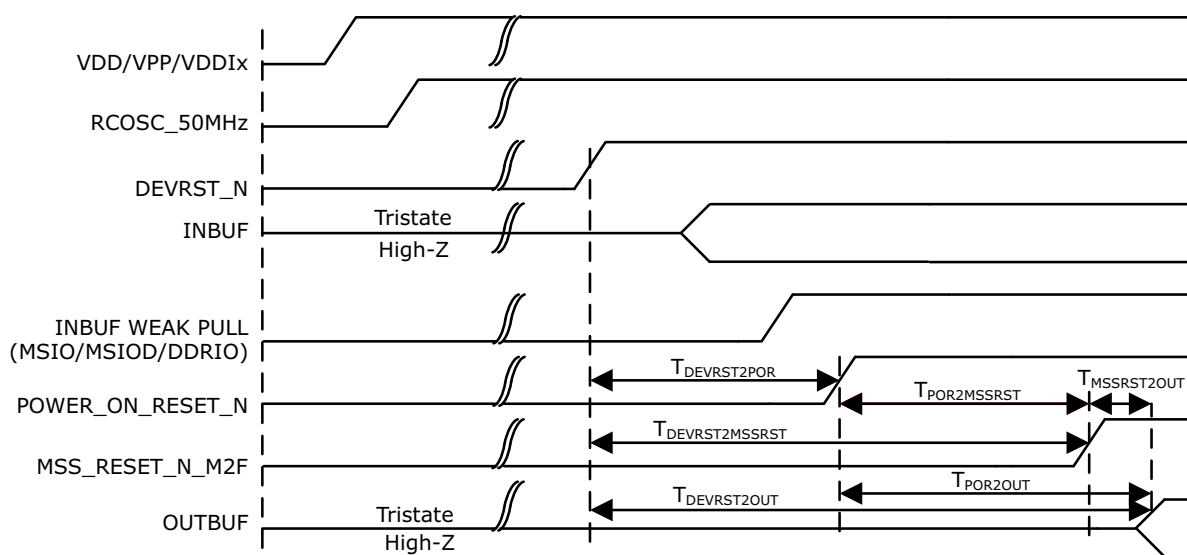
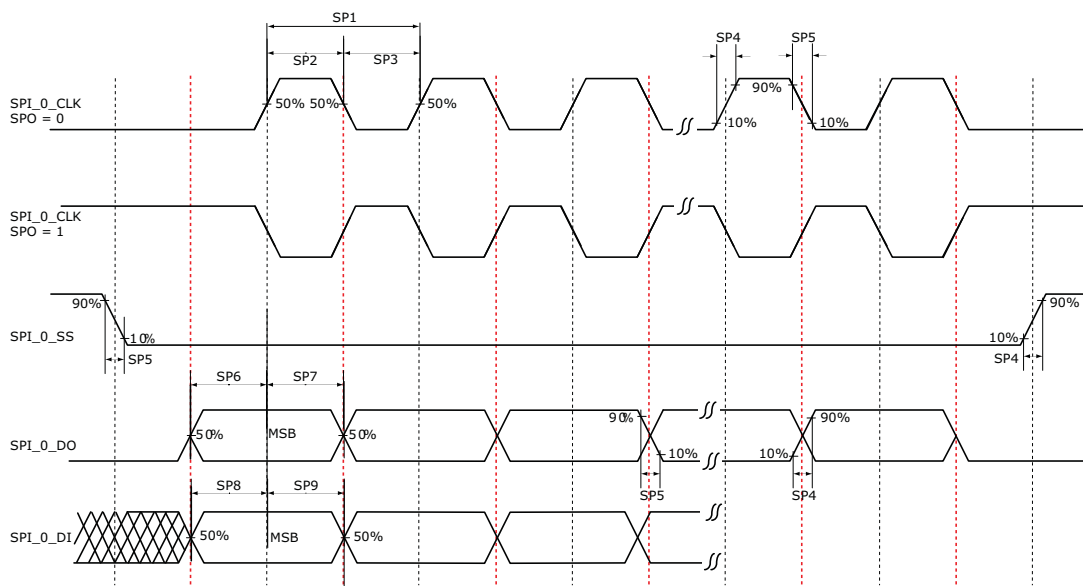


Figure 22 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)



### 2.3.32 CAN Controller Characteristics

The following table lists the CAN controller characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 306 • CAN Controller Characteristics

Parameter	Description	-1	-Std	Unit
FCANREFCLK <sup>1</sup>	Internally sourced CAN reference clock frequency	160	136	MHz
BAUDCANMAX	Maximum CAN performance baud rate	1	1	Mbps
BAUDCANMIN	Minimum CAN performance baud rate	0.05	0.05	Mbps

1. PCLK to CAN controller must be a multiple of 8 MHz.

### 2.3.33 USB Characteristics

The following table lists the USB characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 307 • USB Characteristics

Parameter	Description	-1	-Std	Unit
FUSBREFCLK	Internally sourced USB reference clock frequency	166	142	MHz
TUSBCLK	USB clock period	16.66	16.66	ns
TUSBPD	Clock to USB data propagation delay	9.0	9.0	ns
TUSBSU	Setup time for USB data	6.0	6.0	ns
TUSBHD	Hold time for USB data	0	0	ns