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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 10K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-FPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s010-vf256

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- Updated Table 24, page 22 with minimum and maximum values for input current low and high (SAR 73114 and 80314).
- Added Non-Deterministic Random Bit Generator (NRBG) Characteristics, page 106 (SAR 73114 and 79517).
- Added 060 device in Table 282, page 110 (SAR 79860).
- Added DEVRST_N to Functional Times, page 116 (SAR 73114).
- Added Cryptographic Block Characteristics, page 106 (SAR 73114 and 79516).
- Update Table 296, page 121 with VTX-AMP details (SAR 81756).
- Update note in Table 297, page 122 (SAR 74570 and 80677).
- Update Table 298, page 122 with generic EPCS details (SAR 75307).
- Added Table 308, page 129 (SAR 50424).

1.2 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- The Surge Current on VDD during DEVRST_B Assertion and Surge Current on VDD during Digest Check using System Services tables were deleted and added reference to *AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note*. (SAR 76865 and 76623).
- Added 060 device in Table 4, page 6 (SAR 76383).
- Updated Table 24, page 22 for ramp time input (SAR 72103).
- Added 060 device details in Table 284, page 112 (SAR 74927).
- Updated Table 290, page 116 for name change (SAR 74925).
- Updated Table 283, page 111 for 060 FG676 Package details (SAR 78849).
- Updated Table 305, page 126 for SmartFusion2 and Table 310, page 129 for IGLOO2 for SPI timing and Fmax (SAR 56645, 75331).
- Updated Table 293, page 119 for Flash*Freeze entry and exit times (SAR 75329, 75330).
- Updated Table 297, page 122 for RX-CID information (SAR 78271).
- Added Table 8, page 8 and Figure 1, page 9 (SAR 78932).
- Updated Table 223, page 76 for timing characteristics and Table 224, page 77 (SAR 75998).
- Added SRAM PUF, page 105 (SAR 64406).
- Added a footnote on digest cycle in Table 5, page 7 (SAR 79812).

1.3 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document.

- Added a note in Table 5, page 7 (SAR 71506).
- Added a note in Table 6, page 8 (SAR 74616).
- Added a note in Figure 3, page 17 (SAR 71506).
- Updated Quiescent Supply Current for 060 in Table 11, page 12 and Table 12, page 13 (SAR 74483).
- Updated programming currents for 060 in Table 13, page 13, Table 14, page 13, and Table 15, page 14.
- Added DEVRST_B assertion tables (SAR 74708).
- Updated I/O speeds for LVDS 3.3 V in Table 18, page 19 and Table 21, page 20 (SAR 69829).
- Updated Table 24, page 22 (SAR 69418).
- Updated Table 25, page 22, Table 26, page 23, Table 27, page 23 (SAR 74570).
- Updated all AC/DC table to link to the Input Capacitance, Leakage Current, and Ramp Time, page 22 for reference (SAR 69418).

- Added Table 244, page 94 and Table 256, page 99 (SAR 73971).
- Updated the SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 71171).
- Added the DEVRST_N Characteristics, page 116 (SAR 64100, 72103).
- Added Table 298, page 122 (SAR 71897).
- Updated Table 25, page 22, Table 26, page 23, and Table 27, page 23 (SAR 74570).
- Added 060 devices in Table 277, page 107, Table 278, page 108, and Table 279, page 108 (SAR 57898).
- Updated duty cycle parameter of crystal in Table 280, page 109 and Table 281, page 109 (SAR 57898).
- Added 32 KHz mode PLL acquisition time in Table 282, page 110 (SAR 68281).
- Updated Table 293, page 119 for 060 devices (SAR 57828).
- Updated Table 297, page 122 for CID value (SAR 70878).

1.4 Revision 8.0

The following is a summary of the changes in revision 8.0 of this document.

- Updated Table 11, page 12 (SAR 69218).
- Updated Table 12, page 13 (SAR 69218).
- Updated Table 283, page 111 (SAR 69000).

1.5 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Updated Table 1, page 4(SAR 68620).

1.6 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- Updated Table 5, page 7 (SAR 65949).
- Updated Table 9, page 10 (SAR 62995).
- Updated Table 123, page 47 and Table 133, page 49 (SAR 67210).
- Added Embedded NVM (eNVM) Characteristics, page 104 (SAR 52509).
- Updated Table 277, page 107 (SAR 64855).
- Updated Table 282, page 110 (SAR 65958 and SAR 56666).
- Added DDR Memory Interface Characteristics, page 120 (SAR 66223).
- Added SFP Transceiver Characteristics, page 120 (SAR 63105).
- Updated Table 302, page 123 and Table 309, page 129 (SAR 66314).

1.7 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Updated Table 1, page 4.
- Updated Table 4, page 6 for T_J symbol information.
- Updated Table 5, page 7 (SAR 63109).
- Updated Table 9, page 10.
- Updated Table 282, page 110 (SAR 62012).
- Added Table 290, page 116 (SAR 64100).
- Added Table 306, page 128, Table 307, page 128 (SAR 50424).

1.8 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document.

- Updated Table 1, page 4. Changed the Status of 090 devices to "Production" (SAR 62750).
- Updated Figure 10, page 70. Removed inverter bubble from DDR_IN latch (SAR 61418).
- Updated SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 62836).

2 IGLOO2 FPGA and SmartFusion2 SoC FPGA

Microsemi's mainstream SmartFusion[®]2 SoC and IGLOO[®]2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated math blocks, multiple embedded memory blocks, and high-performance SerDes communication interfaces on a single chip. Both families benefit from low-power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to 5 MBs of embedded RAM, up to 16 SerDes lanes, and up to four PCI Express Gen 2 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 devices integrate an entire low-power, real-time microcontroller subsystem (MSS) with a rich set of industry-standard peripherals including Ethernet, USB, and CAN, while IGLOO2 devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

2.1 Device Status

The following table shows the design security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

Table 1 • IGLOO2 and SmartFusion2 Design Security Densities

Design Security Device Densities	Status
005	Production
010, 010T	Production
025, 025T	Production
050, 050T	Production
060, 060T	Production
090, 090T	Production
150, 150T	Production

The following table shows the data security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

Table 2 • IGLOO2 and SmartFusion2 Data Security Densities

Data Security Device Densities	Status
005S	Production
010TS	Production
025TS	Production
050TS	Production
060TS	Production
090TS	Production
150TS	Production

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIO I/O bank at V_{OH}/V_{OL} Level.

Table 26 • I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank

V_{DDI} Domain	R(WEAK PULL-UP) at V_{OH} (Ω)		R(WEAK PULL-DOWN) at V_{OL} (Ω)	
	Min	Max	Min	Max
3.3 V	9.9K	17.1K	9.98K	17.5K
2.5 V ^{1,2}	10K	17.6K	10.1K	18.4K
1.8 V ^{1,2}	10.4K	19.1K	10.4K	20.4K
1.5 V ^{1,2}	10.7K	20.4K	10.8K	22.2K
1.2 V ^{1,2}	11.3K	23.2K	11.5K	26.7K

1. $R(\text{WEAK PULL-DOWN}) = (V_{OL\text{spec}})/I(\text{WEAK PULL-DOWN MAX})$.
2. $R(\text{WEAK PULL-UP}) = (V_{DDI\text{max}} - V_{OH\text{spec}})/I(\text{WEAK PULL-UP MIN})$.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIOD I/O bank at V_{OH}/V_{OL} Level.

Table 27 • I/O Weak Pull-up/Pull-down Resistances for MSIOD I/O Bank

V_{DDI} Domain	R(WEAK PULL-UP) at V_{OH} (Ω)		R(WEAK PULL-DOWN) at V_{OL} (Ω)	
	Min	Max	Min	Max
2.5 V ^{1,2}	9.6K	16.6K	9.5K	16.4K
1.8 V ^{1,2}	9.7K	17.3K	9.7K	17.1K
1.5 V ^{1,2}	9.9K	18K	9.8K	17.6K
1.2 V ^{1,2}	10.3K	19.6K	10K	19.1K

1. $R(\text{WEAK PULL-DOWN}) = (V_{OL\text{spec}})/I(\text{WEAK PULL-DOWN MAX})$.
2. $R(\text{WEAK PULL-UP}) = (V_{DDI\text{max}} - V_{OH\text{spec}})/I(\text{WEAK PULL-UP MIN})$.

The following table lists the hysteresis voltage value for schmitt trigger mode input buffers.

Table 28 • Schmitt Trigger Input Hysteresis

Input Buffer Configuration	Hysteresis Value (Typical, unless otherwise noted)
3.3 V LVTTTL/LVCMOS/ PCI/PCI-X	$0.05 \times V_{DDI}$ (worst-case)
2.5 V LVCMOS	$0.05 \times V_{DDI}$ (worst-case)
1.8 V LVCMOS	$0.1 \times V_{DDI}$ (worst-case)
1.5 V LVCMOS	60 mV
1.2 V LVCMOS	20 mV

2.3.5.6 Single-Ended I/O Standards

2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 29 • LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

Table 30 • LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DC input logic high	V_{IH} (DC)	2.0	3.45	V
DC input logic low	V_{IL} (DC)	-0.3	0.8	V
Input current high ¹	I_{IH} (DC)			
Input current low ¹	I_{IL} (DC)			

1. See Table 24, page 22.

Table 31 • LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DC output logic high ¹	V_{OH}	$V_{DDI} - 0.4$		V
DC output logic low ¹	V_{OL}		0.4	V

1. The V_{OH}/V_{OL} test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

Table 32 • LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	2.4		V
DC output logic low	V_{OL}		0.4	V

Table 33 • LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	600	Mbps	AC loading: 17 pF load, maximum drive/slew

2.3.5.7 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs that are in compliance with the JEDEC specification JESD8-5A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 38 • LVCMOS 2.5 V DC Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V

Table 39 • LVCMOS 2.5 V DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	V_{IH} (DC)	1.7	2.625	V
DC input logic high (for MSIO I/O bank)	V_{IH} (DC)	1.7	3.45	V
DC input logic low	V_{IL} (DC)	-0.3	0.7	V
Input current high ¹	I_{IH} (DC)			
Input current low ¹	I_{IL} (DC)			

1. See Table 24, page 22.

Table 40 • LVCMOS 2.5 V DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH} ¹	$V_{DDI} - 0.4$	-	V
DC output logic low	V_{OL} ²		0.4	V

1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

Table 41 • LVCMOS 2.5 V AC Minimum and Maximum Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	400	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D_{MAX}	410	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	420	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 42 • LVCMOS 2.5 V AC Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	Rodt_cal	75, 60, 50, 33, 25, 20	Ω

Table 58 • LVCMOS 1.8 V Transmitter Characteristics for MSIO I/O Bank

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.441	4.047	4.165	4.9	4.413	5.192	4.891	5.755	5.138	6.044	ns
4 mA	Slow	3.218	3.786	3.642	4.284	3.941	4.636	5.665	6.665	5.568	6.551	ns
6 mA	Slow	3.141	3.694	3.501	4.118	3.823	4.498	6.587	7.75	6.032	7.096	ns
8 mA	Slow	3.165	3.723	3.319	3.904	3.654	4.298	6.898	8.115	6.216	7.313	ns
10 mA	Slow	3.202	3.767	3.278	3.857	3.616	4.254	7.25	8.529	6.435	7.571	ns
12 mA	Slow	3.277	3.855	3.175	3.736	3.519	4.139	7.392	8.697	6.538	7.692	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 59 • LVCMOS 1.8 V Transmitter Characteristics for MSIOD I/O Bank

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	2.725	3.206	3.316	3.901	3.484	4.099	5.204	6.123	4.997	5.88	ns
4 mA	Slow	2.242	2.638	2.777	3.267	2.947	3.466	5.729	6.74	5.448	6.41	ns
6 mA	Slow	1.995	2.347	2.466	2.901	2.63	3.094	6.372	7.496	5.987	7.043	ns
8 mA	Slow	2.001	2.354	2.44	2.87	2.6	3.058	6.633	7.804	6.193	7.286	ns
10 mA	Slow	2.025	2.382	2.312	2.719	2.47	2.906	6.94	8.165	6.412	7.544	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

2.3.5.9 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 60 • LVCMOS 1.5 V DC Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{DDI}	1.425	1.5	1.575	V

Table 61 • LVCMOS 1.5 V DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input logic high for (MSIOD and DDRIO I/O banks)	V _{IH} (DC)	0.65 × V _{DDI}	1.575	V
DC input logic high (for MSIO I/O bank)	V _{IH} (DC)	0.65 × V _{DDI}	3.45	V
DC input logic low	V _{IL} (DC)	-0.3	0.35 × V _{DDI}	V
Input current high ¹	I _{IH} (DC)			-
Input current low ¹	I _{IL} (DC)			-

1. See Table 24, page 22.

Table 128 • DDR2/SSTL18 Transmitter Characteristics (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
SSTL18 Class I (for DDRIO I/O Bank)											
Single-ended	2.383	2.804	2.23	2.623	2.229	2.622	2.202	2.591	2.201	2.59	ns
Differential	2.413	2.84	2.797	3.29	2.797	3.29	2.282	2.685	2.282	2.685	ns
SSTL18 Class II (for DDRIO I/O Bank)											
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.171	2.555	2.17	2.554	ns
Differential	2.315	2.724	2.698	3.173	2.698	3.173	2.242	2.639	2.242	2.639	ns

2.3.6.5 Stub-Series Terminated Logic 1.5 V (SSTL15)

SSTL15 Class I and Class II are supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR3) standard. IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

The following table lists the SSTL15 DC voltage specifications for DDRIO bank.

Table 129 • SSTL15 DC Recommended DC Operating Conditions (for DDRIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.425	1.5	1.575	V
Termination voltage	V_{TT}	0.698	0.750	0.803	V
Input reference voltage	V_{REF}	0.698	0.750	0.803	V

Table 130 • SSTL15 DC Input Voltage Specification (for DDRIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}(DC)$	$V_{REF} + 0.1$	1.575	V
DC input logic low	$V_{IL}(DC)$	-0.3	$V_{REF} - 0.1$	V
Input current high ¹	$I_{IH}(DC)$			
Input current low ¹	$I_{IL}(DC)$			

1. See Table 24, page 22.

2.3.6.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 139 • LPDDR DC Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max
Supply voltage	V_{DDI}	1.71	1.8	1.89
Termination voltage	V_{TT}	0.838	0.900	0.964
Input reference voltage	V_{REF}	0.838	0.900	0.964

Table 140 • LPDDR DC Input Voltage Specification

Parameter	Symbol	Min	Max
DC input logic high	V_{IH} (DC)	$0.7 \times V_{DDI}$	1.89
DC input logic low	V_{IL} (DC)	-0.3	$0.3 \times V_{DDI}$
Input current high ¹	I_{IH} (DC)		
Input current low ¹	I_{IL} (DC)		

1. See Table 24, page 22.

Table 141 • LPDDR DC Output Voltage Specification Reduced Drive

Parameter	Symbol	Min	Max
DC output logic high	V_{OH}	$0.9 \times V_{DDI}$	
DC output logic low	V_{OL}		$0.1 \times V_{DDI}$
Output minimum source DC current	I_{OH} at V_{OH}	0.1	
Output minimum sink current	I_{OL} at V_{OL}	-0.1	

Table 142 • LPDDR DC Output Voltage Specification Full Drive¹

Parameter	Symbol	Min	Max
DC output logic high	V_{OH}	$0.9 \times V_{DDI}$	
DC output logic low	V_{OL}		$0.1 \times V_{DDI}$
Output minimum source DC current	I_{OH} at V_{OH}	0.1	
Output minimum sink current	I_{OL} at V_{OL}	-0.1	

1. To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.

Table 143 • LPDDR DC Differential Voltage Specification

Parameter	Symbol	Min
DC input differential voltage	V_{ID} (DC)	$0.4 \times V_{DDI}$

Table 144 • LPDDR AC Differential Voltage Specifications (for DDRIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF}	$0.6 \times V_{DDI}$		V
AC differential cross point voltage	V_x	$0.4 \times V_{DDI}$	$0.6 \times V_{DDI}$	V

Table 145 • LPDDR AC Specifications (for DDRIO I/O Bank Only)

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	400	Mbps	AC loading: per JEDEC specifications

Table 146 • LPDDR AC Calibrated Impedance Option (for DDRIO I/O Bank Only)

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	R_{REF}	20, 42	Ω	Reference resistor = 150 Ω
Effective impedance value (ODT)	R_{TT}	50, 70, 150	Ω	Reference resistor = 150 Ω

Table 147 • LPDDR AC Test Parameter Specifications (for DDRIO I/O Bank Only)

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.9	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for LPDDR (T_{DP})	R_{TT_TEST}	50	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	Ω

AC Switching Characteristics

Worst-case commercial conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, worst-case V_{DDI} .

Table 148 • LPDDR Receiver Characteristics for DDRIO I/O Bank with Fixed Codes

	On-Die Termination (ODT)	T_{PY}		Unit
		-1	-Std	
Pseudo differential	None	1.568	1.845	ns
True differential	None	1.588	1.869	ns

Table 149 • LPDDR Reduced Drive for DDRIO I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ENZL}		T_{ENZH}		T_{ENHZ}		T_{ENLZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.383	2.804	2.23	2.623	2.229	2.622	2.202	2.591	2.201	2.59	ns
Differential	2.396	2.819	2.764	3.252	2.764	3.252	2.255	2.653	2.255	2.653	ns

Table 185 • M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 186 • M-LVDS Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	V_{OD}	300	650	mV
Output common mode voltage (for MSIO I/O bank only)	V_{OCM}	0.3	2.1	V
Input common mode voltage	V_{ICM}	0.3	1.2	V
Input differential voltage	V_{ID}	50	2400	mV

Table 187 • M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	500	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 188 • M-LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	50	Ω

Table 189 • M-LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 190 • M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.738	3.221	ns
100	2.735	3.218	ns

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 8K × 2 in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 234 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register				0.32	0.377	ns
Read access time without pipeline register	T_{CLK2Q}			2.272	2.673	ns
Access time with feed-through write timing				1.511	1.778	ns
Address setup time	T_{ADDRSU}	0.612		0.72		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.33		0.388		ns
Data hold time	T_{DHD}	0.082		0.096		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}			1.511	1.778	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.529		0.622		ns
Read enable hold time	T_{RDEHD}	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}			1.528	1.797	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.488		0.574		ns
Write enable hold time	T_{WEHD}	0.048		0.057		ns
Maximum frequency	F_{MAX}			400	340	MHz

2.3.12.2 FPGA Fabric Micro SRAM (μ SRAM)

The following table lists the μ SRAM in 64×18 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 237 • μ SRAM (RAM64x18) in 64×18 Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register				1.677		1.973
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode			1.856		2.184	
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode			-0.778		-0.915	
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)			0.046		0.054	
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)			0.236		0.278	
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.839		0.987	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns

The following table lists the programming times in worst-case conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 256 • JTAG Programming (Fabric Only)

M2S/M2GL Device	Image size		Verify	Unit
	Bytes	Program		
005	302672	44	10	Sec
010	568784	50	18	Sec
025	1223504	73	26	Sec
050	2424832	88	54	Sec
060	2418896	99	54	Sec
090	3645968	135	126	Sec
150	6139184	177	193	Sec

Table 257 • JTAG Programming (eNVM Only)

M2S/M2GL Device	Image size		Verify	Unit
	Bytes	Program		
005	137536	61	4	Sec
010	274816	100	9	Sec
025	274816	100	9	Sec
050	2,78,528	106	8	Sec
060	268480	98	8	Sec
090	544496	176	15	Sec
150	544496	177	15	Sec

Table 258 • JTAG Programming (Fabric and eNVM)

M2S/M2GL Device	Image size		Verify	Unit
	Bytes	Program		
005	439296	71	11	Sec
010	842688	129	20	Sec
025	1497408	142	35	Sec
050	2695168	184	59	Sec
060	2686464	180	70	Sec
090	4190208	288	147	Sec
150	6682768	338	231	Sec

2.3.17 Non-Deterministic Random Bit Generator (NRBG) Characteristics

For more information about NRBG, see *AC407: Using NRBG Services in SmartFusion2 and IGLOO2 Devices Application Note*. The following table lists the NRBG in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 275 • Non-Deterministic Random Bit Generator (NRBG)

Service	Timing	Unit	Conditions	
			Prediction Resistance	Additional Input
Instantiate	85	ms	OFF	X
Generate (after Instantiate) ¹	4.5 ms + (6.25 us/byte x No. of Bytes)		OFF	0
	6.0 ms + (6.25 us/byte x No. of Bytes)		OFF	64
	7.0 ms + (6.25 us/byte x No. of Bytes)		OFF	128
Generate (after Instantiate)	47	ms	ON	X
Generate (subsequent) ¹	0.5 ms + (6.25 us/byte x No. of Bytes)		OFF	0
	2.0 ms + (6.25 us/byte x No. of Bytes)		OFF	64
	3.0 ms + (6.25 us/byte x No. of Bytes)		OFF	128
Generate (subsequent)	43	ms	ON	X
Reseed	40	ms		
Uninstantiate	0.16	ms		
Reset	0.10	ms		
Self test	20	ms	First time after power-up	
	6	ms	Subsequent	

1. If PUF_OFF, generate will incur additional PUF delay time for consecutive service calls.

2.3.18 Cryptographic Block Characteristics

For more information about cryptographic block and associated services, see *AC410: Using AES System Services in SmartFusion2 and IGLOO2 Devices Application Note* and *AC432: Using SHA-256 System Services in SmartFusion2 and IGLOO2 Devices Application Note*.

The following table lists the cryptographic block characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 276 • Cryptographic Block Characteristics

Service	Conditions	Timing	Unit
Any service	First certificate check penalty at boot	11.5	ms
AES128/256 (encoding / decoding) ¹	100 blocks up to 64k blocks	700	kbps

2.3.21 Clock Conditioning Circuits (CCC)

The following table lists the CCC/PLL specifications in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 282 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification

Parameter	Min	Typ	Max	Unit	Conditions
Clock conditioning circuitry input frequency F_{IN_CCC}	1		200	MHz	All CCC
	0.032		200	MHz	32 kHz capable CCC
Clock conditioning circuitry output frequency $F_{OUT_CCC}^1$	0.078		400	MHz	
PLL VCO frequency ²	500		1000	MHz	
Delay increments in programmable delay blocks		75	100	ps	
Number of programmable values in each programmable delay block			64		
Acquisition time		70	100	μs	$F_{IN} \geq 1\text{ MHz}$
		1	16	ms	$F_{IN} = 32\text{ kHz}$
Input duty cycle (reference clock)					Internal Feedback
	10		90	%	$1\text{ MHz} \leq F_{IN_CCC} \leq 25\text{ MHz}$
	25		75	%	$25\text{ MHz} \leq F_{IN_CCC} \leq 100\text{ MHz}$
	35		65	%	$100\text{ MHz} \leq F_{IN_CCC} \leq 150\text{ MHz}$
	45		55	%	$150\text{ MHz} \leq F_{IN_CCC} \leq 200\text{ MHz}$
					External Feedback (CCC, FPGA, Off-chip)
	25		75	%	$1\text{ MHz} \leq F_{IN_CCC} \leq 25\text{ MHz}$
	35		65	%	$25\text{ MHz} \leq F_{IN_CCC} \leq 35\text{ MHz}$
	45		55	%	$35\text{ MHz} \leq F_{IN_CCC} \leq 50\text{ MHz}$
	Output duty cycle	48		52	%
48			52	%	005, 010, and 025 devices $F_{OUT} < 350\text{ MHz}$
46			54	%	005, 010, and 025 devices $350\text{ MHz} \leq F_{out} \leq 400\text{ MHz}$
48			52	%	060 and 090 devices $F_{OUT} \leq 100\text{ MHz}$
44			52	%	060 and 090 devices $100\text{ MHz} \leq F_{OUT} \leq 400\text{ MHz}$
48			52	%	150 devices $F_{OUT} \leq 120\text{ MHz}$
45			52	%	150 devices $120\text{ MHz} \leq F_{OUT} \leq 400\text{ MHz}$
Spread Spectrum Characteristics					
Modulation frequency range	25	35	50	k	
Modulation depth range	0		1.5	%	
Modulation depth control		0.5		%	

2.3.22 JTAG

Table 284 • JTAG 1532 for 005, 010, 025, and 050 Devices

Parameter	Symbol	005		010		025		050		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Clock to Q (data out)	T_{TCK2Q}	7.47	8.79	7.73	9.09	7.75	9.12	7.89	9.28	ns
Reset to Q (data out)	T_{RSTB2Q}	7.65	9	6.43	7.56	6.13	7.21	7.40	8.70	ns
Test data input setup time	T_{DISU}	-1.05	-0.89	-0.69	-0.59	-0.67	-0.57	-0.30	-0.25	ns
Test data input hold time	T_{DIHD}	2.38	2.8	2.38	2.8	2.42	2.85	2.09	2.45	ns
Test mode select setup time	T_{TMSSU}	-0.73	-0.62	-1.03	-1.21	-1.1	-0.94	0.28	0.33	ns
Test mode select hold time	T_{TMDHD}	1.36	1.6	1.43	1.68	1.93	2.27	0.16	0.19	ns
ResetB removal time	$T_{TRSTREM}$	-0.77	-0.65	-1.08	-0.92	-1.33	-1.13	-0.45	-0.38	ns
ResetB recovery time	$T_{TRSTREC}$	-0.76	-0.65	-1.07	-0.91	-1.34	-1.14	-0.45	-0.38	ns
TCK maximum frequency	F_{TCKMAX}	25	21.25	25	21.25	25	21.25	25.00	21.25	MHz

Table 285 • JTAG 1532 for 060, 090, and 150 Devices

Parameter	Symbol	060		090		150		Unit
		-1	-Std	-1	-Std	-1	-Std	
Clock to Q (data out)	T_{TCK2Q}	8.38	9.86	8.96	10.54	8.66	10.19	ns
Reset to Q (data out)	T_{RSTB2Q}	8.54	10.04	7.75	9.12	8.79	10.34	ns
Test data input setup time	T_{DISU}	-1.18	-1	-1.31	-1.11	-0.96	-0.82	ns
Test data input hold time	T_{DIHD}	2.52	2.97	2.68	3.15	2.57	3.02	ns
Test mode select setup time	T_{TMSSU}	-0.97	-0.83	-1.02	-0.87	-0.53	-0.45	ns
Test mode select hold time	T_{TMDHD}	1.7	2	1.67	1.96	1.02	1.2	ns
ResetB removal time	$T_{TRSTREM}$	-1.21	-1.03	-0.76	-0.65	-1.03	-0.88	ns
ResetB recovery time	$T_{TRSTREC}$	-1.21	-1.03	-0.77	-0.65	-1.03	-0.88	ns
TCK maximum frequency	F_{TCKMAX}	25	21.25	25	21.25	25	21.25	MHz

2.3.23 System Controller SPI Characteristics

The following table lists the system controller characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 286 • System Controller SPI Characteristics for All Devices

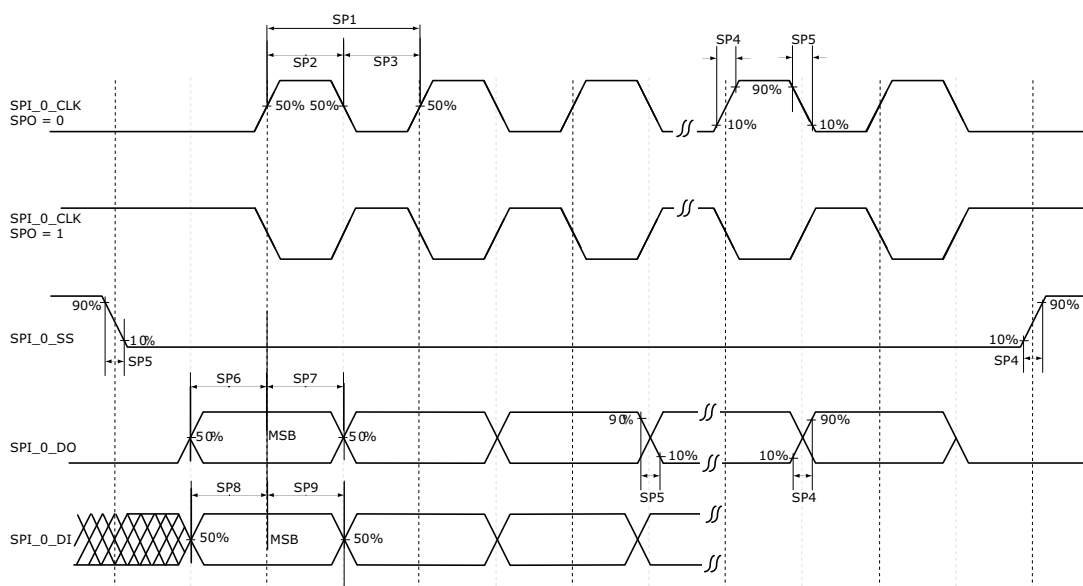
Symbol	Description	Conditions	Min	Typ	Unit
sp1	SC_SPI_SCK minimum period		20		ns
sp2	SC_SPI_SCK minimum pulse width high		10		ns
sp3	SC_SPI_SCK minimum pulse width low		10		ns
sp4 ¹	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%–90%) 1	I/O configuration: LVTTTL 3.3 V– 20 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C		1.239	ns
sp5 ¹	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%–90%) 1	I/O configuration: LVTTTL 3.3 V– 20 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C		1.245	ns
sp6	Data from master (SC_SPI_SDO) setup time		160		ns
sp7	Data from master (SC_SPI_SDO) hold time		160		ns
sp8	SC_SPI_SDI setup time		20		ns
sp9	SC_SPI_SDI hold time		20		ns

1. For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>. Use the supported I/O Configurations for the System Controller SPI in the following table.

Table 287 • Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)

Voltage Supply	I/O Drive Configuration	Unit
3.3 V	20	mA
2.5 V	16	mA
1.8 V	12	mA
1.5 V	8	mA
1.2 V	4	mA

Figure 22 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)



2.3.32 CAN Controller Characteristics

The following table lists the CAN controller characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 306 • CAN Controller Characteristics

Parameter	Description	-1	-Std	Unit
FCANREFCLK ¹	Internally sourced CAN reference clock frequency	160	136	MHz
BAUDCANMAX	Maximum CAN performance baud rate	1	1	Mbps
BAUDCANMIN	Minimum CAN performance baud rate	0.05	0.05	Mbps

1. PCLK to CAN controller must be a multiple of 8 MHz.

2.3.33 USB Characteristics

The following table lists the USB characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 307 • USB Characteristics

Parameter	Description	-1	-Std	Unit
FUSBREFCLK	Internally sourced USB reference clock frequency	166	142	MHz
TUSBCLK	USB clock period	16.66	16.66	ns
TUSBPD	Clock to USB data propagation delay	9.0	9.0	ns
TUSBSU	Setup time for USB data	6.0	6.0	ns
TUSBHD	Hold time for USB data	0	0	ns