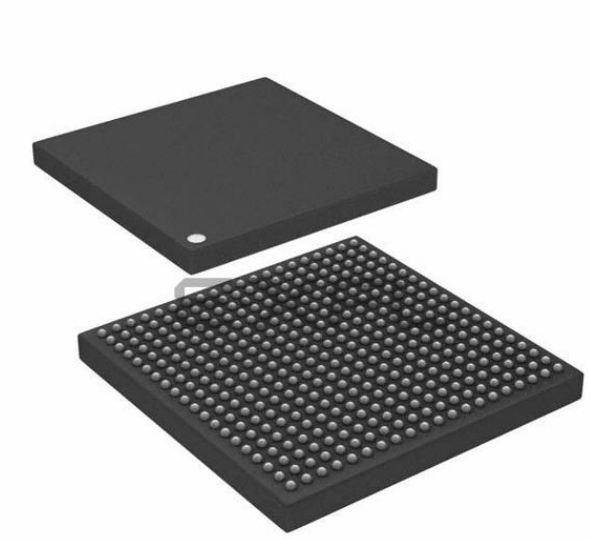

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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | ARM® Cortex®-M3 |
| Flash Size | 256KB |
| RAM Size | 64KB |
| Peripherals | DDR, PCIe, SERDES |
| Connectivity | CANbus, Ethernet, I²C, SPI, UART/USART, USB |
| Speed | 166MHz |
| Primary Attributes | FPGA - 10K Logic Modules |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 400-LFBGA |
| Supplier Device Package | 400-VFBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2s010-vfg400i |

- Added Table 244, page 94 and Table 256, page 99 (SAR 73971).
- Updated the SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 71171).
- Added the DEVRST_N Characteristics, page 116 (SAR 64100, 72103).
- Added Table 298, page 122 (SAR 71897).
- Updated Table 25, page 22, Table 26, page 23, and Table 27, page 23 (SAR 74570).
- Added 060 devices in Table 277, page 107, Table 278, page 108, and Table 279, page 108 (SAR 57898).
- Updated duty cycle parameter of crystal in Table 280, page 109 and Table 281, page 109 (SAR 57898).
- Added 32 KHz mode PLL acquisition time in Table 282, page 110 (SAR 68281).
- Updated Table 293, page 119 for 060 devices (SAR 57828).
- Updated Table 297, page 122 for CID value (SAR 70878).

## 1.4 Revision 8.0

The following is a summary of the changes in revision 8.0 of this document.

- Updated Table 11, page 12 (SAR 69218).
- Updated Table 12, page 13 (SAR 69218).
- Updated Table 283, page 111 (SAR 69000).

## 1.5 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Updated Table 1, page 4(SAR 68620).

## 1.6 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- Updated Table 5, page 7 (SAR 65949).
- Updated Table 9, page 10 (SAR 62995).
- Updated Table 123, page 47 and Table 133, page 49 (SAR 67210).
- Added Embedded NVM (eNVM) Characteristics, page 104 (SAR 52509).
- Updated Table 277, page 107 (SAR 64855).
- Updated Table 282, page 110 (SAR 65958 and SAR 56666).
- Added DDR Memory Interface Characteristics, page 120 (SAR 66223).
- Added SFP Transceiver Characteristics, page 120 (SAR 63105).
- Updated Table 302, page 123 and Table 309, page 129 (SAR 66314).

## 1.7 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Updated Table 1, page 4.
- Updated Table 4, page 6 for $T_J$ symbol information.
- Updated Table 5, page 7 (SAR 63109).
- Updated Table 9, page 10.
- Updated Table 282, page 110 (SAR 62012).
- Added Table 290, page 116 (SAR 64100).
- Added Table 306, page 128, Table 307, page 128 (SAR 50424).

## 1.8 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document.

- Updated Table 1, page 4. Changed the Status of 090 devices to "Production" (SAR 62750).
- Updated Figure 10, page 70. Removed inverter bubble from DDR_IN latch (SAR 61418).
- Updated SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 62836).

## 1.9 Revision 3.0

In revision 3.0 of this document, the Theta B/C columns and FCS325 package was updated. For more information, see Table 9, page 10 (SAR 62002).

## 1.10 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Table 1, page 4 was updated (SAR 59056).
- Table 7, page 8 temperature and data retention information was updated SAR (61363).
- Storage Operating Table was updated and split into three tables – Table 5, page 7, Table 7, page 8 (SAR 58725).
- Updated Theta B/C columns and FCS325 package in Table 9, page 10 (SAR 62002).
- Added 090-FCS325 thermal resistance to Table 9, page 10 (SAR 59384).
- TQ144 package was added to Table 9, page 10 (SAR 57708).
- Added PLL jitter data for the VF400 package (SAR 53162).
- Added Additional Worst Case IDD to Table 11, page 12 and Table 12, page 13 (SAR 59077).
- Table 13, page 13, Table 14, page 13, and Table 15, page 14 were added to verify Inrush currents (SAR 56348).
- Table 18, page 19 and Table 21, page 20 – I/O speeds were replaced.
- Max speed was changed in Table 41, page 26 (SAR 57221) and in Table 52, page 29 (SAR 57113).
- Minimum and Maximum DC/AC Input and Output Levels Specification, page 29 and Table 49, page 29–Table 57, page 31 were added.
- Added Cload to Table 89, page 39 (SAR 56238).
- Removed "Rs" information in DDR Timing Measurement Table 123, page 47, Table 133, page 49, and Table 144, page 52.
- Updated drive programming for M/B-LVDS outputs (SAR 58154).
- Added an inverter bubble to DDR_IN latch in Figure 10, page 70 (SAR 61418).
- QF waveform in Figure 11, page 71 was updated (SAR 59816).
- uSRAM Write Clock minimum values were updated in Table 237, page 86–Table 243, page 93 (SAR 55236).
- Fixed typo in the 32 kHz Crystal (XTAL) oscillator accuracy data section (SAR 59669).
- The "On-Chip Oscillator" section was split, and the Embedded NVM (eNVM) Characteristics, page 104 was added. Table 277, page 107–Table 281, page 109 were revised.(SARs 57898 and 59669).
- PLL VCP Frequency and conditions were added to Table 282, page 110 (SAR 57416).
- Fixed typo for PLL jitter data in the 100-400 MHz range (SAR 60727).
- Updated FCCC information in Table 282, page 110 and Table 283, page 111 (SAR 60799).
- Device 025 specifications were added to Table 283, page 111 (SAR 51625).
- JTAG Table 284, page 112 was replaced (SAR 51188).
- Flash*Freeze Table 293, page 119 was replaced (SAR 57828).
- Added support for HCSL I/O Standard for SERDES reference clocks in Table 300, page 123 and Table 301, page 123 (SAR 50748).
- Tir and Tif parameters were added to Table 303, page 124 (SAR 52203).
- Speed grade consistency was fixed in tables throughout the datasheet (SAR 50722).
- Added jitter attenuation information (SAR 59405).

## 1.11 Revision 1.0

The following is a summary of the changes in revision 1.0 of this document.

- The IGLOO2 v2 and the SmartFusion2 v5 datasheets are combined into this single product family datasheet.

***Figure 1 •*** **High Temperature Data Retention (HTR)**

### 2.3.1.1 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to –1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to $V_{CCI}$ + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

**Note:** The above specifications do not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant with the PCI standard including the PCI overshoot/undershoot specifications.

### 2.3.1.2 Thermal Characteristics

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ1 through EQ3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

*EQ 1*

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

*EQ 2*

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

*EQ 3*

## 2.3.5 User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the I/Os section of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

### 2.3.5.1 Input Buffer and AC Loading

The following figure shows the input buffer and AC loading.

***Figure 3 •*** **Input Buffer AC Loading**

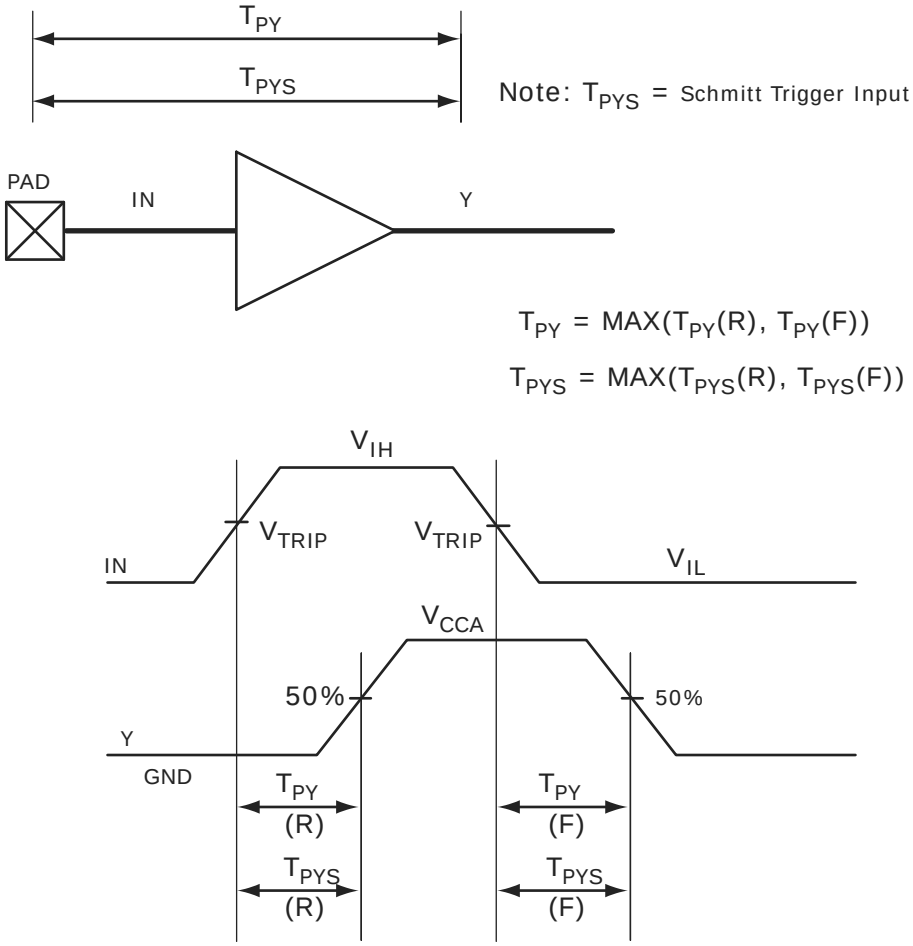


***Table 19 •*** **Maximum Data Rate Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---|---|---|---|---|
| LPDDR | | | 400 | Mbps |
| HSTL1.5 V | | | 400 | Mbps |
| SSTL 2.5 V | 510 | 700 | 400 | Mbps |
| SSTL 1.8 V | | | 667 | Mbps |
| SSTL 1.5 V | | | 667 | Mbps |

***Table 20 •*** **Maximum Data Rate Summary Table for Differential I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | Unit |
|---|---|---|---|
| LVPECL (input only) | 900 | | Mbps |
| LVDS 3.3 V | 535 | | Mbps |
| LVDS 2.5 V | 535 | 700 | Mbps |
| RSDS | 520 | 700 | Mbps |
| BLVDS | 500 | | Mbps |
| MLVDS | 500 | | Mbps |
| Mini-LVDS | 520 | 700 | Mbps |

***Table 21 •*** **Maximum Frequency Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---|---|---|---|---|
| PCI 3.3 V | 315 | | | MHz |
| LVTTL 3.3 V | 300 | | | MHz |
| LVCMOS 3.3 V | 300 | | | MHz |
| LVCMOS 2.5 V | 205 | 210 | 200 | MHz |
| LVCMOS 1.8 V | 147.5 | 200 | 200 | MHz |
| LVCMOS 1.5 V | 80 | 110 | 118 | MHz |
| LVCMOS 1.2 V | 60 | 80 | 100 | MHz |
| LPDDR– LVCMOS 1.8 V mode | | | 200 | MHz |

### 2.3.5.6 Single-Ended I/O Standards

#### 2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

#### 2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 29 •*** **LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 3.15 | 3.3 | 3.45 | V |

***Table 30 •*** **LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | 2.0 | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.8 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 31 •*** **LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high[1] | $V_{OH}$ | $V_{DDI}$ – 0.4 | | V |
| DC output logic low[1] | $V_{OL}$ | | 0.4 | V |

1. The $V_{OH}/V_{OL}$ test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

***Table 32 •*** **LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 2.4 | | V |
| DC output logic low | $V_{OL}$ | | 0.4 | V |

***Table 33 •*** **LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 600 | Mbps | AC loading: 17 pF load, maximum drive/slew |

***Table 128 •*** **DDR2/SSTL18 Transmitter Characteristics (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| **SSTL18 Class I (for DDRIO I/O Bank)** | | | | | | | | | | | |
| Single-ended | 2.383 | 2.804 | 2.23 | 2.623 | 2.229 | 2.622 | 2.202 | 2.591 | 2.201 | 2.59 | ns |
| Differential | 2.413 | 2.84 | 2.797 | 3.29 | 2.797 | 3.29 | 2.282 | 2.685 | 2.282 | 2.685 | ns |
| **SSTL18 Class II (for DDRIO I/O Bank)** | | | | | | | | | | | |
| Single-ended | 2.281 | 2.683 | 2.196 | 2.584 | 2.195 | 2.583 | 2.171 | 2.555 | 2.17 | 2.554 | ns |
| Differential | 2.315 | 2.724 | 2.698 | 3.173 | 2.698 | 3.173 | 2.242 | 2.639 | 2.242 | 2.639 | ns |

### *2.3.6.5 Stub-Series Terminated Logic 1.5 V (SSTL15)*

SSTL15 Class I and Class II are supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR3) standard. IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

The following table lists the SSTL15 DC voltage specifications for DDRIO bank.

***Table 129 •*** **SSTL15 DC Recommended DC Operating Conditions (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.425 | 1.5 | 1.575 | V |
| Termination voltage | $V_{TT}$ | 0.698 | 0.750 | 0.803 | V |
| Input reference voltage | $V_{REF}$ | 0.698 | 0.750 | 0.803 | V |

***Table 130 •*** **SSTL15 DC Input Voltage Specification (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high | $V_{IH}(DC)$ | $V_{REF}$ + 0.1 | 1.575 | V |
| DC input logic low | $V_{IL}(DC)$ | –0.3 | $V_{REF}$ – 0.1 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

### 2.3.6.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 139 •*** **LPDDR DC Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max |
|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.71 | 1.8 | 1.89 |
| Termination voltage | $V_{TT}$ | 0.838 | 0.900 | 0.964 |
| Input reference voltage | $V_{REF}$ | 0.838 | 0.900 | 0.964 |

***Table 140 •*** **LPDDR DC Input Voltage Specification**

| Parameter | Symbol | Min | Max |
|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | 0.7 × $V_{DDI}$ | 1.89 |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.3 × $V_{DDI}$ |
| Input current high[1] | $I_{IH}$ (DC) | | |
| Input current low[1] | $I_{IL}$ (DC) | | |

1. See Table 24, page 22.

***Table 141 •*** **LPDDR DC Output Voltage Specification Reduced Drive**

| Parameter | Symbol | Min | Max |
|---|---|---|---|
| DC output logic high | $V_{OH}$ | 0.9 × $V_{DDI}$ | |
| DC output logic low | $V_{OL}$ | | 0.1 × $V_{DDI}$ |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 0.1 | |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –0.1 | |

***Table 142 •*** **LPDDR DC Output Voltage Specification Full Drive[1]**

| Parameter | Symbol | Min | Max |
|---|---|---|---|
| DC output logic high | $V_{OH}$ | 0.9 × $V_{DDI}$ | |
| DC output logic low | $V_{OL}$ | | 0.1 × $V_{DDI}$ |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 0.1 | |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –0.1 | |

1. To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.

***Table 143 •*** **LPDDR DC Differential Voltage Specification**

| Parameter | Symbol | Min |
|---|---|---|
| DC input differential voltage | $V_{ID}$ (DC) | 0.4 × $V_{DDI}$ |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V.

***Table 180 •*** **B-LVDS AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.738 | 3.221 | ns |
| 100 | 2.735 | 3.218 | ns |

***Table 181 •*** **B-LVDS AC Switching Characteristics for Receiver for MSIOD I/O Bank (Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.495 | 2.934 | ns |
| 100 | 2.495 | 2.935 | ns |

***Table 182 •*** **B-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2.258 | 2.656 | 2.343 | 2.756 | 2.329 | 2.74 | 2.12 | 2.494 | 2.123 | 2.497 | ns |

### *2.3.7.3 M-LVDS*

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

**Minimum and Maximum Input and Output Levels**

***Table 183 •*** **M-LVDS Recommended DC Operating Conditions**

| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
|---|---|---|---|---|---|
| Supply voltage[1] | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

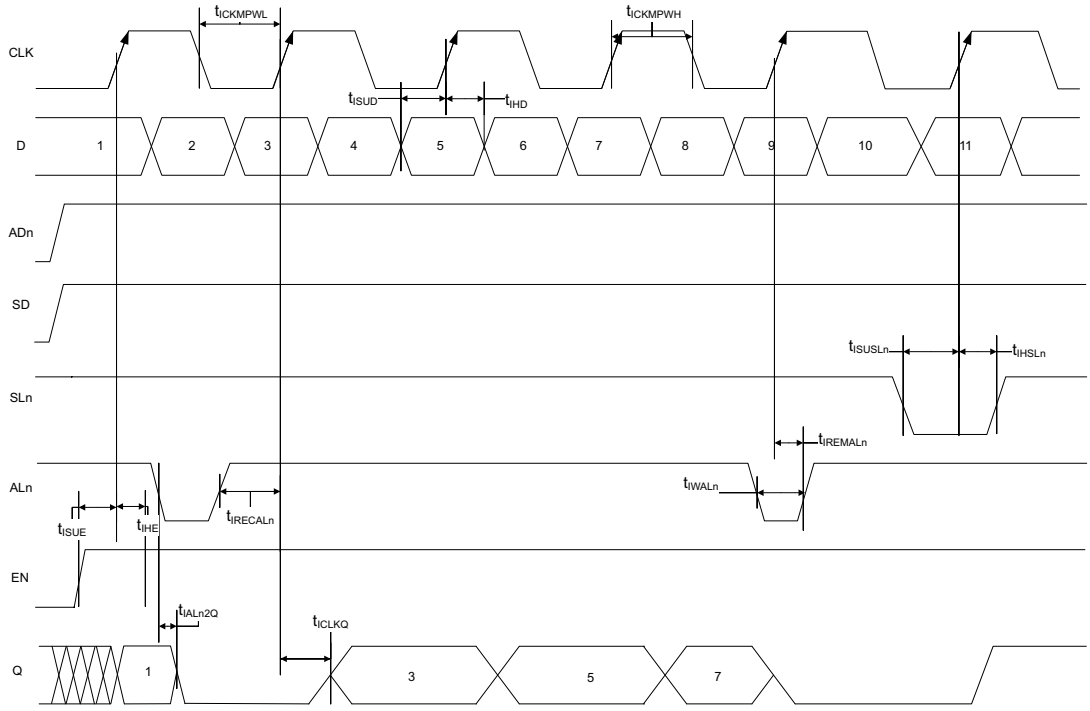
1. Only M-LVDS TYPE I is supported.

***Table 184 •*** **M-LVDS DC Input Voltage Specification**

| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** |
|---|---|---|---|---|
| DC input voltage | $V_I$ | 0 | 2.925 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[2] | $I_{IL}$ (DC) | | | |

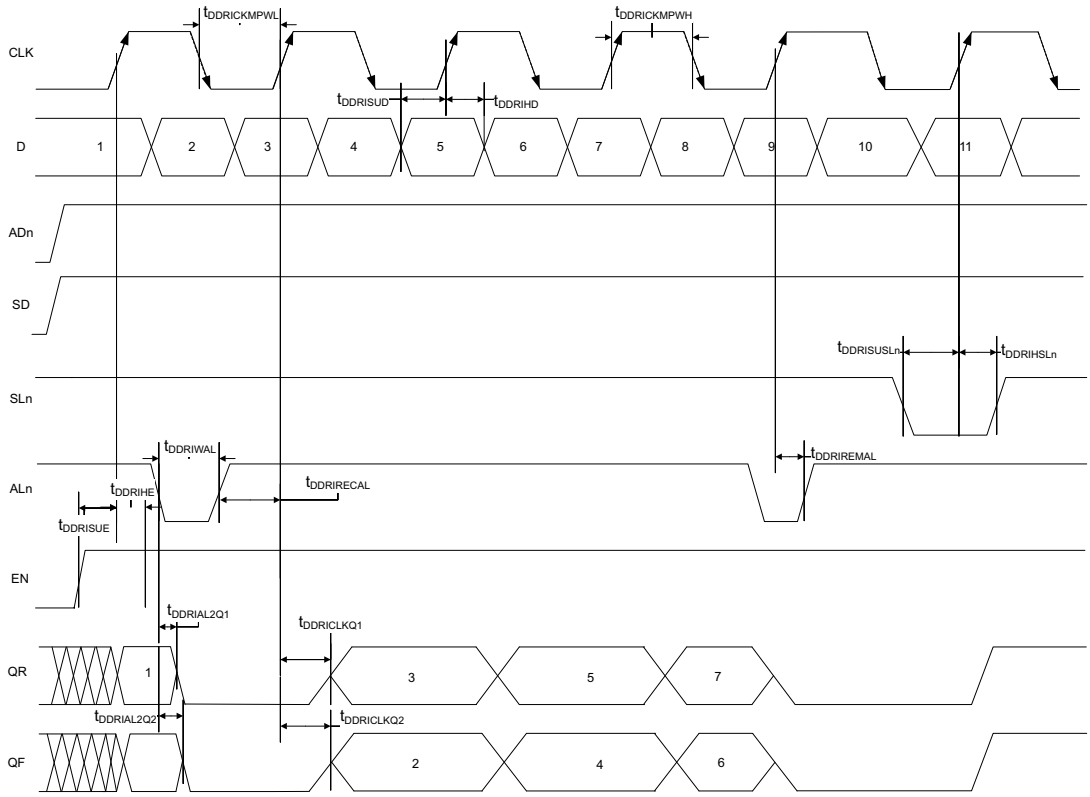
1. See Table 24, page 22.

***Figure 7 •*** **I/O Register Input Timing Diagram**



### 2.3.9.2 Input DDR Timing Diagram

***Figure 11 •*** **Input DDR Timing Diagram**




### 2.3.9.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 221 •*** **Input DDR Propagation Delays**

| Symbol | Description | Measuring Nodes (from, to) | –1 | –Std | Unit |
|---|---|---|---|---|---|
| $T_{DDRICLKQ1}$ | Clock-to-Out Out_QR for input DDR | B, C | 0.16 | 0.188 | ns |
| $T_{DDRICLKQ2}$ | Clock-to-Out Out_QF for input DDR | B, D | 0.166 | 0.195 | ns |
| $T_{DDRISUD}$ | Data setup for input DDR | A, B | 0.357 | 0.421 | ns |
| $T_{DDRIHD}$ | Data hold for input DDR | A, B | 0 | 0 | ns |
| $T_{DDRISUE}$ | Enable setup for input DDR | E, B | 0.46 | 0.542 | ns |
| $T_{DDRIHE}$ | Enable hold for input DDR | E, B | 0 | 0 | ns |
| $T_{DDRISUSLN}$ | Synchronous load setup for input DDR | G, B | 0.46 | 0.542 | ns |
| $T_{DDRIHSLN}$ | Synchronous load hold for input DDR | G, B | 0 | 0 | ns |
| $T_{DDRIAL2Q1}$ | Asynchronous load-to-out QR for input DDR | F, C | 0.587 | 0.69 | ns |
| $T_{DDRIAL2Q2}$ | Asynchronous load-to-out QF for input DDR | F, D | 0.541 | 0.636 | ns |
| $T_{DDRIREMAL}$ | Asynchronous load removal time for input DDR | F, B | 0 | 0 | ns |
| $T_{DDRIRECAL}$ | Asynchronous load recovery time for input DDR | F, B | 0.074 | 0.087 | ns |

***Table 231 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18 *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.529 | | 1.799 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.449 | | 0.528 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.167 | | 0.197 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | – | 1.506 | – | 1.772 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.39 | | 0.458 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.242 | | 0.285 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 2K × 9 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 232 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.334 | | 0.393 | ns |
| Read access time without pipeline register | | | 2.273 | | 2.674 | ns |
| Access time with feed-through write timing | | | 1.529 | | 1.799 | ns |

***Table 232 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Address setup time | $T_{ADDRSU}$ | 0.475 | | 0.559 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.336 | | 0.395 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.529 | | 1.799 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.485 | | 0.57 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.514 | | 1.781 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.415 | | 0.488 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 233 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |

***Table 251 •*** **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only) *(continued)***

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 150 | 544496 | 10 | 158 | 15 | Sec |

***Table 252 •*** **SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 439296 | 9 | 61 | 11 | Sec |
| 010 | 842688 | 15 | 107 | 21 | Sec |
| 025 | 1497408 | 26 | 121 | 35 | Sec |
| 050 | 2695168 | 43 | 141 | 55 | Sec |
| 060 | 2686464 | 48 | 143 | 60 | Sec |
| 090 | 4190208 | 75 | 244 | 91 | Sec |
| 150 | 6682768 | 117 | 296 | 141 | Sec |

***Table 253 •*** **Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)**

| M2S/M2GL Device | Auto Programming 100 kHz | Auto Update 25 MHz | Programming Recovery 12.5 MHz | Unit |
|---|---|---|---|---|
| 005 | 47 | 27 | 28 | Sec |
| 010 | 77 | 35 | 35 | Sec |
| 025 | 150 | 42 | 41 | Sec |
| 050 | 33[1] | Not Supported | Not Supported | Sec |
| 060 | 291 | 83 | 82 | Sec |
| 090 | 427 | 109 | 108 | Sec |
| 150 | 708 | 157 | 160 | Sec |

1. Auto Programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

***Table 254 •*** **Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)**

| M2S/M2GL Device | Auto Programming 100 kHz | Auto Update 25 MHz | Programming Recovery 12.5 MHz | Unit |
|---|---|---|---|---|
| 005 | 41 | 48 | 49 | Sec |
| 010 | 86 | 87 | 87 | Sec |
| 025 | 87 | 85 | 86 | Sec |
| 050 | 85 | Not Supported | Not Supported | Sec |
| 060 | 78 | 86 | 86 | Sec |
| 090 | 154 | 162 | 162 | Sec |

The following table lists the programming times in worst-case conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V. External SPI flash part# AT25DF641-s3H is used during this measurement.

***Table 256 •*** **JTAG Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 302672 | 44 | 10 | Sec |
| 010 | 568784 | 50 | 18 | Sec |
| 025 | 1223504 | 73 | 26 | Sec |
| 050 | 2424832 | 88 | 54 | Sec |
| 060 | 2418896 | 99 | 54 | Sec |
| 090 | 3645968 | 135 | 126 | Sec |
| 150 | 6139184 | 177 | 193 | Sec |

***Table 257 •*** **JTAG Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 137536 | 61 | 4 | Sec |
| 010 | 274816 | 100 | 9 | Sec |
| 025 | 274816 | 100 | 9 | Sec |
| 050 | 2,78,528 | 106 | 8 | Sec |
| 060 | 268480 | 98 | 8 | Sec |
| 090 | 544496 | 176 | 15 | Sec |
| 150 | 544496 | 177 | 15 | Sec |

***Table 258 •*** **JTAG Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 439296 | 71 | 11 | Sec |
| 010 | 842688 | 129 | 20 | Sec |
| 025 | 1497408 | 142 | 35 | Sec |
| 050 | 2695168 | 184 | 59 | Sec |
| 060 | 2686464 | 180 | 70 | Sec |
| 090 | 4190208 | 288 | 147 | Sec |
| 150 | 6682768 | 338 | 231 | Sec |

## 2.3.14 Math Block Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC math block supports 18×18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently. The following table lists the math blocks with all registers used in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 268 •*** **Math Blocks with all Registers Used**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input, control register setup time | $T_{MISU}$ | 0.149 | | 0.176 | | ns |
| Input, control register hold time | $T_{MIHD}$ | 1.68 | | 1.976 | | ns |
| CDIN input setup time | $T_{MOCDINSU}$ | 0.185 | | 0.218 | | ns |
| CDIN input hold time | $T_{MOCDINHD}$ | 0.08 | | 0.094 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | –0.419 | | –0.493 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | 0.011 | | 0.013 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | 0 | | 0 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.088 | | 0.104 | | ns |
| Output register clock to out delay | $T_{MOCQ}$ | | 0.232 | | 0.273 | ns |
| CLK minimum period | $T_{MCLKMP}$ | 2.245 | | 2.641 | | ns |

The following table lists the math blocks with input bypassed and output registers used in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 269 •*** **Math Block with Input Bypassed and Output Registers Used**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Output register setup time | $T_{MOSU}$ | 2.294 | | 2.699 | | ns |
| Output register hold time | $T_{MOHD}$ | 1.68 | | 1.976 | | ns |
| CDIN input setup time | $T_{MOCDINSU}$ | 0.115 | | 0.136 | | ns |
| CDIN input hold time | $T_{MOCDINHD}$ | –0.444 | | –0.522 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | –0.419 | | –0.493 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | 0.011 | | 0.013 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | 0 | | 0 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.014 | | 0.017 | | ns |
| Output register clock to out delay | $T_{MOCQ}$ | | 0.232 | | 0.273 | ns |
| CLK minimum period | $T_{MCLKMP}$ | 2.179 | | 2.563 | | ns |

***Table 276 •*** **Cryptographic Block Characteristics *(continued)***

| Service | Conditions | Timing | Unit |
|---|---|---|---|
| SHA256 | 512 bits | 540 | kbps |
| | 1024 bits | 780 | kbps |
| | 2048 bits | 950 | kbps |
| | 24 kbits | 1140 | kbps |
| HMAC | 512 bytes | 820 | kbps |
| | 1024 bytes | 890 | kbps |
| | 2048 bytes | 930 | kbps |
| | 24 kbytes | 980 | kbps |
| KeyTree | | 1.8 | ms |
| Challenge-response | PUF = OFF | 25 | ms |
| | PUF = ON | 7 | ms |
| ECC point multiplication | | 590 | ms |
| ECC point addition | | 8 | ms |

1. Using cypher block chaining (CBC) mode.

## 2.3.19 Crystal Oscillator

The following table describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

***Table 277 •*** **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 20 | | MHz | |
| Accuracy | ACCXTAL | | | 0.0047 | % | 005, 010, 025, 050, 060, and 090 devices |
| | | | | 0.0058 | % | 150 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 200 | 300 | ps | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 200 | 300 | ps | 010, 025, 050, and 060 devices |
| | | | 250 | 410 | ps | 150 devices |
| | | | 250 | 550 | ps | 005 and 090 devices |
| Operating current | IDYNXTAL | | 1.5 | | mA | 010, 050, and 060 devices |
| | | | 1.65 | | mA | 005, 025, 090, and 150 devices |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |

***Table 277 •*** **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)** ***(continued)***

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 0.8 | ms | 005, 010, 025, and 050 devices |
| | | | | 1.0 | ms | 090 and 150 devices |

***Table 278 •*** **Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 2 | | MHz | |
| Accuracy | ACCXTAL | | | 0.00105 | % | 050 devices |
| | | | | 0.003 | % | 005, 010, 025, 090, and 150 devices |
| | | | | 0.004 | % | 060 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 1 | 5 | ns | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 1 | 5 | ns | |
| Operating current | IDYNXTAL | | 0.3 | | mA | |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 4.5 | ms | 010 and 050 devices |
| | | | | 5 | ms | 005 and 025 devices |
| | | | | 7 | ms | 090 and 150 devices |

***Table 279 •*** **Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 32 | | kHz | |
| Accuracy | ACCXTAL | | | 0.004 | % | 005, 010, 025, 050, 060, and 090 devices |
| | | | | 0.005 | % | 150 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 150 | 300 | ns | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 150 | 300 | ns | |
| Operating current | IDYNXTAL | | 0.044 | | mA | 010 and 050 devices |
| | | | 0.060 | | mA | 005, 025, 060, 090, and 150 devices |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 115 | ms | 005, 025, 050, 090, and 150 devices |
| | | | | 126 | ms | 010 devices |

The following table lists the receiver pa in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 297 •*** **Receiver Parameters**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VRX-IN-PP-CC | Differential input peak-to-peak sensitivity (2.5 Gbps) | 0.238 | | 1.2 | V |
| | Differential input peak-to-peak sensitivity (2.5 Gbps, de-emphasized) | 0.219 | | 1.2 | V |
| | Differential input peak-to-peak sensitivity (5.0 Gbps) | 0.300 | | 1.2 | V |
| | Differential input peak-to-peak sensitivity (5.0 Gbps, de-emphasized) | 0.300 | | 1.2 | V |
| VRX-CM-AC-P | Input common mode range (AC coupled) | | | 150 | mV |
| ZRX-DIFF-DC | Differential input termination | 80 | 100 | 120 | Ω |
| REXT | External calibration resistor | 1,188 | 1,200 | 1,212 | Ω |
| CDR-LOCK-RST | CDR relock time from reset | | | 15 | µs |
| RLRX-DIFF | Return loss differential mode (2.5 Gbps) | –10 | | | dB |
| | Return loss differential mode (5.0 Gbps) | | | | |
| | 0.05 GHz to 1.25 GHz | –10 | | | dB |
| | 1.25 GHz to 2.5 GHz | –8 | | | dB |
| RLRX-CM | Return loss common mode (2.5 Gbps, 5.0 Gbps) | –6 | | | dB |
| RX-CID[1] | CID limit PCIe Gen1/2 | | | 200 | UI |
| VRX-IDLE-DET-DIFF-PP | Signal detect limit | 65 | | 175 | mV |

1. AC-coupled, BER = $e^{-12}$, using synchronous clock.

***Table 298 •*** **SerDes Protocol Compliance**

| Protocol | Maximum Data Rate (Gbps) | –1 | –Std |
|---|---|---|---|
| PCIe Gen 1 | 2.5 | Yes | Yes |
| PCIe Gen 2 | 5.0 | Yes | |
| XAUI | 3.125 | Yes | |
| Generic EPCS | 3.2 | Yes | |
| Generic EPCS | 2.5 | Yes | Yes |