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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 10K Logic Modules
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	400-LFBGA
Supplier Device Package	400-VFBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s010t-vf400i">https://www.e-xfl.com/product-detail/microchip-technology/m2s010t-vf400i</a>

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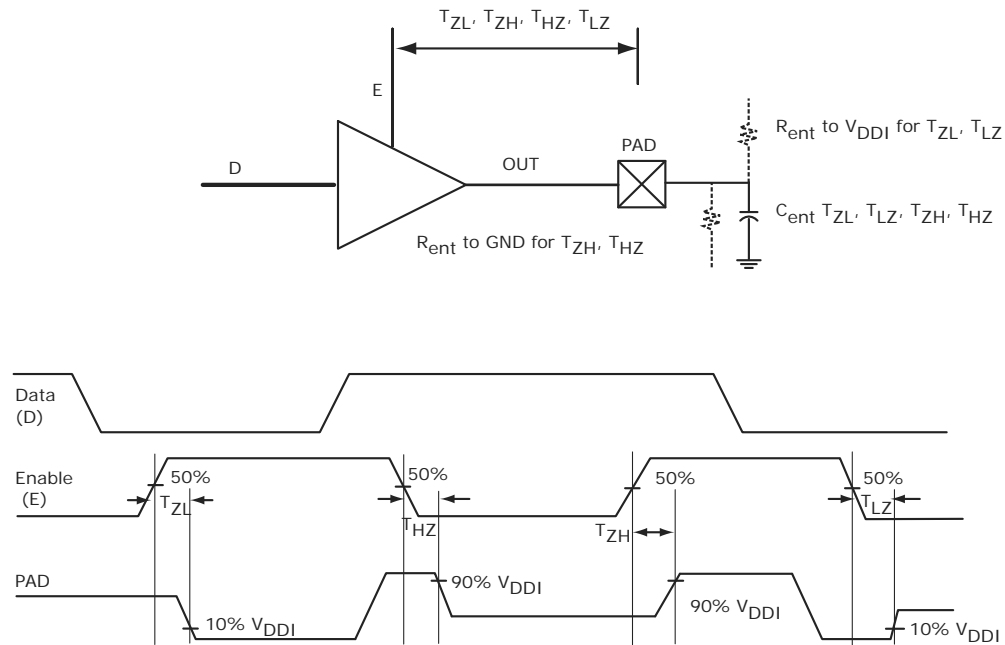




### 2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

**Figure 5 • Tristate Buffer for Enable Path Test Point**



### 2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

**Table 18 • Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	630			Mbps
LVTTL 3.3 V	600			Mbps
LVC MOS 3.3 V	600			Mbps
LVC MOS 2.5 V	410	420	400	Mbps
LVC MOS 1.8 V	295	400	400	Mbps
LVC MOS 1.5 V	160	220	235	Mbps
LVC MOS 1.2 V	120	160	200	Mbps
LPDDR-LVC MOS 1.8 V mode			400	Mbps

### 2.3.5.7 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs that are in compliance with the JEDEC specification JESD8-5A.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 38 • LVCMOS 2.5 V DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V

**Table 39 • LVCMOS 2.5 V DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	$V_{IH}$ (DC)	1.7	2.625	V
DC input logic high (for MSIO I/O bank)	$V_{IH}$ (DC)	1.7	3.45	V
DC input logic low	$V_{IL}$ (DC)	-0.3	0.7	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 40 • LVCMOS 2.5 V DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	$V_{OH}$ <sup>1</sup>	$V_{DDI} - 0.4$	-	V
DC output logic low	$V_{OL}$ <sup>2</sup>		0.4	V

1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

**Table 41 • LVCMOS 2.5 V AC Minimum and Maximum Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	$D_{MAX}$	400	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	410	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	$D_{MAX}$	420	Mbps	AC loading: 17 pF load, maximum drive/slew

**Table 42 • LVCMOS 2.5 V AC Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	Rodt_cal	75, 60, 50, 33, 25, 20	$\Omega$



**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 1.425\text{ V}$

**Table 67 • LVCMOS 1.5 V Receiver Characteristics for DDRIO I/O Bank with Fixed Codes (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
	-1	-Std	-1	-Std	
None	2.051	2.413	2.086	2.455	ns

**Table 68 • LVCMOS 1.5 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
	-1	-Std	-1	-Std	
None	3.311	3.896	3.285	3.865	ns
50	3.654	4.299	3.623	4.263	ns
75	3.533	4.156	3.501	4.119	ns
150	3.415	4.018	3.388	3.986	ns

**Table 69 • LVCMOS 1.5 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
	-1	-Std	-1	-Std	
None	2.959	3.481	2.93	3.447	ns
50	3.298	3.88	3.268	3.845	ns
75	3.162	3.719	3.128	3.68	ns
150	3.053	3.592	3.021	3.554	ns

**Table 70 • LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	5.122	6.026	4.31	5.07	5.145	6.052	5.258	6.186	4.672	5.496	ns
	Medium	4.58	5.389	3.86	4.54	4.6	5.411	4.977	5.855	4.357	5.126	ns
	Medium fast	4.323	5.086	3.629	4.269	4.341	5.107	4.804	5.652	4.228	4.974	ns
	Fast	4.296	5.054	3.609	4.245	4.314	5.075	4.791	5.636	4.219	4.963	ns
4 mA	Slow	4.449	5.235	3.707	4.361	4.443	5.227	6.058	7.127	5.458	6.421	ns
	Medium	3.961	4.66	3.264	3.839	3.954	4.651	5.778	6.797	5.116	6.018	ns
	Medium fast	3.729	4.387	3.043	3.579	3.72	4.376	5.63	6.624	4.981	5.86	ns
	Fast	3.704	4.358	3.027	3.56	3.695	4.347	5.624	6.617	4.973	5.851	ns

### 2.3.6.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 103 • DDR1/SSTL2 DC Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V
Termination voltage	$V_{TT}$	1.164	1.250	1.339	V
Input reference voltage	$V_{REF}$	1.164	1.250	1.339	V

**Table 104 • DDR1/SSTL2 DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}$ (DC)	$V_{REF} + 0.15$	2.625	V
DC input logic low	$V_{IL}$ (DC)	-0.3	$V_{REF} - 0.15$	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 105 • DDR1/SSTL2 DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
<b>SSTL2 Class I (DDR Reduced Drive)</b>				
DC output logic high	$V_{OH}$	$V_{TT} + 0.608$		V
DC output logic low	$V_{OL}$		$V_{TT} - 0.608$	V
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	8.1		mA
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-8.1		mA
<b>SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Bank Only</b>				
DC output logic high	$V_{OH}$	$V_{TT} + 0.81$		V
DC output logic low	$V_{OL}$		$V_{TT} - 0.81$	V
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	16.2		mA
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-16.2		mA

**Table 106 • DDR1/SSTL2 DC Differential Voltage Specification**

Parameter	Symbol	Min	Unit
DC input differential voltage	$V_{ID}$ (DC)	0.3	V

**Table 107 • SSTL2 AC Differential Voltage Specifications**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	$V_{DIFF(AC)}$	0.7		V
AC differential cross point voltage	$V_x(AC)$	$0.5 \times V_{DDI} - 0.2$	$0.5 \times V_{DDI} + 0.2$	V

**Table 108 • SSTL2 Minimum and Maximum AC Switching Speeds**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	$D_{MAX}$	400	Mbps	AC loading: per JEDEC specifications
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	575	Mbps	AC loading: 17pF load
Maximum data rate (for MSIOD I/O bank)	$D_{MAX}$	700	Mbps	AC loading: 3 pF / 50 $\Omega$ load
		510	Mbps	AC loading: 17pF load

**Table 109 • SSTL2 AC Impedance Specifications**

Parameter	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	20, 42	$\Omega$	Reference resistor = 150 $\Omega$

**Table 110 • DDR1/SSTL2 AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	1.25	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Reference resistance for data test path for SSTL2 Class I ( $T_{DP}$ )	$R_{TT\_TEST}$	50	$\Omega$
Reference resistance for data test path for SSTL2 Class II ( $T_{DP}$ )	$R_{TT\_TEST}$	25	$\Omega$
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

### AC Switching Characteristics

Worst commercial-case conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

**Table 111 • SSTL2 Receiver Characteristics for DDRIO I/O Bank (Input Buffers)**

	On-Die Termination (ODT)	$T_{PY}$		Unit
		-1	-Std	
Pseudo differential	None	1.549	1.821	ns
True differential	None	1.589	1.87	ns

**Table 118 • DDR1/SSTL2 Class II Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.29	2.693	1.988	2.338	1.978	2.326	1.989	2.34	1.979	2.328	ns
Differential	2.418	2.846	2.304	2.711	2.297	2.702	2.131	2.506	2.124	2.499	ns

**2.3.6.4 Stub-Series Terminated Logic 1.8 V (SSTL18)**

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

**Table 119 • SSTL18 DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	1.71	1.8	1.89	V
Termination voltage	$V_{TT}$	0.838	0.900	0.964	V
Input reference voltage	$V_{REF}$	0.838	0.900	0.964	V

**Table 120 • SSTL18 DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}$ (DC)	$V_{REF} + 0.125$	1.89	V
DC input logic low	$V_{IL}$ (DC)	-0.3	$V_{REF} - 0.125$	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 121 • SSTL18 DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
<b>SSTL18 Class I (DDR2 Reduced Drive)</b>				
DC output logic high	$V_{OH}$	$V_{TT} + 0.603$		V
DC output logic low	$V_{OL}$		$V_{TT} - 0.603$	V
Output minimum source DC current (DDRIO I/O bank only)	$I_{OH}$ at $V_{OH}$	6.5		mA
Output minimum sink current (DDRIO I/O bank only)	$I_{OL}$ at $V_{OL}$	-6.5		mA
<b>SSTL18 Class II (DDR2 Full Drive)<sup>1</sup></b>				
DC output logic high	$V_{OH}$	$V_{TT} + 0.603$		V
DC output logic low	$V_{OL}$		$V_{TT} - 0.603$	V
Output minimum source DC current (DDRIO I/O bank only)	$I_{OH}$ at $V_{OH}$	13.4		mA
Output minimum sink current (DDRIO I/O bank only)	$I_{OL}$ at $V_{OL}$	-13.4		mA

1. To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.

**Table 122 • SSTL18 DC Differential Voltage Specification**

Parameter	Symbol	Min	Unit
DC input differential voltage	$V_{ID}$ (DC)	0.3	V

**Table 123 • SSTL18 AC Differential Voltage Specifications (Applicable to DDRIO Bank Only)**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	$V_{DIFF}$ (AC)	0.5		V
AC differential cross point voltage	$V_x$ (AC)	$0.5 \times V_{DDI} - 0.175$	$0.5 \times V_{DDI} + 0.175$	V

**Table 124 • SSTL18 Minimum and Maximum AC Switching Speed (Applicable to DDRIO Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	$D_{MAX}$	667	Mbps	AC loading: per JEDEC specification

**Table 125 • SSTL18 AC Impedance Specifications (Applicable to DDRIO Bank Only)**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	$R_{REF}$	20, 42	$\Omega$	Reference resistor = 150 $\Omega$
Effective impedance value (ODT)	$R_{TT}$	50, 75, 150	$\Omega$	Reference resistor = 150 $\Omega$

**Table 126 • SSTL18 AC Test Parameter Specifications (Applicable to DDRIO Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	0.9	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Reference resistance for data test path for SSTL18 Class I ( $T_{DP}$ )	$R_{TT\_TEST}$	50	$\Omega$
Reference resistance for data test path for SSTL18 Class II ( $T_{DP}$ )	$R_{TT\_TEST}$	25	$\Omega$
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 1.71\text{ V}$

**Table 127 • DDR2/SSTL18 Receiver Characteristics for DDRIO I/O Bank with Fixed Code**

	On-Die Termination (ODT)	$T_{PY}$		Unit
		-1	-Std	
Pseudo differential	None	1.567	1.844	ns
True differential	None	1.588	1.869	ns

**Table 221 • Input DDR Propagation Delays (continued)**

<b>Symbol</b>	<b>Description</b>	<b>Measuring Nodes (from, to)</b>	<b>-1</b>	<b>-Std</b>	<b>Unit</b>
$T_{DDRIWAL}$	Asynchronous load minimum pulse width for input DDR	F, F	0.304	0.357	ns
$T_{DDRICKMPWH}$	Clock minimum pulse width high for input DDR	B, B	0.075	0.088	ns
$T_{DDRICKMPWL}$	Clock minimum pulse width low for input DDR	B, B	0.159	0.187	ns

**Table 232 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 (continued)**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Address setup time	$T_{ADDRSU}$	0.475		0.559		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.336		0.395		ns
Data hold time	$T_{DHD}$	0.082		0.096		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns
Block select hold time	$T_{BLKHD}$	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		1.529		1.799	ns
Block select minimum pulse width	$T_{BLKMPW}$	0.186		0.219		ns
Read enable setup time	$T_{RDESU}$	0.485		0.57		ns
Read enable hold time	$T_{RDEHD}$	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	$T_{R2Q}$		1.514		1.781	ns
Asynchronous reset removal time	$T_{RSTREM}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTREC}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	$T_{RSTMPW}$	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTSU}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTHD}$	0.036		0.043		ns
Write enable setup time	$T_{WESU}$	0.415		0.488		ns
Write enable hold time	$T_{WEHD}$	0.048		0.057		ns
Maximum frequency	$F_{MAX}$		400		340	MHz

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 233 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	$T_{CY}$	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	$T_{PLCY}$	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns

**Table 238 •  $\mu$ SRAM (RAM64x16) in 64 x 16 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read synchronous reset hold time	$T_{SRSTHD}$	0.061		0.071		ns
Write clock period	$T_{CCY}$	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	$T_{BLKCSU}$	0.404		0.476		ns
Write block hold time	$T_{BLKCHD}$	0.007		0.008		ns
Write input data setup time	$T_{DINCSU}$	0.115		0.135		ns
Write input data hold time	$T_{DINCHD}$	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.026		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

The following table lists the  $\mu$ SRAM in 128 x 9 mode in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 239 •  $\mu$ SRAM (RAM128x9) in 128 x 9 Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	$T_{CY}$	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	$T_{PLCY}$	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	$T_{CLK2Q}$		0.266		0.313	ns
Read access time without pipeline register				1.677		1.973
Read address setup time in synchronous mode	$T_{ADDRSU}$	0.301		0.354		ns
Read address setup time in asynchronous mode			1.856		2.184	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.091		0.107		ns
Read address hold time in asynchronous mode			-0.778		-0.915	
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHD}$	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.036		2.396	ns



**Table 239 •  $\mu$ SRAM (RAM128x9) in 128 × 9 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read asynchronous reset removal time (pipelined clock)		-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)	$T_{RSTREM}$	0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)		0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)	$T_{RSTREC}$	0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	$T_{R2Q}$		0.835		0.982	ns
Read synchronous reset setup time	$T_{SRSTSU}$	0.271		0.319		ns
Read synchronous reset hold time	$T_{SRSTHD}$	0.061		0.071		ns
Write clock period	$T_{CCY}$	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	$T_{BLKCSU}$	0.404		0.476		ns
Write block hold time	$T_{BLKCHD}$	0.007		0.008		ns
Write input data setup time	$T_{DINCSU}$	0.115		0.135		ns
Write input data hold time	$T_{DINCHD}$	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.026		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

The following table lists the  $\mu$ SRAM in 128 × 8 mode in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 240 •  $\mu$ SRAM (RAM128x8) in 128 × 8 Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	$T_{CY}$	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	$T_{PLCY}$	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register			0.266		0.313	ns
Read access time without pipeline register	$T_{CLK2Q}$		1.677		1.973	ns
Read address setup time in synchronous mode		0.301		0.354		ns
Read address setup time in asynchronous mode	$T_{ADDRSU}$	1.856		2.184		ns

**Table 251 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only) (continued)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
150	544496	10	158	15	Sec

**Table 252 • SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	9	61	11	Sec
010	842688	15	107	21	Sec
025	1497408	26	121	35	Sec
050	2695168	43	141	55	Sec
060	2686464	48	143	60	Sec
090	4190208	75	244	91	Sec
150	6682768	117	296	141	Sec

**Table 253 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	Unit
	100 kHz	25 MHz	12.5 MHz	
005	47	27	28	Sec
010	77	35	35	Sec
025	150	42	41	Sec
050	33 <sup>1</sup>	Not Supported	Not Supported	Sec
060	291	83	82	Sec
090	427	109	108	Sec
150	708	157	160	Sec

1. Auto Programming in 050 device is done through SC\_SPI, and SPI CLK is set to 6.25 MHz.

**Table 254 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	Unit
	100 kHz	25 MHz	12.5 MHz	
005	41	48	49	Sec
010	86	87	87	Sec
025	87	85	86	Sec
050	85	Not Supported	Not Supported	Sec
060	78	86	86	Sec
090	154	162	162	Sec

**Table 265 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	69	49	50	Sec
010	99	57	57	Sec
025	150	64	63	Sec
050	55 <sup>1</sup>	Not Supported	Not Supported	Sec
060	313	105	104	Sec
090	449	131	130	Sec
150	730	179	183	Sec

1. Auto programming in 050 device is done through SC\_SPI, and SPI CLK is set to 6.25 MHz.

**Table 266 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	63	70	71	Sec
010	108	109	109	Sec
025	109	107	108	Sec
050	107	Not Supported	Not Supported	Sec
060	100	108	108	Sec
090	176	184	184	Sec
150	183	183	183	Sec

**Table 267 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	109	89	88	Sec
010	183	135	135	Sec
025	251	142	143	Sec
050	134	Not Supported	Not Supported	Sec
060	390	183	180	Sec
090	604	283	282	Sec
150	889	331	332	Sec

## 2.3.20 On-Chip Oscillator

The following tables describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

**Table 280 • Electrical Characteristics of the 50 MHz RC Oscillator**

Parameter	Symbol	Typ	Max	Unit	Condition
Operating frequency	F50RC	50		MHz	
Accuracy	ACC50RC	1	4	%	050 devices
		1	5	%	005, 025, and 060 devices
		1	6.3	%	090 devices
		1	7.1	%	010 and 150 devices
Output duty cycle	CYC50RC	49–51	46.5–53.5	%	
Output jitter (peak to peak)	JIT50RC	Period Jitter			
		200	300	ps	005, 010, 050, and 060 devices
		200	400	ps	150 devices
		300	500	ps	025 and 090 devices
		Cycle-to-Cycle Jitter			
		200	300	ps	005 and 050 devices
		320	420	ps	010, 060, and 150 devices
		320	850	ps	025 and 090 devices
Operating current	IDYN50RC	6.5		mA	

**Table 281 • Electrical Characteristics of the 1 MHz RC Oscillator**

Parameter	Symbol	Typ	Max	Unit	Condition
Operating frequency	F1RC	1		MHz	
Accuracy	ACC1RC	1	3	%	005, 010, 025, and 050 devices
		1	4.5	%	060, and 150 devices
		1	5.6	%	090 devices
Output duty cycle	CYC1RC	49–51	46.5–53.5	%	005, 010, 025, 050, 090 and 150 devices
		49-51	46.0-54.0	%	060 devices
Output jitter (peak to peak)	JIT1RC	Period Jitter			
		10	20	ns	005, 010, 025, and 050 devices
		10	28	ns	060, 090 and 150 devices
		Cycle-to-Cycle Jitter			
		10	20	ns	005, 010, and 050 devices
		10	35	ns	025, 060, and 150 devices
		10	45	ns	090 devices
Operating current	IDYN1RC	0.1		mA	
Startup time	SU1RC	17		μs	050, 090, and 150 devices
		18		μs	005, 010, and 025 devices

**Table 293 • Flash\*Freeze Entry and Exit Times (continued)**

Parameter	Symbol	Entry/Exit Timing			Unit	Conditions
		FCLK = 100MHz		FCLK = 3 MHz		
		005, 010, 025, 060, 090, and 150	050	All Devices		
Exit time with respect to the fabric PLL lock <sup>1</sup>	TFF_EXIT	1.5	1.5	1.5	ms	eNVM and MSS/HPMS PLL = ON during F*F
		1.5	1.5	1.5	ms	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit
Exit time with respect to the fabric buffer output	TFF_EXIT	21	15	21	µs	eNVM and MSS/HPMS PLL = ON during F*F
		65	55	65	µs	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit

1. PLL Lock Delay set to 1024 cycles (default).

### 2.3.28 DDR Memory Interface Characteristics

The following table lists the DDR memory interface characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 294 • DDR Memory Interface Characteristics**

Standard	Supported Data Rate		Unit
	Min	Max	
DDR3	667	667	Mbps
DDR2	667	667	Mbps
LPDDR	50	400	Mbps

### 2.3.29 SFP Transceiver Characteristics

IGLOO2 and SmartFusion2 SerDes complies with small form-factor pluggable (SFP) requirements as specified in SFP INF-80741. The following table provides the electrical characteristics.

The following table lists the SFP transceiver electrical characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 295 • SFP Transceiver Electrical Characteristics**

Pin	Direction	Differential Peak-Peak Voltage		Unit
		Min	Max	
RD+/- <sup>1</sup>	Output	1600	2400	mV
TD+/- <sup>2</sup>	Input	350	2400	mV

1. Based on default SerDes transmitter settings for PCIe Gen1. Lower amplitudes are available through programming changes to TX\_AMP setting.
2. Based on Input Voltage Common-Mode (VICM) = 0 V. Requires AC Coupling.