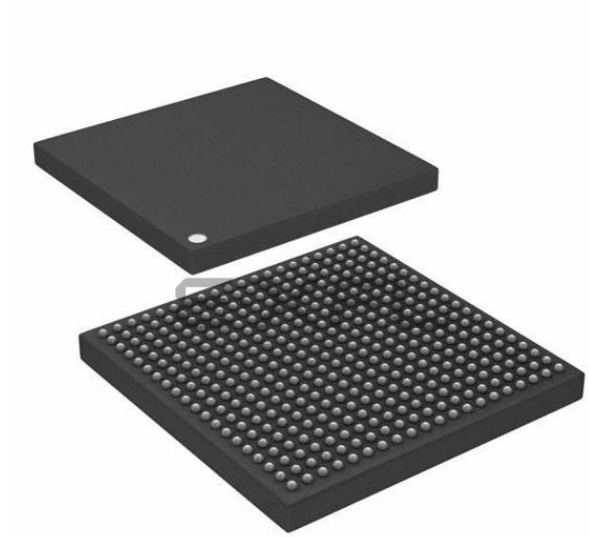


Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 10K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-LFBGA
Supplier Device Package	400-VFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s010t-vfg400

Tables

where

θ_{JA} = Junction-to-air thermal resistance

θ_{JB} = Junction-to-board thermal resistance

θ_{JC} = Junction-to-case thermal resistance

T_J = Junction temperature

T_A = Ambient temperature

T_B = Board temperature (measured 1.0 mm away from the package edge)

T_C = Case temperature

P = Total power dissipated by the device

Table 9 • **Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices**

	Still Air	1.0 m/s	2.5 m/s			
Device		**θ_{JA}**		**θ_{JB}**	**θ_{JC}**	**Unit**
005						
FG484	19.36	15.81	14.63	9.74	5.27	°C/W
VF256	41.30	38.16	35.30	28.41	3.94	°C/W
VF400	20.19	16.94	15.41	8.86	4.95	°C/W
TQ144	42.80	36.80	34.50	37.20	10.80	°C/W
010						
FG484	18.22	14.83	13.62	8.83	4.92	°C/W
VF256	37.36	34.26	31.45	24.84	7.89	°C/W
VF400	19.40	15.75	14.22	8.11	4.22	°C/W
TQ144	38.60	32.60	30.30	31.80	8.60	°C/W
025						
FG484	17.03	13.66	12.45	7.66	4.18	°C/W
VF256	33.85	30.59	27.85	21.63	6.13	°C/W
VF400	18.36	14.89	13.36	7.12	3.41	°C/W
FCS325	29.17	24.87	23.12	14.44	2.31	°C/W
050						
FG484	15.29	12.19	10.99	6.27	3.24	°C/W
FG896	14.70	12.50	10.90	7.20	4.90	°C/W
VF400	17.53	14.17	12.63	6.32	2.81	°C/W
FCS325	27.38	23.18	21.41	12.47	1.59	°C/W
060						
FG484	15.40	12.06	10.85	6.14	3.15	°C/W
FG676	15.49	12.21	11.06	7.07	3.87	°C/W
VF400	17.45	14.01	12.47	6.22	2.69	°C/W
FCS325	27.03	22.91	21.25	12.33	1.54	°C/W
090						
FG484	14.64	11.37	10.16	5.43	2.77	°C/W
FG676	14.52	11.19	10.37	6.17	3.24	°C/W
FCS325	26.63	22.26	20.13	14.24	2.50	°C/W

2.3.4 Timing Model

This section describes timing model and timing parameters.

Figure 2 • **Timing Model**

The following table lists the timing model parameters in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 17 • **Timing Model Parameters**

Index	Symbol	Description	–1	Unit	For More Information
A	T_{PY}	Propagation delay of DDR3 receiver	1.605	ns	See Table 137, page 50
B	T_{ICLKQ}	Clock-to-Q of the input data register	0.16	ns	See Table 221, page 71
	T_{ISUD}	Setup time of the input data register	0.357	ns	See Table 221, page 71
C	T_{RCKH}	Input high delay for global clock	1.53	ns	See Table 227, page 78
	T_{RCKL}	Input low delay for global clock	0.897	ns	See Table 227, page 78
D	T_{PY}	Input propagation delay of LVDS receiver	2.774	ns	See Table 167, page 56
E	T_{DP}	Propagation delay of a three-input AND gate	0.198	ns	See Table 223, page 76

Table 19 • **Maximum Data Rate Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
LPDDR			400	Mbps
HSTL1.5 V			400	Mbps
SSTL 2.5 V	510	700	400	Mbps
SSTL 1.8 V			667	Mbps
SSTL 1.5 V			667	Mbps

Table 20 • **Maximum Data Rate Summary Table for Differential I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	Unit
LVPECL (input only)	900		Mbps
LVDS 3.3 V	535		Mbps
LVDS 2.5 V	535	700	Mbps
RSDS	520	700	Mbps
BLVDS	500		Mbps
MLVDS	500		Mbps
Mini-LVDS	520	700	Mbps

Table 21 • **Maximum Frequency Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	315			MHz
LVTTL 3.3 V	300			MHz
LVCMOS 3.3 V	300			MHz
LVCMOS 2.5 V	205	210	200	MHz
LVCMOS 1.8 V	147.5	200	200	MHz
LVCMOS 1.5 V	80	110	118	MHz
LVCMOS 1.2 V	60	80	100	MHz
LPDDR– LVCMOS 1.8 V mode			200	MHz

Table 34 • **LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.4	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 35 • **LVTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank**

Output Drive Selection	V_{OH} (V)	V_{OL} (V)	IOH (at V_{OH}) mA	IOL (at V_{OL}) mA
2 mA	V_{DDI} – 0.4	0.4	2	2
4 mA	V_{DDI} – 0.4	0.4	4	4
8 mA	V_{DDI} – 0.4	0.4	8	8
12 mA	V_{DDI} – 0.4	0.4	12	12
16 mA	V_{DDI} – 0.4	0.4	16	16
20 mA	V_{DDI} – 0.4	0.4	20	20

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 3.0 V

Table 36 • **LVTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	–1	–Std	–1	–Std	
None	2.262	2.663	2.289	2.695	ns

Table 37 • **LVTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		Unit
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	
2 mA	Slow	3.192	3.755	3.47	4.083	2.969	3.494	1.856	2.183	3.337	3.926	ns
4 mA	Slow	2.331	2.742	2.673	3.145	2.526	2.973	3.034	3.569	4.451	5.236	ns
8 mA	Slow	2.135	2.511	2.33	2.741	2.297	2.703	4.532	5.331	4.825	5.676	ns
12 mA	Slow	2.052	2.414	2.107	2.479	2.162	2.544	5.75	6.764	5.445	6.406	ns
16 mA	Slow	2.062	2.425	2.072	2.438	2.145	2.525	5.993	7.05	5.625	6.618	ns
20 mA	Slow	2.148	2.527	1.999	2.353	2.088	2.458	6.262	7.367	5.876	6.913	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 1.425 V

Table 67 • **LVCMOS 1.5 V Receiver Characteristics for DDRIO I/O Bank with Fixed Codes (Input Buffers)**

On-Die Termination (ODT)	T_{PY}		T_{PYS}		
	–1	–Std	–1	–Std	Unit
None	2.051	2.413	2.086	2.455	ns

Table 68 • **LVCMOS 1.5 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

On-Die Termination (ODT)	T_{PY}		T_{PYS}		
	–1	–Std	–1	–Std	Unit
None	3.311	3.896	3.285	3.865	ns
50	3.654	4.299	3.623	4.263	ns
75	3.533	4.156	3.501	4.119	ns
150	3.415	4.018	3.388	3.986	ns

Table 69 • **LVCMOS 1.5 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

On-Die Termination (ODT)	T_{PY}		T_{PYS}		
	–1	–Std	–1	–Std	Unit
None	2.959	3.481	2.93	3.447	ns
50	3.298	3.88	3.268	3.845	ns
75	3.162	3.719	3.128	3.68	ns
150	3.053	3.592	3.021	3.554	ns

Table 70 • **LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	Unit
2 mA	Slow	5.122	6.026	4.31	5.07	5.145	6.052	5.258	6.186	4.672	5.496	ns
	Medium	4.58	5.389	3.86	4.54	4.6	5.411	4.977	5.855	4.357	5.126	ns
	Medium fast	4.323	5.086	3.629	4.269	4.341	5.107	4.804	5.652	4.228	4.974	ns
	Fast	4.296	5.054	3.609	4.245	4.314	5.075	4.791	5.636	4.219	4.963	ns
4 mA	Slow	4.449	5.235	3.707	4.361	4.443	5.227	6.058	7.127	5.458	6.421	ns
	Medium	3.961	4.66	3.264	3.839	3.954	4.651	5.778	6.797	5.116	6.018	ns
	Medium fast	3.729	4.387	3.043	3.579	3.72	4.376	5.63	6.624	4.981	5.86	ns
	Fast	3.704	4.358	3.027	3.56	3.695	4.347	5.624	6.617	4.973	5.851	ns

Table 118 • **DDR1/SSTL2 Class II Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
	–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
Single-ended	2.29	2.693	1.988	2.338	1.978	2.326	1.989	2.34	1.979	2.328	ns
Differential	2.418	2.846	2.304	2.711	2.297	2.702	2.131	2.506	2.124	2.499	ns

2.3.6.4 Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double date rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 119 • **SSTL18 DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.71	1.8	1.89	V
Termination voltage	V_{TT}	0.838	0.900	0.964	V
Input reference voltage	V_{REF}	0.838	0.900	0.964	V

Table 120 • **SSTL18 DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high	V_{IH} (DC)	V_{REF} + 0.125	1.89	V
DC input logic low	V_{IL} (DC)	–0.3	V_{REF} – 0.125	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

1. See Table 24, page 22.

Table 121 • **SSTL18 DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
SSTL18 Class I (DDR2 Reduced Drive)				
DC output logic high	V_{OH}	V_{TT} + 0.603		V
DC output logic low	V_{OL}		V_{TT}– 0.603	V
Output minimum source DC current (DDRIO I/O bank only)	I_{OH} at V_{OH}	6.5		mA
Output minimum sink current (DDRIO I/O bank only)	I_{OL} at V_{OL}	–6.5		mA
SSTL18 Class II (DDR2 Full Drive)[1]				
DC output logic high	V_{OH}	V_{TT} + 0.603		V
DC output logic low	V_{OL}		V_{TT}– 0.603	V
Output minimum source DC current (DDRIO I/O bank only)	I_{OH} at V_{OH}	13.4		mA
Output minimum sink current (DDRIO I/O bank only)	I_{OL} at V_{OL}	–13.4		mA

1. To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.

Table 122 • **SSTL18 DC Differential Voltage Specification**

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID} (DC)	0.3	V

Table 123 • **SSTL18 AC Differential Voltage Specifications (Applicable to DDRIO Bank Only)**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF} (AC)	0.5		V
AC differential cross point voltage	V_x (AC)	0.5 × V_{DDI} – 0.175	0.5 × V_{DDI} + 0.175	V

Table 124 • **SSTL18 Minimum and Maximum AC Switching Speed (Applicable to DDRIO Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	667	Mbps	AC loading: per JEDEC specification

Table 125 • **SSTL18 AC Impedance Specifications (Applicable to DDRIO Bank Only)**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	R_{REF}	20, 42	Ω	Reference resistor = 150 Ω
Effective impedance value (ODT)	R_{TT}	50, 75, 150	Ω	Reference resistor = 150 Ω

Table 126 • **SSTL18 AC Test Parameter Specifications (Applicable to DDRIO Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.9	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for SSTL18 Class I (T_{DP})	RTT_TEST	50	Ω
Reference resistance for data test path for SSTL18 Class II (T_{DP})	RTT_TEST	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 1.71 V

Table 127 • **DDR2/SSTL18 Receiver Characteristics for DDRIO I/O Bank with Fixed Code**

		T_{PY}		
	On-Die Termination (ODT)	–1	–Std	Unit
Pseudo differential	None	1.567	1.844	ns
True differential	None	1.588	1.869	ns

Table 131 • **SSTL15 DC Output Voltage Specification (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DDR3/SSTL15 Class I (DDR3 Reduced Drive)				
DC output logic high	V_{OH}	0.8 × V_{DDI}		V
DC output logic low	V_{OL}		0.2 × V_{DDI}	V
Output minimum source DC current	I_{OH} at V_{OH}	6.5		mA
Output minimum sink current	I_{OL} at V_{OL}	–6.5		mA
DDR3/SSTL15 Class II (DDR3 Full Drive)				
DC output logic high	V_{OH}	0.8 × V_{DDI}		V
DC output logic low	V_{OL}		0.2 × V_{DDI}	V
Output minimum source DC current	I_{OH} at V_{OH}	7.6		mA
Output minimum sink current	I_{OL} at V_{OL}	–7.6		mA

Table 132 • **SSTL15 DC Differential Voltage Specification (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID}	0.2	V

Note: To meet JEDEC electrical compliance, use DDR3 full drive transmitter.

Table 133 • **SSTL15 AC SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF} (AC)	0.3		V
AC differential cross point voltage	V_x (AC)	0.5 × V_{DDI} – 0.150	0.5 × V_{DDI} + 0.150	V

Table 134 • **SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	667	Mbps	AC loading: per JEDEC specifications

Table 135 • **SSTL15 AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	R_{REF}	34, 40	Ω	Reference resistor = 240 Ω
Effective impedance value (ODT)	R_{TT}	20, 30, 40, 60, 120	Ω	Reference resistor = 240 Ω

Table 150 • **LPDDR Full Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

	T_{DP}		T_{ENZL}		T_{ENZH}		T_{ENHZ}		T_{ENLZ}		
	–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.171	2.555	2.17	2.554	ns
Differential	2.298	2.703	2.288	2.692	2.288	2.692	2.593	3.051	2.593	3.051	ns

Minimum and Maximum DC/AC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode

Table 151 • **LPDDR-LVCMOS 1.8 V Mode Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.710	1.8	1.89	V

Table 152 • **LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	V_{IH} (DC)	0.65 × V_{DDI}	1.89	V
DC input logic high (for MSIO I/O bank)	V_{IH} (DC)	0.65 × V_{DDI}	3.45	V
DC input logic low	V_{IL} (DC)	–0.3	0.35 × V_{DDI}	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

1. See Table 24, page 22.

Table 153 • **LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	V_{DDI} – 0.45		V
DC output logic low	V_{OL}		0.45	V

Table 154 • **LPDDR-LVCMOS 1.8 V Minimum and Maximum AC Switching Speeds**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	400	Mbps	AC loading: 17pf load, 8 ma drive and above/all slew

Table 155 • **LPDDR-LVCMOS 1.8 V Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CAL	75, 60, 50, 33, 25, 20	Ω

Table 162 • **LVDS DC Output Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 163 • **LVDS DC Differential Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
Differential output voltage swing	V_{OD}	250	350	450	mV
Output common mode voltage	V_{OCM}	1.125	1.25	1.375	V
Input common mode voltage	V_{ICM}	0.05	1.25	2.35	V
Input differential voltage	V_{ID}	100	350	600	mV

Table 164 • **LVDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	535	Mbps	AC loading: 12 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank) no pre-emphasis	D_{MAX}	620	Mbps	AC loading: 10 pF / 100 Ω differential load
		700	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 165 • **LVDS AC Impedance Specifications**

Parameter	Symbol	Typ	Max	Unit
Termination resistance	RT	100		Ω

Table 166 • **LVDS AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF

LVDS25 AC Switching Characteristics

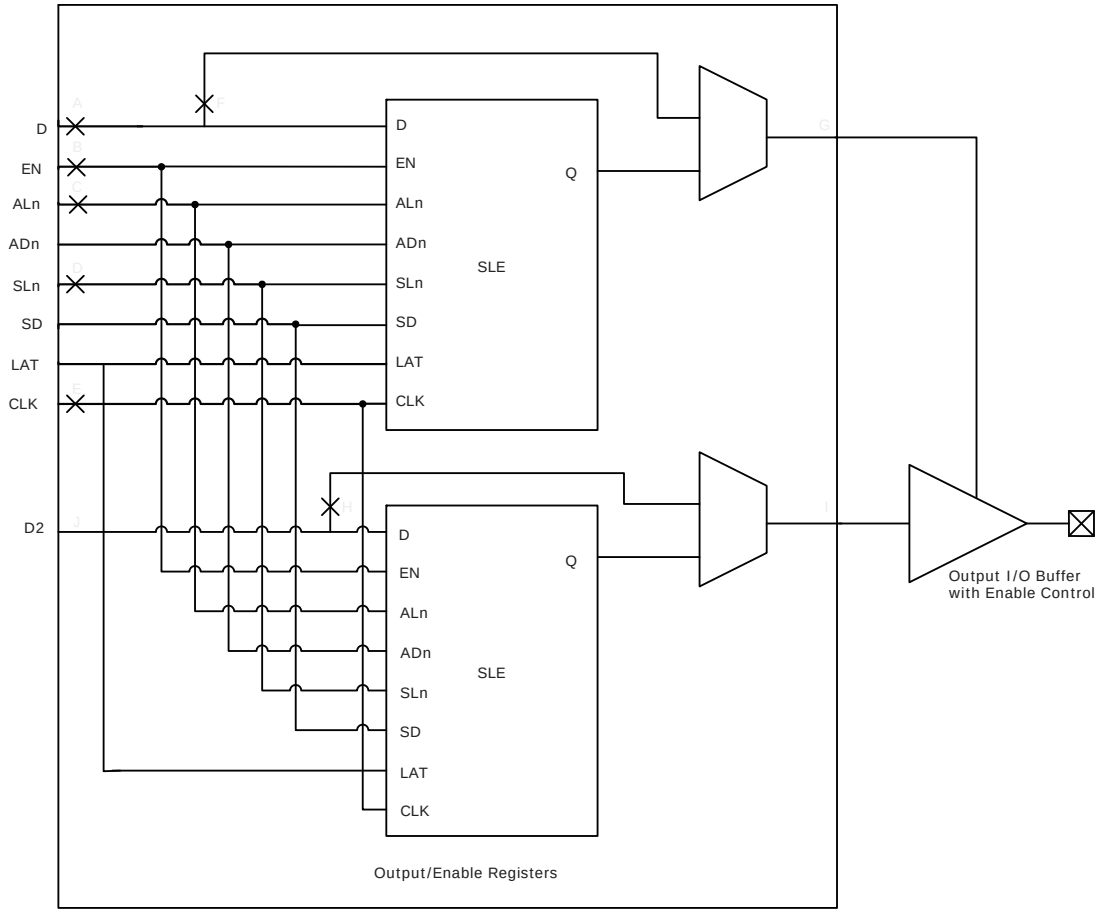
Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V

Table 167 • **LVDS25 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.774	3.263	ns
100	2.775	3.264	ns

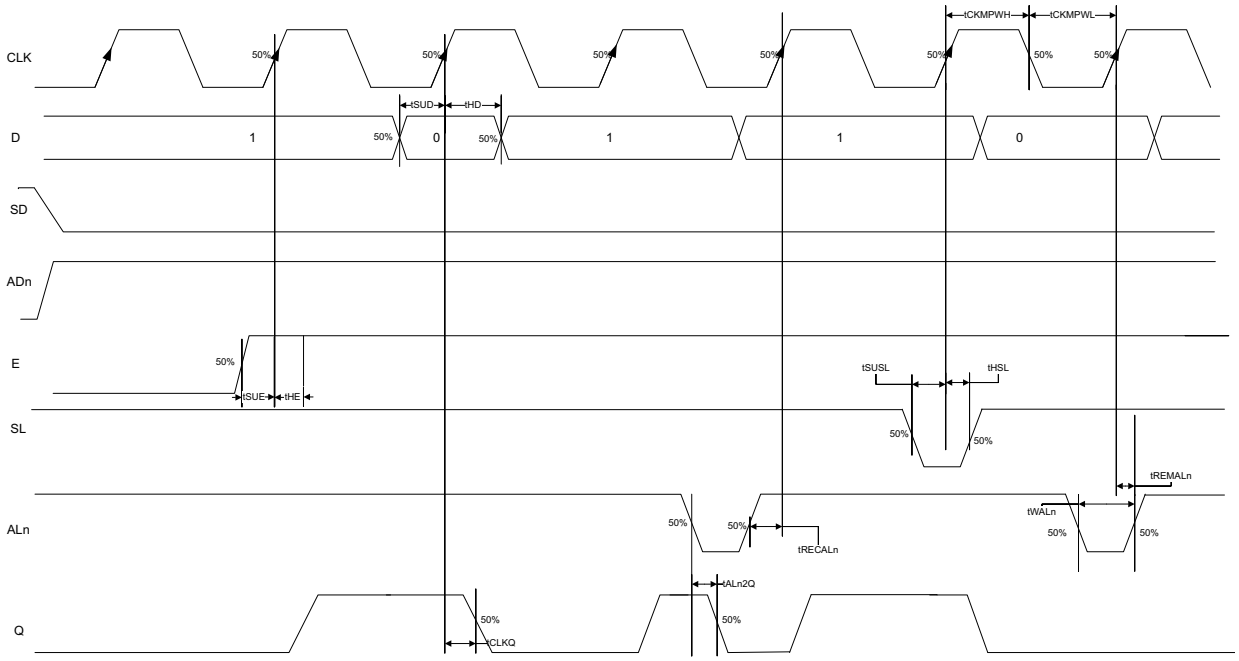
2.3.8.2 Output/Enable Register

Figure 8 • Timing Model for Output/Enable Register



The following figure shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

Figure 16 • **Sequential Module Timing Diagram**



2.3.10.3.1 Timing Characteristics

The following table lists the register delays in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 224 • **Register Delays**

Parameter	Symbol	–1	–Std	Unit
Clock-to-Q of the core register	T_{CLKQ}	0.108	0.127	ns
Data setup time for the core register	T_{SUD}	0.254	0.298	ns
Data hold time for the core register	T_{HD}	0	0	ns
Enable setup time for the core register	T_{SUE}	0.335	0.394	ns
Enable hold time for the core register	T_{HE}	0	0	ns
Synchronous load setup time for the core register	T_{SUSL}	0.335	0.394	ns
Synchronous load hold time for the core register	T_{HSL}	0	0	ns
Asynchronous Clear-to-Q of the core register (ADn = 1)	T_{ALN2Q}	0.473	0.556	ns
Asynchronous preset-to-Q of the core register (ADn = 0)		0.451	0.531	ns
Asynchronous load removal time for the core register	T_{REMALN}	0	0	ns
Asynchronous load recovery time for the core register	T_{RECALN}	0.353	0.415	ns
Asynchronous load minimum pulse width for the core register	T_{WALN}	0.266	0.313	ns
Clock minimum pulse width high for the core register	T_{CKMPWH}	0.065	0.077	ns
Clock minimum pulse width low for the core register	T_{CKMPWL}	0.139	0.164	ns

Table 232 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 *(continued)***

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Address setup time	T_{ADDRSU}	0.475		0.559		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.336		0.395		ns
Data hold time	T_{DHD}	0.082		0.096		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		1.529		1.799	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.485		0.57		ns
Read enable hold time	T_{RDEHD}	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}		1.514		1.781	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.415		0.488		ns
Write enable hold time	T_{WEHD}	0.048		0.057		ns
Maximum frequency	F_{MAX}		400		340	MHz

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 233 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns

Table 233 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4 *(continued)***

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register	T_{CLK2Q}		0.323		0.38	ns
Read access time without pipeline register			2.273		2.673	ns
Access time with feed-through write timing			1.511		1.778	ns
Address setup time	T_{ADDRSU}	0.543		0.638		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.334		0.393		ns
Data hold time	T_{DHD}	0.082		0.096		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		1.511		1.778	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.516		0.607		ns
Read enable hold time	T_{RDEHD}	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}		1.507		1.773	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.458		0.539		ns
Write enable hold time	T_{WEHD}	0.048		0.057		ns
Maximum frequency	F_{MAX}		400		340	MHz

Table 240 • **µSRAM (RAM128x8) in 128 × 8 Mode *(continued)***

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		–0.778		–0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.982	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

Table 243 • **µSRAM (RAM1024x1) in 1024 × 1 Mode *(continued)***

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.83		0.98	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.003		0.004		ns
Write input data hold time	T_{DINCHD}	0.137		0.161		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.247		0.29		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.03		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

2.3.13 Programming Times

The following tables list the programming times in typical conditions when T_J = 25 °C, V_{DD} = 1.2 V. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 244 • **JTAG Programming (Fabric Only)**

M2S/M2GL Device	**Image size Bytes**	**Program**	**Verify**	**Unit**
005	302672	22	10	Sec
010	568784	28	18	Sec
025	1223504	51	26	Sec
050	2424832	66	54	Sec
060	2418896	77	54	Sec
090	3645968	113	126	Sec
150	6139184	155	193	Sec

Table 254 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only) *(continued)*

M2S/M2GL Device	Auto Programming 100 kHz	Auto Update 25 MHz	Programming Recovery 12.5 MHz	Unit
150	161	161	161	Sec

Table 255 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)

M2S/M2GL Device	Auto Programming 100 kHz	Auto Update 25 MHz	Programming Recovery 12.5 MHz	Unit
005	47	27	28	Sec
010	77	35	35	Sec
025	150	42	41	Sec
050	33[1]	Not Supported	Not Supported	Sec
060	291	83	82	Sec
090	427	109	108	Sec
150	708	157	160	Sec
005	41	48	49	Sec
010	86	87	87	Sec
025	87	85	86	Sec
050	85	Not Supported	Not Supported	Sec
060	78	86	86	Sec
090	154	162	162	Sec
150	161	161	161	Sec
005	87	67	66	Sec
010	161	113	113	Sec
025	229	120	121	Sec
050	112	Not Supported	Not Supported	Sec
060	368	161	158	Sec
090	582	261	260	Sec
150	867	309	310	Sec

1. Auto Programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

Table 262 • **SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	302672	6	41	8	Sec
010	568784	10	48	14	Sec
025	1223504	21	61	29	Sec
050	2424832	39	82	50	Sec
060	2418896	44	87	54	Sec
090	3645968	66	112	79	Sec
150	6139184	108	162	128	Sec

Table 263 • **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	137536	3	64	4	Sec
010	274816	4	104	7	Sec
025	274816	4	104	8	Sec
050	2,78,528	4	102	8	Sec
060	268480	6	102	8	Sec
090	544496	10	179	15	Sec
150	544496	10	180	15	Sec

Table 264 • **SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	9	83	11	Sec
010	842688	15	129	21	Sec
025	1497408	26	143	35	Sec
050	2695168	43	163	55	Sec
060	2686464	48	165	60	Sec
090	4190208	75	266	91	Sec
150	6682768	117	318	141	Sec

Table 293 • **Flash*Freeze Entry and Exit Times *(continued)***

		Entry/Exit Timing FCLK = 100MHz		Entry/Exit Timing FCLK = 3 MHz		
Parameter	**Symbol**	**005, 010, 025, 060, 090, and 150**	**050**	**All Devices**	**Unit**	**Conditions**
Exit time with respect to the fabric PLL lock[1]	TFF_EXIT	1.5	1.5	1.5	ms	eNVM and MSS/HPMS PLL = ON during F*F
		1.5	1.5	1.5	ms	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit
Exit time with respect to the fabric buffer output	TFF_EXIT	21	15	21	µs	eNVM and MSS/HPMS PLL = ON during F*F
		65	55	65	µs	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit

1. PLL Lock Delay set to 1024 cycles (default).

2.3.28 DDR Memory Interface Characteristics

The following table lists the DDR memory interface characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 294 • **DDR Memory Interface Characteristics**

	Supported Data Rate		
Standard	**Min**	**Max**	**Unit**
DDR3	667	667	Mbps
DDR2	667	667	Mbps
LPDDR	50	400	Mbps

2.3.29 SFP Transceiver Characteristics

IGLOO2 and SmartFusion2 SerDes complies with small form-factor pluggable (SFP) requirements as specified in SFP INF-80741. The following table provides the electrical characteristics.

The following table lists the SFP transceiver electrical characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 295 • **SFP Transceiver Electrical Characteristics**

		Differential Peak-Peak Voltage		
Pin	**Direction**	**Min**	**Max**	**Unit**
RD+/-[1]	Output	1600	2400	mV
TD+/-[2]	Input	350	2400	mV

1. Based on default SerDes transmitter settings for PCIe Gen1. Lower amplitudes are available through programming changes to TX_AMP setting.
2. Based on Input Voltage Common-Mode (VICM) = 0 V. Requires AC Coupling.