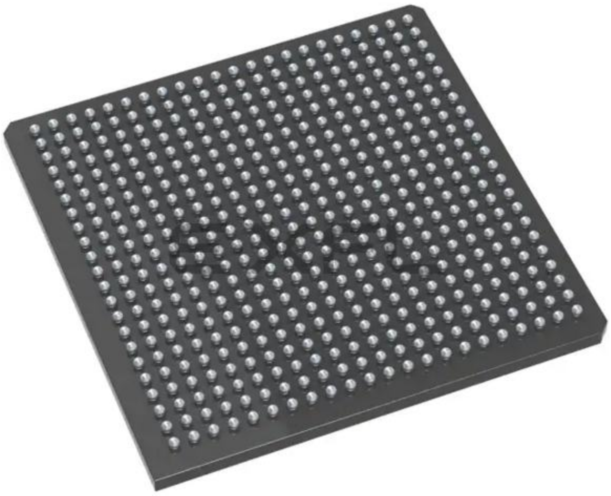
Microchip Technology - M2S010TS-1FGG484 Datasheet



Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 10K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s010ts-1fgg484

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2.2 References

The following documents are recommended references:

- *PB0121: IGLOO2 Product Brief*
- *DS0124: IGLOO2 Pin Descriptions*
- *PB0115: SmartFusion2 SoC FPGA Product Brief*
- *DS0115: SmartFusion2 Pin Descriptions*

All product documentation for IGLOO2 and SmartFusion2 is available at:
http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga
http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#overview

2.3 Electrical Specifications

2.3.1 Operating Conditions

The following table lists the stress limits. Stress applied above the specified limit may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table are not implied.

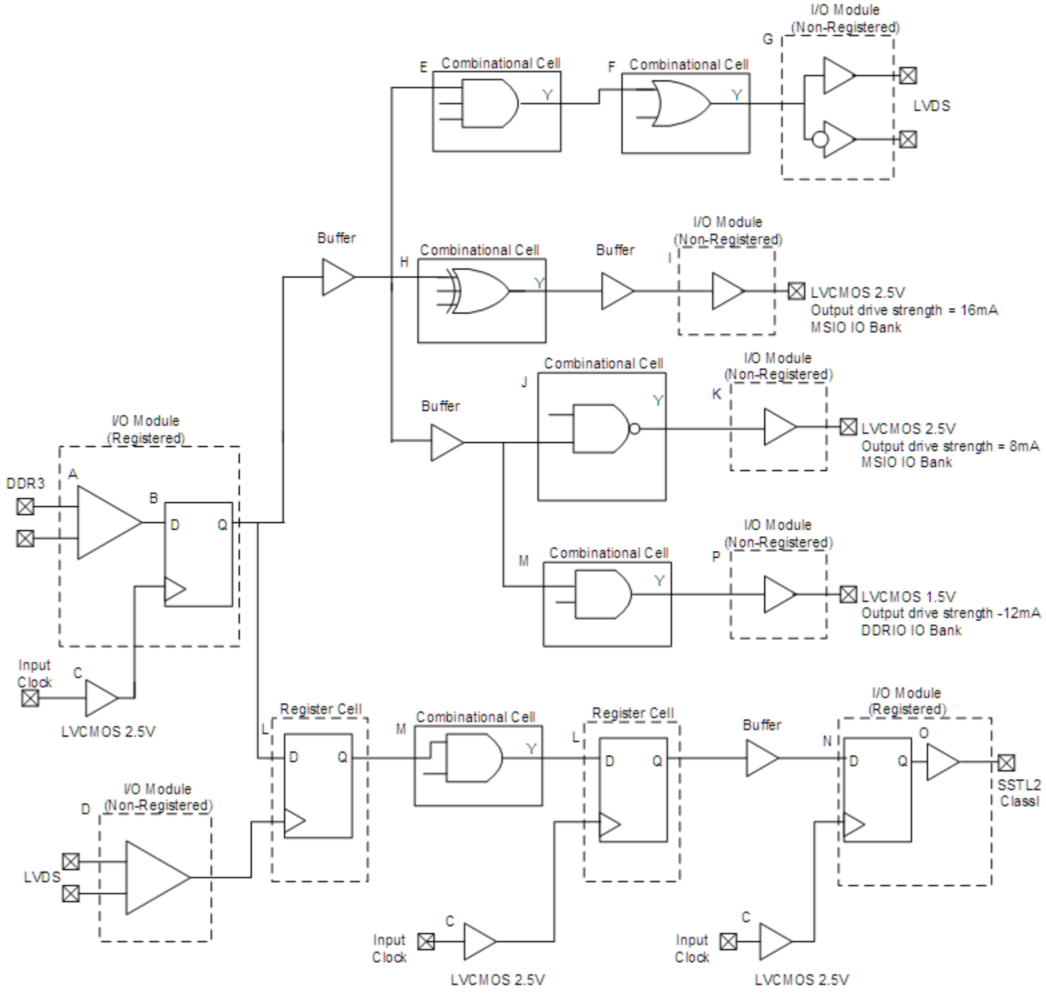
Table 3 • **Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Unit
DC core supply voltage. Must always power this pin.	V_{DD}	–0.3	1.32	V
Power supply for charge pumps (for normal operation and programming). Must always power this pin.	V_{PP}	–0.3	3.63	V
Analog power pad for MDDR PLL	MSS_MDDR_PLL_VDDA	–0.3	3.63	V
Analog power pad for MDDR PLL	HPMS_MDDR_PLL_VDDA	–0.3	3.63	V
Analog power pad for FDDR PLL	FDDR_PLL_VDDA	–0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_MSS_MDDR_VDDA	–0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_HPMS_MDDR_VDDA	–0.3	3.63	V
Analog power pad for PLL0–5	CCC_XX[01]_PLL_VDDA	–0.3	3.63	V
High supply voltage for PLL SerDes[01]	SERDES_[01]_PLL_VDDA	–0.3	3.63	V
Analog power for SerDes[01] PLL lane0 to lane3. This is a 2.5 V SerDes internal PLL supply.	SERDES_[01]_L[0123]_VDDAPLL	–0.3	2.75	V
TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply.	SERDES_[01]_L[0123]_VDDAIO	–0.3	1.32	V
PCIe/PCS power supply	SERDES_[01]_VDD	–0.3	1.32	V
DC FPGA I/O buffer supply voltage for MSIO I/O bank	V_{DDIx}	–0.3	3.63	V
DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks	V_{DDIx}	–0.3	2.75	V
I/O Input voltage for MSIO I/O bank	V_I	–0.3	3.63	V
I/O Input voltage for MSIOD/DDRIO I/O bank	V_I	–0.3	2.75	V
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to V_{PP}.	V_{PPNVM}	–0.3	3.63	V
Storage temperature[1]	T_{STG}	–65	150	°C
Junction temperature	T_J	–55	135	°C

2.3.4 Timing Model

This section describes timing model and timing parameters.

Figure 2 • **Timing Model**



The following table lists the timing model parameters in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

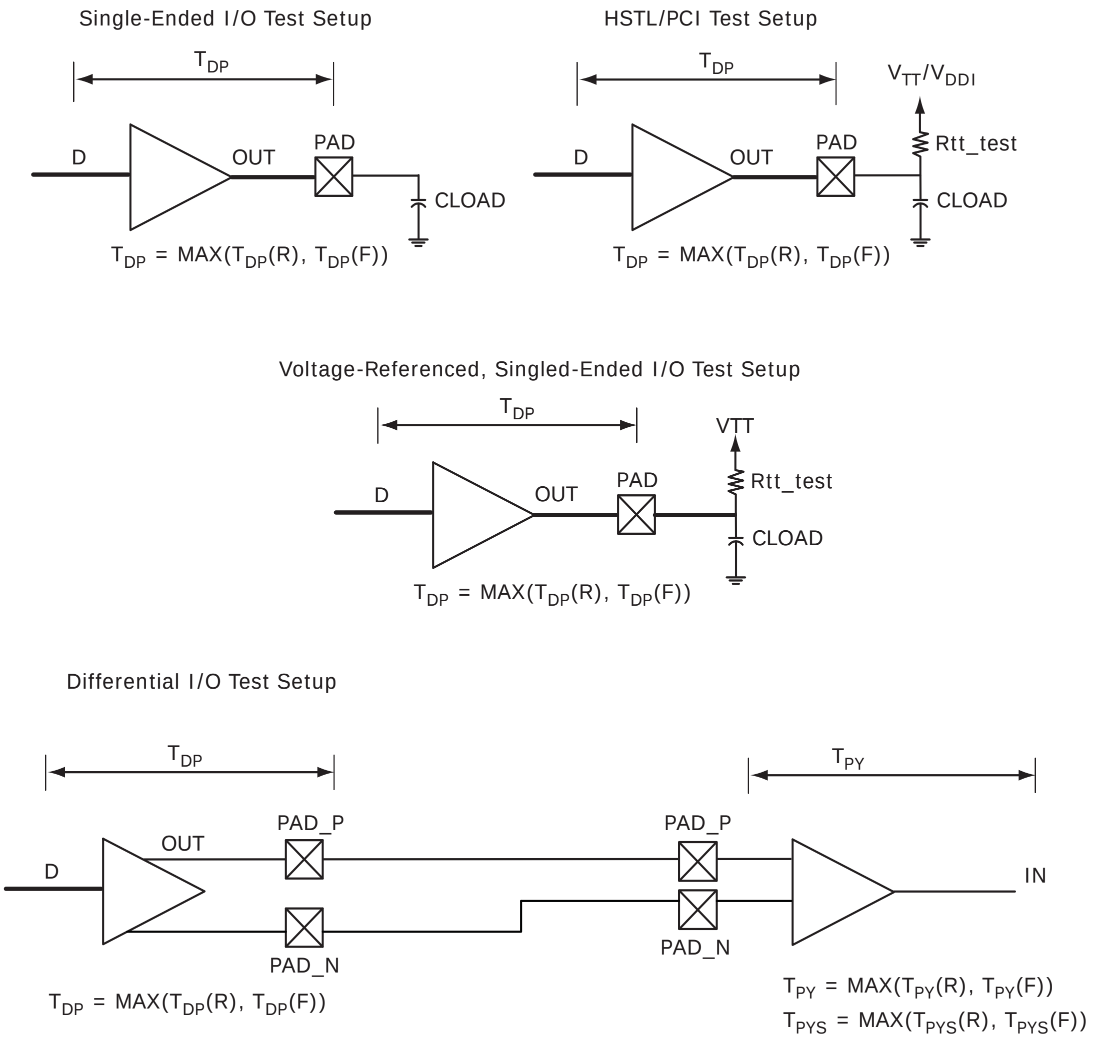
Table 17 • **Timing Model Parameters**

Index	Symbol	Description	–1	Unit	For More Information
A	T_{PY}	Propagation delay of DDR3 receiver	1.605	ns	See Table 137, page 50
B	T_{ICLKQ}	Clock-to-Q of the input data register	0.16	ns	See Table 221, page 71
	T_{ISUD}	Setup time of the input data register	0.357	ns	See Table 221, page 71
C	T_{RCKH}	Input high delay for global clock	1.53	ns	See Table 227, page 78
	T_{RCKL}	Input low delay for global clock	0.897	ns	See Table 227, page 78
D	T_{PY}	Input propagation delay of LVDS receiver	2.774	ns	See Table 167, page 56
E	T_{DP}	Propagation delay of a three-input AND gate	0.198	ns	See Table 223, page 76

2.3.5.2 Output Buffer and AC Loading

The following figure shows the output buffer and AC loading.

Figure 4 • **Output Buffer AC Loading**



2.3.5.6 Single-Ended I/O Standards

2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 29 • **LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

Table 30 • **LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC input logic high	V_{IH} (DC)	2.0	3.45	V
DC input logic low	V_{IL} (DC)	–0.3	0.8	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

1. See Table 24, page 22.

Table 31 • **LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC output logic high[1]	V_{OH}	V_{DDI} – 0.4		V
DC output logic low[1]	V_{OL}		0.4	V

1. The V_{OH}/V_{OL} test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

Table 32 • **LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	2.4		V
DC output logic low	V_{OL}		0.4	V

Table 33 • **LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	600	Mbps	AC loading: 17 pF load, maximum drive/slew

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 3.0 V

Table 91 • **PCI/PCIX AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)**

	T_{PY}		T_{PYS}		
On-Die Termination (ODT)	**–1**	**–Std**	**–1**	**–Std**	**Unit**
None	2.229	2.623	2.238	2.633	ns

Table 92 • **PCI/PCIX AC switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)**

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
2.146	2.525	2.043	2.404	2.084	2.452	6.095	7.171	5.558	6.539	ns

2.3.6 Memory Interface and Voltage Referenced I/O Standards

This section describes High-Speed Transceiver Logic (HSTL) memory interface and voltage reference I/O standards.

2.3.6.1 High-Speed Transceiver Logic (HSTL)

The HSTL standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO2 FPGA and SmartFusion2 SoC FPGA devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification (Applicable to DDRIO Bank Only)

Table 93 • **HSTL Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.425	1.5	1.575	V
Termination voltage	V_{TT}	0.698	0.750	0.803	V
Input reference voltage	V_{REF}	0.698	0.750	0.803	V

Table 94 • **HSTL DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high	V_{IH} (DC)	V_{REF} + 0.1	1.575	V
DC input logic low	V_{IL} (DC)	–0.3	V_{REF} – 0.1	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

[1] See Table 24, page 22.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V.

Table 210 • **RSDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.855	3.359	ns
100	2.85	3.353	ns

Table 211 • **RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.602	3.061	ns
100	2.597	3.055	ns

Table 212 • **RSDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
2.097	2.467	2.303	2.709	2.291	2.695	1.961	2.307	1.947	2.29	ns

Table 213 • **RSDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
	–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
No pre-emphasis	1.614	1.899	1.559	1.834	1.55	1.823	1.59	1.87	1.575	1.852	ns
Min pre-emphasis	1.604	1.887	1.742	2.05	1.728	2.032	1.889	2.222	1.858	2.185	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

2.3.7.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

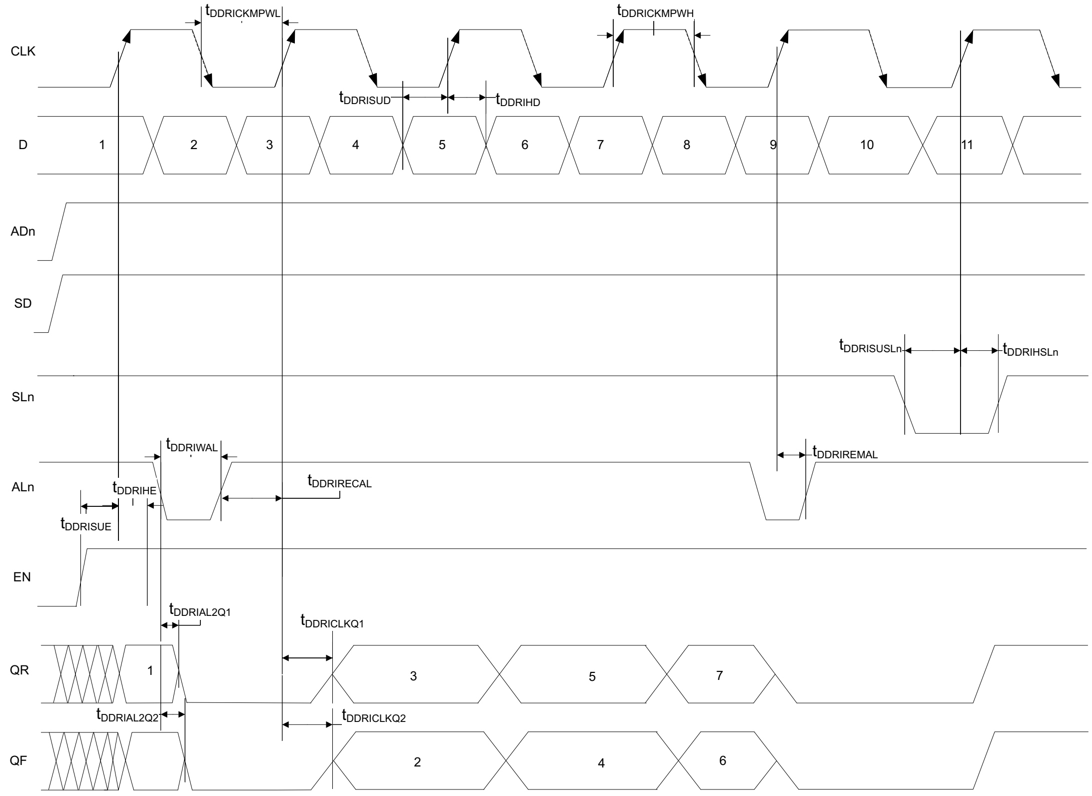
Minimum and Maximum Input and Output Levels (Applicable to MSIO I/O Bank Only)

Table 214 • **LVPECL Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

2.3.9.2 Input DDR Timing Diagram

Figure 11 • **Input DDR Timing Diagram**



2.3.9.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

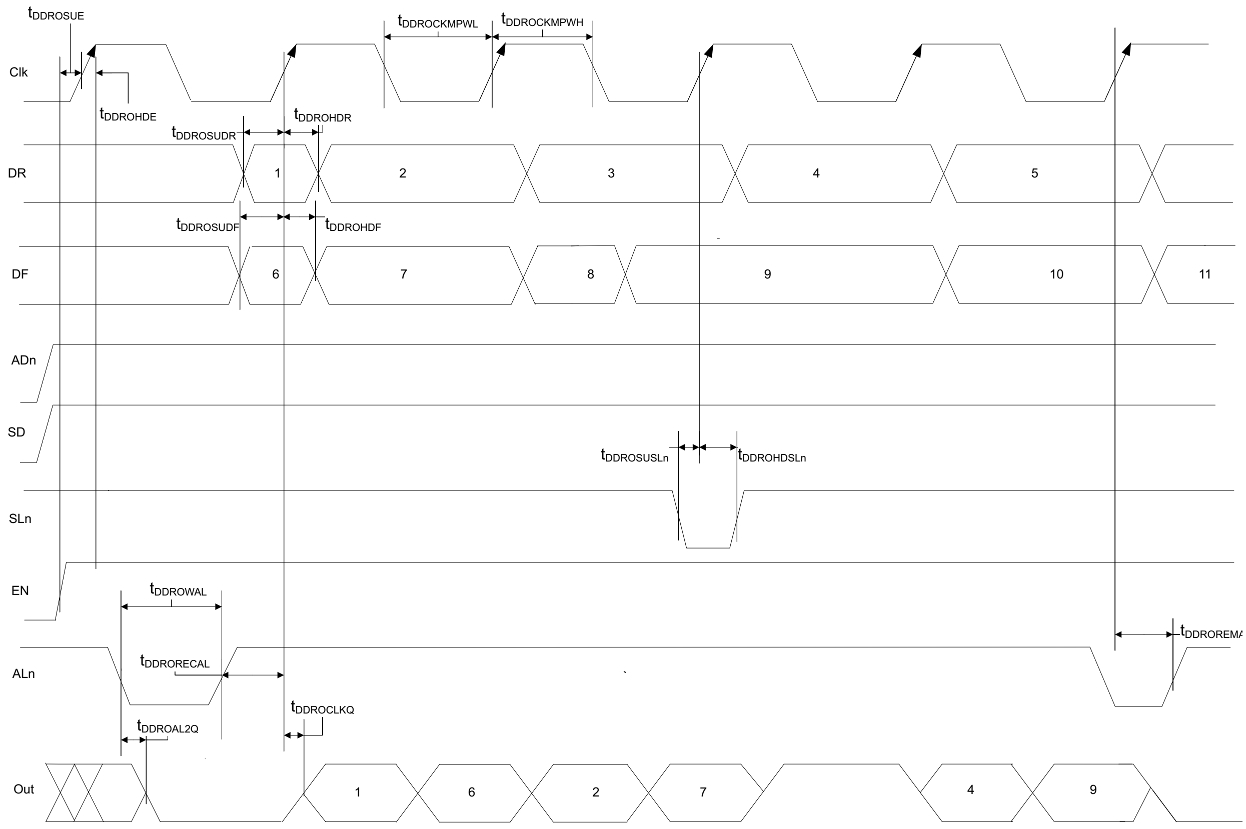
Table 221 • **Input DDR Propagation Delays**

Symbol	Description	Measuring Nodes (from, to)	–1	–Std	Unit
$T_{DDRICLKQ1}$	Clock-to-Out Out_QR for input DDR	B, C	0.16	0.188	ns
$T_{DDRICLKQ2}$	Clock-to-Out Out_QF for input DDR	B, D	0.166	0.195	ns
$T_{DDRISUD}$	Data setup for input DDR	A, B	0.357	0.421	ns
T_{DDRIHD}	Data hold for input DDR	A, B	0	0	ns
$T_{DDRISUE}$	Enable setup for input DDR	E, B	0.46	0.542	ns
T_{DDRIHE}	Enable hold for input DDR	E, B	0	0	ns
$T_{DDRISUSLN}$	Synchronous load setup for input DDR	G, B	0.46	0.542	ns
$T_{DDRIHSLN}$	Synchronous load hold for input DDR	G, B	0	0	ns
$T_{DDRIAL2Q1}$	Asynchronous load-to-out QR for input DDR	F, C	0.587	0.69	ns
$T_{DDRIAL2Q2}$	Asynchronous load-to-out QF for input DDR	F, D	0.541	0.636	ns
$T_{DDRIREMAL}$	Asynchronous load removal time for input DDR	F, B	0	0	ns
$T_{DDRIRECAL}$	Asynchronous load recovery time for input DDR	F, B	0.074	0.087	ns

Table 221 • **Input DDR Propagation Delays *(continued)***

Symbol	**Description**	**Measuring Nodes (from, to)**	**–1**	**–Std**	**Unit**
$T_{DDRIWAL}$	Asynchronous load minimum pulse width for input DDR	F, F	0.304	0.357	ns
$T_{DDRICKMPWH}$	Clock minimum pulse width high for input DDR	B, B	0.075	0.088	ns
$T_{DDRICKMPWL}$	Clock minimum pulse width low for input DDR	B, B	0.159	0.187	ns

Figure 13 • Output DDR Timing Diagram



2.3.9.5 Timing Characteristics

The following table lists the output DDR propagation delays in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 222 • Output DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	–1	–Std	Unit
$T_{DDROCLKQ}$	Clock-to-out of DDR for output DDR	E, G	0.263	0.309	ns
$T_{DDROSUDF}$	Data_F data setup for output DDR	F, E	0.143	0.168	ns
$T_{DDROSUDR}$	Data_R data setup for output DDR	A, E	0.19	0.223	ns
$T_{DDROHDF}$	Data_F data hold for output DDR	F, E	0	0	ns
$T_{DDROHDR}$	Data_R data hold for output DDR	A, E	0	0	ns
$T_{DDROSUE}$	Enable setup for input DDR	B, E	0.419	0.493	ns
T_{DDROHE}	Enable hold for input DDR	B, E	0	0	ns
$T_{DDROSUSLN}$	Synchronous load setup for input DDR	D, E	0.196	0.231	ns
$T_{DDROHSLN}$	Synchronous load hold for input DDR	D, E	0	0	ns
$T_{DDROAL2Q}$	Asynchronous load-to-out for output DDR	C, G	0.528	0.621	ns
$T_{DDROREMAL}$	Asynchronous load removal time for output DDR	C, E	0	0	ns
$T_{DDRORECAL}$	Asynchronous load recovery time for output DDR	C, E	0.034	0.04	ns

Table 222 • **Output DDR Propagation Delays *(continued)***

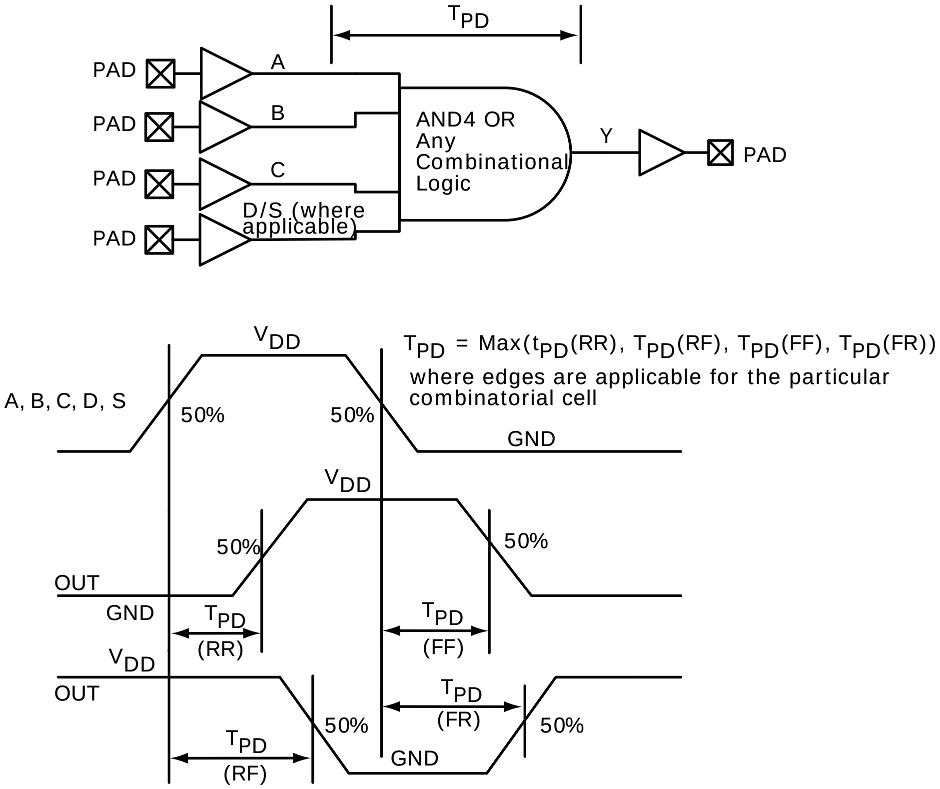
Symbol	Description	Measuring Nodes (from, to)	–1	–Std	Unit
$T_{DDROWAL}$	Asynchronous load minimum pulse width for output DDR	C, C	0.304	0.357	ns
$T_{DDROCKMPWH}$	Clock minimum pulse width high for the output DDR	E, E	0.075	0.088	ns
$T_{DDROCKMPWL}$	Clock minimum pulse width low for the output DDR	E, E	0.159	0.187	ns

2.3.10 Logic Element Specifications

2.3.10.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, see *SmartFusion2 and IGLOO2 Macro Library Guide*.

Figure 14 • **LUT-4**



The following table lists the RAM1K18 – dual-port mode for depth × width configuration 8K × 2 in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 234 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2**

		–1		**–Std**		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register	T_{CLK2Q}		0.32		0.377	ns
Read access time without pipeline register			2.272		2.673	ns
Access time with feed-through write timing			1.511		1.778	ns
Address setup time	T_{ADDRSU}	0.612		0.72		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.33		0.388		ns
Data hold time	T_{DHD}	0.082		0.096		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		1.511		1.778	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.529		0.622		ns
Read enable hold time	T_{RDEHD}	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}		1.528		1.797	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.488		0.574		ns
Write enable hold time	T_{WEHD}	0.048		0.057		ns
Maximum frequency	F_{MAX}		400		340	MHz

Table 237 • **µSRAM (RAM64x18) in 64 × 18 Mode *(continued)***

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the µSRAM in 64 × 16 mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 238 • **µSRAM (RAM64x16) in 64 × 16 Mode**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		–0.778		–0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.983	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns

Table 239 • **µSRAM (RAM128x9) in 128 × 9 Mode *(continued)***

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.982	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the µSRAM in 128 × 8 mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 240 • **µSRAM (RAM128x8) in 128 × 8 Mode**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns

The following table lists the programming times in worst-case conditions when T_J = 100 °C, V_{DD} = 1.14 V. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 256 • **JTAG Programming (Fabric Only)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	302672	44	10	Sec
010	568784	50	18	Sec
025	1223504	73	26	Sec
050	2424832	88	54	Sec
060	2418896	99	54	Sec
090	3645968	135	126	Sec
150	6139184	177	193	Sec

Table 257 • **JTAG Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	137536	61	4	Sec
010	274816	100	9	Sec
025	274816	100	9	Sec
050	2,78,528	106	8	Sec
060	268480	98	8	Sec
090	544496	176	15	Sec
150	544496	177	15	Sec

Table 258 • **JTAG Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	439296	71	11	Sec
010	842688	129	20	Sec
025	1497408	142	35	Sec
050	2695168	184	59	Sec
060	2686464	180	70	Sec
090	4190208	288	147	Sec
150	6682768	338	231	Sec

2.3.14 Math Block Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC math block supports 18×18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently. The following table lists the math blocks with all registers used in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 268 • **Math Blocks with all Registers Used**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input, control register setup time	T_{MISU}	0.149		0.176		ns
Input, control register hold time	T_{MIHD}	1.68		1.976		ns
CDIN input setup time	$T_{MOCDINSU}$	0.185		0.218		ns
CDIN input hold time	$T_{MOCDINHD}$	0.08		0.094		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	–0.419		–0.493		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	0.011		0.013		ns
Asynchronous reset removal time	$T_{MARSTREM}$	0		0		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.088		0.104		ns
Output register clock to out delay	T_{MOCQ}		0.232		0.273	ns
CLK minimum period	T_{MCLKMP}	2.245		2.641		ns

The following table lists the math blocks with input bypassed and output registers used in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 269 • **Math Block with Input Bypassed and Output Registers Used**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Output register setup time	T_{MOSU}	2.294		2.699		ns
Output register hold time	T_{MOHD}	1.68		1.976		ns
CDIN input setup time	$T_{MOCDINSU}$	0.115		0.136		ns
CDIN input hold time	$T_{MOCDINHD}$	–0.444		–0.522		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	–0.419		–0.493		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	0.011		0.013		ns
Asynchronous reset removal time	$T_{MARSTREM}$	0		0		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.014		0.017		ns
Output register clock to out delay	T_{MOCQ}		0.232		0.273	ns
CLK minimum period	T_{MCLKMP}	2.179		2.563		ns

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 270 • **Math Block with Input Register Used and Output in Bypass Mode**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input register setup time	T_{MISU}	0.149		0.176		ns
Input register hold time	T_{MIHD}	0.185		0.218		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	0.08		0.094		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	–0.012		–0.014		ns
Asynchronous reset removal time	$T_{MARSTREM}$	–0.005		–0.005		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.088		0.104		ns
Input register clock to output delay	T_{MICQ}		2.52		2.964	ns
CDIN to output delay	$T_{MCDIN2Q}$		1.951		2.295	ns

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 271 • **Math Block with Input and Output in Bypass Mode**

		–1	–Std	
Parameter	**Symbol**	**Max**	**Max**	**Unit**
Input to output delay	T_{MIQ}	2.568	3.022	ns
CDIN to output delay	$T_{MCDIN2Q}$	1.951	2.295	ns

2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when V_{DD} = 1.14 V, V_{PPNVM} = V_{PP} = 2.375 V.

Table 272 • **eNVM Read Performance**

		Operating Temperature Range						
Symbol	**Description**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
T_J	Junction temperature range	–55 °C to 125 °C		–40 °C to 100 °C		0 °C to 85 °C		°C
$F_{MAXREAD}$	eNVM maximum read frequency	25	25	25	25	25	25	MHz

The following table lists the eNVM page programming in worst-case conditions when V_{DD} = 1.14 V, V_{PPNVM} = V_{PP} = 2.375 V.

Table 273 • **eNVM Page Programming**

		Operating Temperature Range						
Symbol	**Description**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
T_J	Junction temperature range	–55 °C to 125 °C		–40 °C to 100 °C		0 °C to 85 °C		°C
$T_{PAGEPGM}$	eNVM page programming time	40	40	40	40	40	40	ms

1. The minimum output clock frequency is limited by the PLL. For more information, see *UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide*.
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance is limited by the CCC output frequency.

The following table lists the CCC/PLL jitter specifications in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 283 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications**

CCC Output Maximum Peak-to-Peak Period Jitter F_{OUT_CCC}						
Parameter	**Conditions/Package Combinations**					**Unit**
10 FG484, 050 FG896/FG484/FCS325 Packages[1]	SSO = 0	0 < SSO <= 2	SSO <= 4	SSO <= 8	SSO <= 16	
20 MHz to 100 MHz	Max(110, ± 1% x (1/F_{OUT_CCC}))	Max(150, ± 1% x (1/F_{OUT_CCC}))				ps
100 MHz to 400 MHz	Max(120, ± 1% x (1/F_{OUT_CCC}))	Max(150, ± 1% x (1/F_{OUT_CCC}))			Max(170, ± 1% x (1/F_{OUT_CCC}))	ps
025 FG484/FCS325 Package[1]	0 < SSO <=16					
20 MHz to 74 MHz	± 1% x (1/F_{OUT_CCC}))					ps
74 MHz to 400 MHz	210					ps
005 FG484 Package[1]	0 < SSO <=16					
20 MHz to 53 MHz	± 1% x (1/F_{OUT_CCC}))					ps
53 MHz to 400 MHz	270					ps
090 FG676 and FC325 Package[1]	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x (1/F_{OUT_CCC}))					ps
100 MHz to 400 MHz	150					ps
060 FG676 Package[1]	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x (1/F_{OUT_CCC})					ps
100 MHz to 400 MHz	150					
150 FC1152 Package[1]	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x (1/F_{OUT_CCC}))					ps
100 MHz to 400 MHz	120					ps

1. SSO data is based on LVCMOS 2.5 V MSIO and/or MSIOD bank I/Os.