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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 25K Logic Modules
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s025-vfg256i

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Table 11 • SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD} = 1.2\text{ V}$) – Typical Process

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC2	Flash*Freeze	1.4	2.6	3.7	5.1	5.0	5.1	8.9	mA	Typical ($T_J = 25\text{ }^\circ\text{C}$)
		12.0	20.0	26.6	35.3	35.4	35.7	57.8	mA	Commercial ($T_J = 85\text{ }^\circ\text{C}$)
		18.5	30.8	41.0	54.5	54.5	55.0	89.0	mA	Industrial ($T_J = 100\text{ }^\circ\text{C}$)

Table 12 • SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD} = 1.26\text{ V}$) – Worst-Case Process

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC1	Non-Flash*Freeze	43.8	57.0	84.6	132.3	161.4	163.0	242.5	mA	Commercial ($T_J = 85\text{ }^\circ\text{C}$)
		65.3	85.7	127.8	200.9	245.4	247.8	369.0	mA	Industrial ($T_J = 100\text{ }^\circ\text{C}$)
IDC2	Flash*Freeze	29.1	45.6	51.7	62.7	69.3	70.0	84.8	mA	Commercial ($T_J = 85\text{ }^\circ\text{C}$)
		44.9	70.3	79.7	96.5	106.8	107.8	130.6	mA	Industrial ($T_J = 100\text{ }^\circ\text{C}$)

2.3.2.2 Programming Currents

The following tables represent programming, verify and Inrush currents for SmartFusion2 SoC and IGLOO2 FPGA devices.

Table 13 • Currents During Program Cycle, $0\text{ }^\circ\text{C} \leq T_J \leq 85\text{ }^\circ\text{C}$ – Typical Process

Power Supplies	Voltage (V)	005	010	025	050	060	090	150 ¹	Unit
V_{DD}	1.26	46	53	55	58	30	42	52	mA
V_{PP}	3.46	8	11	6	10	9	12	12	mA
V_{PPNVM}	3.46	1	2	2	3	3	3		mA
V_{DDI}	2.62	31	16	17	1	12	12	81	mA
	3.46	62	31	36	1	12	17	84	mA
Number of banks		7	8	8	10	10	9	19	

1. V_{PP} and V_{PPNVM} are internally shorted.

Table 14 • Currents During Verify Cycle, $0\text{ }^\circ\text{C} \leq T_J \leq 85\text{ }^\circ\text{C}$ – Typical Process

Power Supplies	Voltage (V)	005	010	025	050	060	090	150 ¹	Unit
V_{DD}	1.26	44	53	55	58	33	41	51	mA
V_{PP}	3.46	6	5	3	15	8	11	12	mA
V_{PPNVM}	3.46	1	0	0	1	1	1		mA
V_{DDI}	2.62	31	16	17	1	12	11	81	mA
	3.46	61	32	36	1	12	17	84	mA
Number of banks		7	8	8	10	10	9	19	

1. V_{PP} and V_{PPNVM} are internally shorted.

Table 22 • Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions

I/O	MSIO	MSIOD	DDRIO	Unit
LPDDR			200	MHz
HSTL1.5 V			200	MHz
SSTL 2.5 V	255	350	200	MHz
SSTL 1.8 V			334	MHz
SSTL 1.5 V			334	MHz

Table 23 • Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions

I/O	MSIO	MSIOD	Unit
LVPECL (input only)	450		MHz
LVDS 3.3 V	267.5		MHz
LVDS 2.5 V	267.5	350	MHz
RSDS	260	350	MHz
BLVDS	250		MHz
MLVDS	250		MHz
Mini-LVDS	260	350	MHz

2.3.5.6 Single-Ended I/O Standards

2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 29 • LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

Table 30 • LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DC input logic high	V_{IH} (DC)	2.0	3.45	V
DC input logic low	V_{IL} (DC)	-0.3	0.8	V
Input current high ¹	I_{IH} (DC)			
Input current low ¹	I_{IL} (DC)			

1. See Table 24, page 22.

Table 31 • LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DC output logic high ¹	V_{OH}	$V_{DDI} - 0.4$		V
DC output logic low ¹	V_{OL}		0.4	V

1. The V_{OH}/V_{OL} test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

Table 32 • LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	2.4		V
DC output logic low	V_{OL}		0.4	V

Table 33 • LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	600	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 34 • LVTTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.4	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 35 • LVTTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank

Output Drive Selection	V_{OH} (V)	V_{OL} (V)	IOH (at V_{OH}) mA	IOL (at V_{OL}) mA
2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	$V_{DDI} - 0.4$	0.4	4	4
8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA	$V_{DDI} - 0.4$	0.4	16	16
20 mA	$V_{DDI} - 0.4$	0.4	20	20

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.0\text{ V}$

Table 36 • LVTTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	2.262	2.663	2.289	2.695	ns

Table 37 • LVTTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.192	3.755	3.47	4.083	2.969	3.494	1.856	2.183	3.337	3.926	ns
4 mA	Slow	2.331	2.742	2.673	3.145	2.526	2.973	3.034	3.569	4.451	5.236	ns
8 mA	Slow	2.135	2.511	2.33	2.741	2.297	2.703	4.532	5.331	4.825	5.676	ns
12 mA	Slow	2.052	2.414	2.107	2.479	2.162	2.544	5.75	6.764	5.445	6.406	ns
16 mA	Slow	2.062	2.425	2.072	2.438	2.145	2.525	5.993	7.05	5.625	6.618	ns
20 mA	Slow	2.148	2.527	1.999	2.353	2.088	2.458	6.262	7.367	5.876	6.913	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 62 • LVCMOS 1.5 V DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC output logic high	VOH	$V_{DDI} \times 0.75$		V
DC output logic low	VOL		$V_{DDI} \times 0.25$	V

Table 63 • LVCMOS 1.5 V AC Minimum and Maximum Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	235	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D_{MAX}	160	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	220	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 64 • LVCMOS 1.5 V AC Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CA L	75, 60, 50, 40	Ω

Table 65 • LVCMOS 1.5 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point	V_{TRIP}	0.75	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 66 • LVCMOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			V_{OH} (V)	V_{OL} (V)	IOH (at V_{OH}) mA	IOL (at V_{OL}) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	2	2
4 mA	4 mA	4 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	4	4
6 mA	6 mA	6 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	6	6
8 mA		8 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	8	8
		10 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	10	10
		12 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	12	12

Note: For a detailed I/V curve, use the corresponding IBIS models:
www.microsemi.com/soc/download/ibis/default.aspx.

Table 70 • LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)
(continued)

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
6 mA	Slow	4.244	4.993	3.465	4.076	4.233	4.979	6.39	7.518	5.736	6.748	ns
	Medium	3.774	4.44	3.05	3.587	3.762	4.426	6.114	7.193	5.397	6.35	ns
	Medium fast	3.544	4.17	2.839	3.339	3.529	4.152	5.978	7.033	5.27	6.2	ns
	Fast	3.519	4.14	2.82	3.317	3.504	4.122	5.965	7.017	5.259	6.187	ns
8 mA	Slow	4.099	4.823	3.311	3.894	4.087	4.807	6.584	7.746	5.854	6.888	ns
	Medium	3.656	4.301	2.927	3.443	3.642	4.284	6.311	7.425	5.553	6.533	ns
	Medium fast	3.437	4.044	2.731	3.213	3.42	4.023	6.182	7.273	5.435	6.394	ns
	Fast	3.41	4.012	2.715	3.193	3.393	3.991	6.178	7.269	5.425	6.383	ns
10 mA	Slow	4.029	4.74	3.238	3.809	4.015	4.723	6.732	7.921	5.965	7.018	ns
	Medium	3.601	4.237	2.867	3.372	3.586	4.218	6.473	7.615	5.669	6.669	ns
	Medium fast	3.384	3.981	2.672	3.143	3.365	3.958	6.351	7.471	5.55	6.529	ns
	Fast	3.357	3.949	2.655	3.123	3.338	3.927	6.345	7.464	5.54	6.518	ns
12 mA	Slow	3.974	4.675	3.196	3.759	3.958	4.656	6.842	8.049	6.068	7.139	ns
	Medium	3.55	4.176	2.827	3.326	3.534	4.157	6.584	7.746	5.751	6.766	ns
	Medium fast	3.345	3.935	2.638	3.103	3.325	3.911	6.488	7.633	5.641	6.637	ns
	Fast	3.316	3.902	2.621	3.083	3.297	3.878	6.486	7.63	5.626	6.619	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 71 • LVCMOS 1.5 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	4.423	5.203	5.397	6.35	5.686	6.69	5.609	6.599	5.561	6.542	ns
4 mA	Slow	4.05	4.765	4.503	5.298	4.92	5.788	7.358	8.657	6.525	7.677	ns
6 mA	Slow	4.081	4.801	4.259	5.012	4.699	5.528	7.659	9.011	6.709	7.893	ns
8 mA	Slow	4.234	4.98	4.068	4.786	4.521	5.319	8.218	9.668	7.05	8.294	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 100 • HSTL AC Test Parameter Specification

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.75	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for HSTL15 Class I (T_{DP})	RTT_TEST	50	Ω
Reference resistance for data test path for HSTL15 Class II (T_{DP})	RTT_TEST	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst-case commercial conditions: $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, worst-case V_{DDI} .

Table 101 • HSTL Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)

		T_{PY}		
		-1	-Std	Unit
Pseudo differential	None	1.605	1.888	ns
	47.8	1.614	1.898	ns
True differential	None	1.622	1.909	ns
	47.8	1.628	1.916	ns

Table 102 • HSTL Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
HSTL Class I											
Single-ended	2.6	3.059	2.514	2.958	2.514	2.958	2.431	2.86	2.431	2.86	ns
Differential	2.621	3.083	2.648	3.115	2.647	3.113	2.925	3.442	2.923	3.44	ns
HSTL Class II											
Single-ended	2.511	2.954	2.488	2.927	2.49	2.93	2.409	2.833	2.411	2.836	ns
Differential	2.528	2.974	2.552	3.003	2.551	3.001	2.897	3.409	2.896	3.408	ns

2.3.6.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

Table 136 • SSTL15 AC Test Parameter Specifications (for DDRIO I/O Bank Only)

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.75	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for SSTL15 Class I (T_{DP})	RTT_TEST	50	Ω
Reference resistance for data test path for SSTL15 Class II (T_{DP})	RTT_TEST	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.425\text{ V}$

Table 137 • DDR3/SSTL15 Receiver Characteristics for DDRIO I/O Bank – with Calibration Only

		T_{PY}		
On-Die Termination (ODT)		-1	-Std	Unit
Pseudo differential	None	1.605	1.888	ns
	20	1.616	1.901	ns
	30	1.613	1.897	ns
	40	1.611	1.895	ns
	60	1.609	1.893	ns
	120	1.607	1.89	ns
True differential	None	1.623	1.91	ns
	20	1.637	1.926	ns
	30	1.63	1.918	ns
	40	1.626	1.914	ns
	60	1.622	1.91	ns
	120	1.619	1.905	ns

Table 138 • DDR3/SSTL15 Transmitter Characteristics (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)											
Single-ended	2.533	2.98	2.522	2.967	2.523	2.968	2.427	2.855	2.428	2.856	ns
Differential	2.555	3.005	3.073	3.615	3.073	3.615	2.416	2.843	2.416	2.843	ns
DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)											
Single-ended	2.53	2.977	2.514	2.958	2.516	2.96	2.422	2.849	2.425	2.852	ns
Differential	2.552	3.002	2.591	3.048	2.59	3.047	2.882	3.391	2.881	3.39	ns

Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers) (continued)

	medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	medium_fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10 mA	slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	medium_fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12 mA	slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	medium_fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16 mA	slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	medium_fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO management).

2.3.7 Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

2.3.7.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

Minimum and Maximum Input and Output Levels

Table 160 • LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{DDI}	2.375	2.5	2.625	V	2.5 V range
Supply voltage	V_{DDI}	3.15	3.3	3.45	V	3.3 V range

Table 161 • LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit	Conditions
DC Input voltage	V_I	0	2.925	V	2.5 V range
DC input voltage	V_I	0	3.45	V	3.3 V range
Input current high ¹	I_{IH} (DC)				
Input current low ¹	I_{IL} (DC)				

1. See Table 24, page 22.

Table 185 • M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 186 • M-LVDS Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	V_{OD}	300	650	mV
Output common mode voltage (for MSIO I/O bank only)	V_{OCM}	0.3	2.1	V
Input common mode voltage	V_{ICM}	0.3	1.2	V
Input differential voltage	V_{ID}	50	2400	mV

Table 187 • M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	500	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 188 • M-LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	50	Ω

Table 189 • M-LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 190 • M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.738	3.221	ns
100	2.735	3.218	ns

The following table lists the input data register propagation delays in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 219 • Input Data Register Propagation Delays

Parameter	Symbol	Measuring Nodes (from, to) ¹	-1		Unit
			-1	-Std	
Bypass delay of the input register	T_{IBYP}	F, G	0.353	0.415	ns
Clock-to-Q of the input register	T_{ICLKQ}	E, G	0.16	0.188	ns
Data setup time for the input register	T_{ISUD}	A, E	0.357	0.421	ns
Data hold time for the input register	T_{IHD}	A, E	0	0	ns
Enable setup time for the input register	T_{ISUE}	B, E	0.46	0.542	ns
Enable hold time for the input register	T_{IHE}	B, E	0	0	ns
Synchronous load setup time for the input register	T_{ISUSL}	D, E	0.46	0.542	ns
Synchronous load hold time for the input register	T_{IHSL}	D, E	0	0	ns
Asynchronous clear-to-Q of the input register (ADn=1)	T_{IALN2Q}	C, G	0.625	0.735	ns
Asynchronous preset-to-Q of the input register (ADn=0)		C, G	0.587	0.69	ns
Asynchronous load removal time for the input register	$T_{IREMALN}$	C, E	0	0	ns
Asynchronous load recovery time for the input register	$T_{IRECALN}$	C, E	0.074	0.087	ns
Asynchronous load minimum pulse width for the input register	T_{IWALN}	C, C	0.304	0.357	ns
Clock minimum pulse width high for the input register	$T_{ICKMPWH}$	E, E	0.075	0.088	ns
Clock minimum pulse width low for the input register	$T_{ICKMPWL}$	E, E	0.159	0.187	ns

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

Table 232 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 (continued)

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Address setup time	T_{ADDRSU}	0.475		0.559		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.336		0.395		ns
Data hold time	T_{DHD}	0.082		0.096		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		1.529		1.799	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.485		0.57		ns
Read enable hold time	T_{RDEHD}	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}		1.514		1.781	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.415		0.488		ns
Write enable hold time	T_{WEHD}	0.048		0.057		ns
Maximum frequency	F_{MAX}		400		340	MHz

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 233 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns

The following table lists the RAM1K18 – two-port mode for depth × width configuration 512 × 36 in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 236 • RAM1K18 – Two-Port Mode for Depth × Width Configuration 512 × 36

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register	T_{CLK2Q}		0.334		0.393	ns
Read access time without pipeline register			2.25		2.647	ns
Address setup time	T_{ADDRSU}	0.313		0.368		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.337		0.396		ns
Data hold time	T_{DHD}	0.111		0.13		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.201		0.237		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.25		2.647	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.449		0.528		ns
Read enable hold time	T_{RDEHD}	0.167		0.197		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}		1.506		1.772	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.39		0.458		ns
Write enable hold time	T_{WEHD}	0.242		0.285		ns
Maximum frequency	F_{MAX}		400		340	MHz

2.3.12.2 FPGA Fabric Micro SRAM (μ SRAM)

The following table lists the μ SRAM in 64×18 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 237 • μ SRAM (RAM64x18) in 64×18 Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register				1.677		1.973
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode			1.856		2.184	
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode			-0.778		-0.915	
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)			0.046		0.054	
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)			0.236		0.278	
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.839		0.987	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns

Table 237 • μ SRAM (RAM64x18) in 64 × 18 Mode (continued)

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	-0.026		-0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 64 × 16 mode in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 238 • μ SRAM (RAM64x16) in 64 × 16 Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register				1.677		1.973
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode			1.856		2.184	
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode			-0.778		-0.915	
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)			0.046		0.054	
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)			0.236		0.278	
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.983	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns

Table 243 • μ SRAM (RAM1024x1) in 1024 x 1 Mode (continued)

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.83		0.98	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.003		0.004		ns
Write input data hold time	T_{DINCHD}	0.137		0.161		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.247		0.29		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	-0.03		-0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

2.3.13 Programming Times

The following tables list the programming times in typical conditions when $T_J = 25\text{ }^\circ\text{C}$, $V_{DD} = 1.2\text{ V}$. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 244 • JTAG Programming (Fabric Only)

M2S/M2GL				
Device	Image size Bytes	Program	Verify	Unit
005	302672	22	10	Sec
010	568784	28	18	Sec
025	1223504	51	26	Sec
050	2424832	66	54	Sec
060	2418896	77	54	Sec
090	3645968	113	126	Sec
150	6139184	155	193	Sec

Table 251 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only) (continued)

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
150	544496	10	158	15	Sec

Table 252 • SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	9	61	11	Sec
010	842688	15	107	21	Sec
025	1497408	26	121	35	Sec
050	2695168	43	141	55	Sec
060	2686464	48	143	60	Sec
090	4190208	75	244	91	Sec
150	6682768	117	296	141	Sec

Table 253 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	Unit
	100 kHz	25 MHz	12.5 MHz	
005	47	27	28	Sec
010	77	35	35	Sec
025	150	42	41	Sec
050	33 ¹	Not Supported	Not Supported	Sec
060	291	83	82	Sec
090	427	109	108	Sec
150	708	157	160	Sec

1. Auto Programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

Table 254 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	Unit
	100 kHz	25 MHz	12.5 MHz	
005	41	48	49	Sec
010	86	87	87	Sec
025	87	85	86	Sec
050	85	Not Supported	Not Supported	Sec
060	78	86	86	Sec
090	154	162	162	Sec

Table 293 • Flash*Freeze Entry and Exit Times (continued)

Parameter	Symbol	Entry/Exit Timing			Unit	Conditions
		FCLK = 100MHz		FCLK = 3 MHz		
		005, 010, 025, 060, 090, and 150	050	All Devices		
Exit time with respect to the fabric PLL lock ¹	TFF_EXIT	1.5	1.5	1.5	ms	eNVM and MSS/HPMS PLL = ON during F*F
		1.5	1.5	1.5	ms	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit
Exit time with respect to the fabric buffer output	TFF_EXIT	21	15	21	µs	eNVM and MSS/HPMS PLL = ON during F*F
		65	55	65	µs	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit

1. PLL Lock Delay set to 1024 cycles (default).

2.3.28 DDR Memory Interface Characteristics

The following table lists the DDR memory interface characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 294 • DDR Memory Interface Characteristics

Standard	Supported Data Rate		Unit
	Min	Max	
DDR3	667	667	Mbps
DDR2	667	667	Mbps
LPDDR	50	400	Mbps

2.3.29 SFP Transceiver Characteristics

IGLOO2 and SmartFusion2 SerDes complies with small form-factor pluggable (SFP) requirements as specified in SFP INF-80741. The following table provides the electrical characteristics.

The following table lists the SFP transceiver electrical characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 295 • SFP Transceiver Electrical Characteristics

Pin	Direction	Differential Peak-Peak Voltage		Unit
		Min	Max	
RD+/- ¹	Output	1600	2400	mV
TD+/- ²	Input	350	2400	mV

1. Based on default SerDes transmitter settings for PCIe Gen1. Lower amplitudes are available through programming changes to TX_AMP setting.
2. Based on Input Voltage Common-Mode (VICM) = 0 V. Requires AC Coupling.

2.3.30 SerDes Electrical and Timing AC and DC Characteristics

PCIe is a high-speed, packet-based, point-to-point, low-pin-count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block.

The following table lists the transmitter parameters in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 296 • Transmitter Parameters

Symbol	Description	Min	Max	Unit
VTX-DIFF-PP	Differential swing (2.5 Gbps, 5.0 Gbps)	0.8	1.2	V
VTX-CM-AC-P	Output common mode voltage (2.5 Gbps)		20	mV
VTX-CM-AC-PP	Output common mode voltage (5.0 Gbps)		100	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%, 2.5 Gbps)	0.125		UI
	Rise and fall time (20% to 80%, 5.0 Gbps)	0.15		UI
ZTX-DIFF-DC	Output impedance–differential	80	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SerDes block (2.5 Gbps)		500 ps + 2 UI	ps
	Lane-to-lane TX skew within a SerDes block (5.0 Gbps)		500 ps + 4 UI	ps
RLTX-DIFF	Return loss differential mode (2.5 Gbps)	–10		dB
	Return loss differential mode (5.0 Gbps) 0.05 GHz to 1.25 GHz	–10		dB
	1.25 GHz to 2.5 GHz	–8		dB
RLTX-CM	Return loss common mode (2.5 Gbps, 5.0 Gbps)	–6		dB
TX-LOCK-RST	Transmit PLL lock time from reset		10	μs
VTX-AMP	100 mV setting	90	150	mV
	400 mV setting	320	480	mV
	800 mV setting	660	940	mV
	1200 mV setting	950	1400	mV