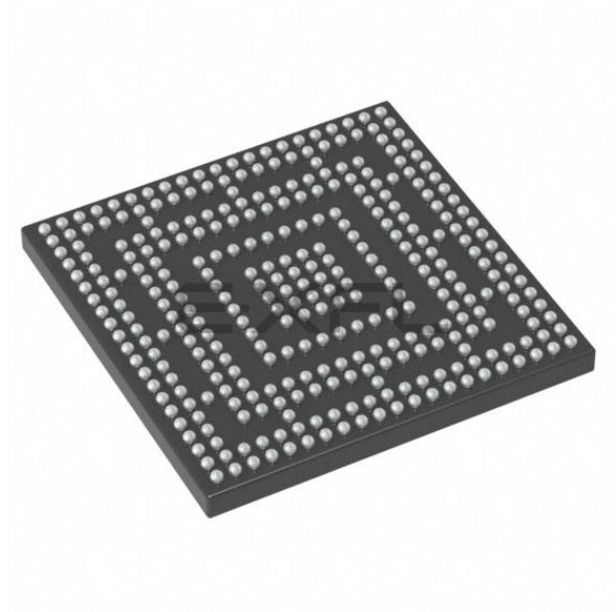

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 25K Logic Modules
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	325-TFBGA, FCBGA
Supplier Device Package	325-FCBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s025t-fcs325i

- Added Table 244, page 94 and Table 256, page 99 (SAR 73971).
- Updated the SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 71171).
- Added the DEVRST_N Characteristics, page 116 (SAR 64100, 72103).
- Added Table 298, page 122 (SAR 71897).
- Updated Table 25, page 22, Table 26, page 23, and Table 27, page 23 (SAR 74570).
- Added 060 devices in Table 277, page 107, Table 278, page 108, and Table 279, page 108 (SAR 57898).
- Updated duty cycle parameter of crystal in Table 280, page 109 and Table 281, page 109 (SAR 57898).
- Added 32 KHz mode PLL acquisition time in Table 282, page 110 (SAR 68281).
- Updated Table 293, page 119 for 060 devices (SAR 57828).
- Updated Table 297, page 122 for CID value (SAR 70878).

1.4 Revision 8.0

The following is a summary of the changes in revision 8.0 of this document.

- Updated Table 11, page 12 (SAR 69218).
- Updated Table 12, page 13 (SAR 69218).
- Updated Table 283, page 111 (SAR 69000).

1.5 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Updated Table 1, page 4(SAR 68620).

1.6 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- Updated Table 5, page 7 (SAR 65949).
- Updated Table 9, page 10 (SAR 62995).
- Updated Table 123, page 47 and Table 133, page 49 (SAR 67210).
- Added Embedded NVM (eNVM) Characteristics, page 104 (SAR 52509).
- Updated Table 277, page 107 (SAR 64855).
- Updated Table 282, page 110 (SAR 65958 and SAR 56666).
- Added DDR Memory Interface Characteristics, page 120 (SAR 66223).
- Added SFP Transceiver Characteristics, page 120 (SAR 63105).
- Updated Table 302, page 123 and Table 309, page 129 (SAR 66314).

1.7 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Updated Table 1, page 4.
- Updated Table 4, page 6 for T_J symbol information.
- Updated Table 5, page 7 (SAR 63109).
- Updated Table 9, page 10.
- Updated Table 282, page 110 (SAR 62012).
- Added Table 290, page 116 (SAR 64100).
- Added Table 306, page 128, Table 307, page 128 (SAR 50424).

1.8 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document.

- Updated Table 1, page 4. Changed the Status of 090 devices to "Production" (SAR 62750).
- Updated Figure 10, page 70. Removed inverter bubble from DDR_IN latch (SAR 61418).
- Updated SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 62836).

1.9 Revision 3.0

In revision 3.0 of this document, the Theta B/C columns and FCS325 package was updated. For more information, see Table 9, page 10 (SAR 62002).

1.10 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Table 1, page 4 was updated (SAR 59056).
- Table 7, page 8 temperature and data retention information was updated SAR (61363).
- Storage Operating Table was updated and split into three tables – Table 5, page 7, Table 7, page 8 (SAR 58725).
- Updated Theta B/C columns and FCS325 package in Table 9, page 10 (SAR 62002).
- Added 090-FCS325 thermal resistance to Table 9, page 10 (SAR 59384).
- TQ144 package was added to Table 9, page 10 (SAR 57708).
- Added PLL jitter data for the VF400 package (SAR 53162).
- Added Additional Worst Case IDD to Table 11, page 12 and Table 12, page 13 (SAR 59077).
- Table 13, page 13, Table 14, page 13, and Table 15, page 14 were added to verify Inrush currents (SAR 56348).
- Table 18, page 19 and Table 21, page 20 – I/O speeds were replaced.
- Max speed was changed in Table 41, page 26 (SAR 57221) and in Table 52, page 29 (SAR 57113).
- Minimum and Maximum DC/AC Input and Output Levels Specification, page 29 and Table 49, page 29–Table 57, page 31 were added.
- Added Cload to Table 89, page 39 (SAR 56238).
- Removed "Rs" information in DDR Timing Measurement Table 123, page 47, Table 133, page 49, and Table 144, page 52.
- Updated drive programming for M/B-LVDS outputs (SAR 58154).
- Added an inverter bubble to DDR_IN latch in Figure 10, page 70 (SAR 61418).
- QF waveform in Figure 11, page 71 was updated (SAR 59816).
- uSRAM Write Clock minimum values were updated in Table 237, page 86–Table 243, page 93 (SAR 55236).
- Fixed typo in the 32 kHz Crystal (XTAL) oscillator accuracy data section (SAR 59669).
- The "On-Chip Oscillator" section was split, and the Embedded NVM (eNVM) Characteristics, page 104 was added. Table 277, page 107–Table 281, page 109 were revised.(SARs 57898 and 59669).
- PLL VCP Frequency and conditions were added to Table 282, page 110 (SAR 57416).
- Fixed typo for PLL jitter data in the 100-400 MHz range (SAR 60727).
- Updated FCCC information in Table 282, page 110 and Table 283, page 111 (SAR 60799).
- Device 025 specifications were added to Table 283, page 111 (SAR 51625).
- JTAG Table 284, page 112 was replaced (SAR 51188).
- Flash*Freeze Table 293, page 119 was replaced (SAR 57828).
- Added support for HCSL I/O Standard for SERDES reference clocks in Table 300, page 123 and Table 301, page 123 (SAR 50748).
- Tir and Tif parameters were added to Table 303, page 124 (SAR 52203).
- Speed grade consistency was fixed in tables throughout the datasheet (SAR 50722).
- Added jitter attenuation information (SAR 59405).

1.11 Revision 1.0

The following is a summary of the changes in revision 1.0 of this document.

- The IGLOO2 v2 and the SmartFusion2 v5 datasheets are combined into this single product family datasheet.

2 IGLOO2 FPGA and SmartFusion2 SoC FPGA

Microsemi's mainstream SmartFusion®2 SoC and IGLOO®2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated math blocks, multiple embedded memory blocks, and high-performance SerDes communication interfaces on a single chip. Both families benefit from low-power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to 5 MBs of embedded RAM, up to 16 SerDes lanes, and up to four PCI Express Gen 2 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 devices integrate an entire low-power, real-time microcontroller subsystem (MSS) with a rich set of industry-standard peripherals including Ethernet, USB, and CAN, while IGLOO2 devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

2.1 Device Status

The following table shows the design security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

Table 1 • **IGLOO2 and SmartFusion2 Design Security Densities**

Design Security Device Densities	Status
005	Production
010, 010T	Production
025, 025T	Production
050, 050T	Production
060, 060T	Production
090, 090T	Production
150, 150T	Production

The following table shows the data security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

Table 2 • **IGLOO2 and SmartFusion2 Data Security Densities**

Data Security Device Densities	Status
005S	Production
010TS	Production
025TS	Production
050TS	Production
060TS	Production
090TS	Production
150TS	Production

Figure 1 • **High Temperature Data Retention (HTR)**

2.3.1.1 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to –1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to V_{CCI} + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

Note: The above specifications do not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant with the PCI standard including the PCI overshoot/undershoot specifications.

2.3.1.2 Thermal Characteristics

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ1 through EQ3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

2.3.4 Timing Model

This section describes timing model and timing parameters.

Figure 2 • **Timing Model**

The following table lists the timing model parameters in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 17 • **Timing Model Parameters**

Index	Symbol	Description	–1	Unit	For More Information
A	T_{PY}	Propagation delay of DDR3 receiver	1.605	ns	See Table 137, page 50
B	T_{ICLKQ}	Clock-to-Q of the input data register	0.16	ns	See Table 221, page 71
	T_{ISUD}	Setup time of the input data register	0.357	ns	See Table 221, page 71
C	T_{RCKH}	Input high delay for global clock	1.53	ns	See Table 227, page 78
	T_{RCKL}	Input low delay for global clock	0.897	ns	See Table 227, page 78
D	T_{PY}	Input propagation delay of LVDS receiver	2.774	ns	See Table 167, page 56
E	T_{DP}	Propagation delay of a three-input AND gate	0.198	ns	See Table 223, page 76

Table 100 • **HSTL AC Test Parameter Specification**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.75	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for HSTL15 Class I (T_{DP})	RTT_TEST	50	Ω
Reference resistance for data test path for HSTL15 Class II (T_{DP})	RTT_TEST	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst-case commercial conditions: T_J = 85 °C, V_{DD} = 1.14 V, worst-case V_{DDI}.

Table 101 • **HSTL Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)**

		T_{PY}		
	On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
Pseudo differential	None	1.605	1.888	ns
	47.8	1.614	1.898	ns
True differential	None	1.622	1.909	ns
	47.8	1.628	1.916	ns

Table 102 • **HSTL Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
	–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
HSTL Class I											
Single-ended	2.6	3.059	2.514	2.958	2.514	2.958	2.431	2.86	2.431	2.86	ns
Differential	2.621	3.083	2.648	3.115	2.647	3.113	2.925	3.442	2.923	3.44	ns
HSTL Class II											
Single-ended	2.511	2.954	2.488	2.927	2.49	2.93	2.409	2.833	2.411	2.836	ns
Differential	2.528	2.974	2.552	3.003	2.551	3.001	2.897	3.409	2.896	3.408	ns

2.3.6.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

Table 107 • **SSTL2 AC Differential Voltage Specifications**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF} (AC)	0.7		V
AC differential cross point voltage	V_x (AC)	0.5 × V_{DDI} – 0.2	0.5 × V_{DDI} + 0.2	V

Table 108 • **SSTL2 Minimum and Maximum AC Switching Speeds**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	400	Mbps	AC loading: per JEDEC specifications
Maximum data rate (for MSIO I/O bank)	D_{MAX}	575	Mbps	AC loading: 17pF load
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	700	Mbps	AC loading: 3 pF / 50 Ω load
		510	Mbps	AC loading: 17pF load

Table 109 • **SSTL2 AC Impedance Specifications**

Parameter	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	20, 42	Ω	Reference resistor = 150 Ω

Table 110 • **DDR1/SSTL2 AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.25	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for SSTL2 Class I (T_{DP})	RTT_TEST	50	Ω
Reference resistance for data test path for SSTL2 Class II (T_{DP})	RTT_TEST	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V

Table 111 • **SSTL2 Receiver Characteristics for DDRIO I/O Bank (Input Buffers)**

	On-Die Termination (ODT)	T_{PY} –1	T_{PY} –Std	Unit
Pseudo differential	None	1.549	1.821	ns
True differential	None	1.589	1.87	ns

Table 131 • **SSTL15 DC Output Voltage Specification (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DDR3/SSTL15 Class I (DDR3 Reduced Drive)				
DC output logic high	V_{OH}	0.8 × V_{DDI}		V
DC output logic low	V_{OL}		0.2 × V_{DDI}	V
Output minimum source DC current	I_{OH} at V_{OH}	6.5		mA
Output minimum sink current	I_{OL} at V_{OL}	–6.5		mA
DDR3/SSTL15 Class II (DDR3 Full Drive)				
DC output logic high	V_{OH}	0.8 × V_{DDI}		V
DC output logic low	V_{OL}		0.2 × V_{DDI}	V
Output minimum source DC current	I_{OH} at V_{OH}	7.6		mA
Output minimum sink current	I_{OL} at V_{OL}	–7.6		mA

Table 132 • **SSTL15 DC Differential Voltage Specification (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID}	0.2	V

Note: To meet JEDEC electrical compliance, use DDR3 full drive transmitter.

Table 133 • **SSTL15 AC SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF} (AC)	0.3		V
AC differential cross point voltage	V_x (AC)	0.5 × V_{DDI} – 0.150	0.5 × V_{DDI} + 0.150	V

Table 134 • **SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	667	Mbps	AC loading: per JEDEC specifications

Table 135 • **SSTL15 AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	R_{REF}	34, 40	Ω	Reference resistor = 240 Ω
Effective impedance value (ODT)	R_{TT}	20, 30, 40, 60, 120	Ω	Reference resistor = 240 Ω

Table 144 • **LPDDR AC Differential Voltage Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF}	0.6 × V_{DDI}		V
AC differential cross point voltage	V_x	0.4 × V_{DDI}	0.6 × V_{DDI}	V

Table 145 • **LPDDR AC Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	400	Mbps	AC loading: per JEDEC specifications

Table 146 • **LPDDR AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	R_{REF}	20, 42	Ω	Reference resistor = 150 Ω
Effective impedance value (ODT)	R_{TT}	50, 70, 150	Ω	Reference resistor = 150 Ω

Table 147 • **LPDDR AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.9	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for LPDDR (T_{DP})	RTT_TEST	50	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	Ω

AC Switching Characteristics

Worst-case commercial conditions: T_J = 85 °C, V_{DD} = 1.14 V, worst-case V_{DDI}.

Table 148 • **LPDDR Receiver Characteristics for DDRIO I/O Bank with Fixed Codes**

		T_{PY}		
	On-Die Termination (ODT)	–1	–Std	Unit
Pseudo differential	None	1.568	1.845	ns
True differential	None	1.588	1.869	ns

Table 149 • **LPDDR Reduced Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

	T_{DP}		T_{ENZL}		T_{ENZH}		T_{ENHZ}		T_{ENLZ}		
	–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	Unit
Single-ended	2.383	2.804	2.23	2.623	2.229	2.622	2.202	2.591	2.201	2.59	ns
Differential	2.396	2.819	2.764	3.252	2.764	3.252	2.255	2.653	2.255	2.653	ns

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V.

Table 210 • **RSDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.855	3.359	ns
100	2.85	3.353	ns

Table 211 • **RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.602	3.061	ns
100	2.597	3.055	ns

Table 212 • **RSDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
2.097	2.467	2.303	2.709	2.291	2.695	1.961	2.307	1.947	2.29	ns

Table 213 • **RSDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
	–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
No pre-emphasis	1.614	1.899	1.559	1.834	1.55	1.823	1.59	1.87	1.575	1.852	ns
Min pre-emphasis	1.604	1.887	1.742	2.05	1.728	2.032	1.889	2.222	1.858	2.185	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

2.3.7.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

Minimum and Maximum Input and Output Levels (Applicable to MSIO I/O Bank Only)

Table 214 • **LVPECL Recommended DC Operating Conditions**

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

Table 243 • **µSRAM (RAM1024x1) in 1024 × 1 Mode *(continued)***

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.83		0.98	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.003		0.004		ns
Write input data hold time	T_{DINCHD}	0.137		0.161		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.247		0.29		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.03		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

2.3.13 Programming Times

The following tables list the programming times in typical conditions when T_J = 25 °C, V_{DD} = 1.2 V. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 244 • **JTAG Programming (Fabric Only)**

M2S/M2GL Device	**Image size Bytes**	**Program**	**Verify**	**Unit**
005	302672	22	10	Sec
010	568784	28	18	Sec
025	1223504	51	26	Sec
050	2424832	66	54	Sec
060	2418896	77	54	Sec
090	3645968	113	126	Sec
150	6139184	155	193	Sec

The following table lists the programming times in worst-case conditions when T_J = 100 °C, V_{DD} = 1.14 V. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 256 • **JTAG Programming (Fabric Only)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	302672	44	10	Sec
010	568784	50	18	Sec
025	1223504	73	26	Sec
050	2424832	88	54	Sec
060	2418896	99	54	Sec
090	3645968	135	126	Sec
150	6139184	177	193	Sec

Table 257 • **JTAG Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	137536	61	4	Sec
010	274816	100	9	Sec
025	274816	100	9	Sec
050	2,78,528	106	8	Sec
060	268480	98	8	Sec
090	544496	176	15	Sec
150	544496	177	15	Sec

Table 258 • **JTAG Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	439296	71	11	Sec
010	842688	129	20	Sec
025	1497408	142	35	Sec
050	2695168	184	59	Sec
060	2686464	180	70	Sec
090	4190208	288	147	Sec
150	6682768	338	231	Sec

Table 259 • **2 Step IAP Programming (Fabric Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	302672	4	39	6	Sec
010	568784	7	45	12	Sec
025	1223504	14	55	23	Sec
050	2424832	29	74	40	Sec
060	2418896	39	83	50	Sec
090	3645968	60	106	73	Sec
150	6139184	100	154	120	Sec

Table 260 • **2 Step IAP Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	137536	2	59	5	Sec
010	274816	4	98	11	Sec
025	274816	4	100	10	Sec
050	2,78,528	3	107	9	Sec
060	268480	5	98	22	Sec
090	544496	10	174	43	Sec
150	544496	10	175	44	Sec

Table 261 • **2 Step IAP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	6	78	11	Sec
010	842688	11	122	21	Sec
025	1497408	19	135	32	Sec
050	2695168	32	158	48	Sec
060	2686464	43	159	70	Sec
090	4190208	68	258	115	Sec
150	6682768	109	308	162	Sec

Table 262 • **SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	302672	6	41	8	Sec
010	568784	10	48	14	Sec
025	1223504	21	61	29	Sec
050	2424832	39	82	50	Sec
060	2418896	44	87	54	Sec
090	3645968	66	112	79	Sec
150	6139184	108	162	128	Sec

Table 263 • **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	137536	3	64	4	Sec
010	274816	4	104	7	Sec
025	274816	4	104	8	Sec
050	2,78,528	4	102	8	Sec
060	268480	6	102	8	Sec
090	544496	10	179	15	Sec
150	544496	10	180	15	Sec

Table 264 • **SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	9	83	11	Sec
010	842688	15	129	21	Sec
025	1497408	26	143	35	Sec
050	2695168	43	163	55	Sec
060	2686464	48	165	60	Sec
090	4190208	75	266	91	Sec
150	6682768	117	318	141	Sec

Table 265 • **Programming Times with 100 kHz, 25 MHz. and 12.5 MHz SPI Clock Rates (Fabric Only)**

	Auto Programming	Auto Update	Programming Recovery	
M2S/M2GL Device	**100 kHz**	**25 MHz**	**12.5 MHz**	**Unit**
005	69	49	50	Sec
010	99	57	57	Sec
025	150	64	63	Sec
050	55[1]	Not Supported	Not Supported	Sec
060	313	105	104	Sec
090	449	131	130	Sec
150	730	179	183	Sec

1. Auto programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

Table 266 • **Programming Times with 100 kHz, 25 MHz. and 12.5 MHz SPI Clock Rates (eNVM Only)**

	Auto Programming	Auto Update	Programming Recovery	
M2S/M2GL Device	**100 kHz**	**25 MHz**	**12.5 MHz**	**Unit**
005	63	70	71	Sec
010	108	109	109	Sec
025	109	107	108	Sec
050	107	Not Supported	Not Supported	Sec
060	100	108	108	Sec
090	176	184	184	Sec
150	183	183	183	Sec

Table 267 • **Programming Times with 100 kHz, 25 MHz. and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

	Auto Programming	Auto Update	Programming Recovery	
M2S/M2GL Device	**100 kHz**	**25 MHz**	**12.5 MHz**	**Unit**
005	109	89	88	Sec
010	183	135	135	Sec
025	251	142	143	Sec
050	134	Not Supported	Not Supported	Sec
060	390	183	180	Sec
090	604	283	282	Sec
150	889	331	332	Sec

Table 276 • **Cryptographic Block Characteristics *(continued)***

Service	Conditions	Timing	Unit
SHA256	512 bits	540	kbps
	1024 bits	780	kbps
	2048 bits	950	kbps
	24 kbits	1140	kbps
HMAC	512 bytes	820	kbps
	1024 bytes	890	kbps
	2048 bytes	930	kbps
	24 kbytes	980	kbps
KeyTree		1.8	ms
Challenge-response	PUF = OFF	25	ms
	PUF = ON	7	ms
ECC point multiplication		590	ms
ECC point addition		8	ms

1. Using cypher block chaining (CBC) mode.

2.3.19 Crystal Oscillator

The following table describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

Table 277 • **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)**

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		20		MHz	
Accuracy	ACCXTAL			0.0047	%	005, 010, 025, 050, 060, and 090 devices
				0.0058	%	150 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		200	300	ps	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		200	300	ps	010, 025, 050, and 060 devices
			250	410	ps	150 devices
			250	550	ps	005 and 090 devices
Operating current	IDYNXTAL		1.5		mA	010, 050, and 060 devices
			1.65		mA	005, 025, 090, and 150 devices
Input logic level high	VIHXTAL	0.9 V_{PP}			V	
Input logic level low	VILXTAL			0.1 V_{PP}	V	

2.3.24 Power-up to Functional Times

The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 288 • **Power-up to Functional Times for SmartFusion2**

				Maximum Power-up to Functional Time for SmartFusion2 (uS)						
Symbol	**From**	**To**	**Description**	**005**	**010**	**025**	**050**	**060**	**090**	**150**
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	647	500	531	483	474	524	647
$T_{POR2MSSRST}$	POWER_ON_RESET_N	MSS_RESET_N_M2F	Fabric to MSS	644	497	528	480	468	518	641
$T_{MSSRST2OUT}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.6	3.6	3.6	3.4	4.9	4.8	4.8
$T_{VDD2OUT}$	V_{DD}	Output available at I/O	V_{DD} at its minimum threshold level to output	3096	2975	3012	2959	2869	2992	3225
$T_{VDD2POR}$	V_{DD}	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	2476	2487	2496	2486	2406	2563	2602
$T_{VDD2MSSRST}$	V_{DD}	MSS_RESET_N_M2F	V_{DD} at its minimum threshold level to MSS	3093	2972	3008	2956	2864	2987	3220
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

2.3.31.2 SmartFusion2 Inter-Integrated Circuit (I^2C) Characteristics

This section describes the DC and switching of the I^2C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, see Figure 21, page 125.

The following table lists the I^2C characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V

Table 303 • **I2C Characteristics**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input low voltage	V_{IL}	–0.3		0.8	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive.
Input high voltage	V_{IH}	2		3.45	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive.
Hysteresis of schmitt triggered inputs for V_{DDI} > 2 V	V_{HYS}	0.05 × V_{DDI}			V	See Table 28, page 23 for more information.
Input current high	I_{IL}			10	µA	See Single-Ended I/O Standards, page 24 for more information.
Input current low	I_{IH}			10	µA	See Single-Ended I/O Standards, page 24 for more information.
Input rise time	T_{ir}			1000	ns	Standard mode
				300	ns	Fast mode
Input fall time	T_{if}			300	ns	Standard mode
				300	ns	Fast mode
Maximum output voltage low (open drain) at 3 mA sink current for V_{DDI} > 2 V	V_{OL}			0.4	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive.
Pin capacitance	Cin			10	pF	V_{IN} = 0, f = 1.0 MHz
Output fall time from VIHMin to VILMax[1]	t_{OF}[1]		21.04		ns	V_{IHmin} to V_{ILMax}, CLOAD = 400 pF
			5.556		ns	V_{IHmin} to V_{ILMax}, CLOAD = 100 pF
Output rise time from VILMax to VIHMin[1]	t_{OR} [1]		19.887		ns	V_{ILMax} to V_{IHmin}, CLOAD = 400 pF
			5.218		ns	V_{ILMax} to V_{IHmin}, CLOAD = 100 pF
Output buffer maximum pull-down resistance[2, 3]	$R_{pull\text{-}up}$[2,3]			50	Ω	
Output buffer maximum pull-up resistance[2, 4]	$R_{pull\text{-}down}$[2,4]			131.25	Ω	

2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 308 • **MMUART Characteristics**

Parameter	Description	–1	–Std	Unit
FMMUART_REF_CLK	Internally sourced MMUART reference clock frequency.	166	142	MHz
BAUDMMUARTTx	Maximum transmit baud rate	10.375	8.875	Mbps
BAUDMMUARTRx	Maximum receive baud rate	10.375	8.875	Mbps

2.3.35 IGLOO2 Specifications

2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 309 • **Maximum Frequency for HPMS Main Clock**

Symbol	Description	–1	–Std	Unit
HPMS_CLK	Maximum frequency for the HPMS main clock	166	142	MHz

2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, see Figure 23, page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 310 • **SPI Characteristics for All Devices**

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPIFMAX	Maximum operating frequency of SPI interface			20	MHz	
sp1	SPI_[0|1]_CLK minimum period					
	SPI_[0|1]_CLK = PCLK/2	12			ns	
	SPI_[0|1]_CLK = PCLK/4	24.1			ns	
	SPI_[0|1]_CLK = PCLK/8	48.2			ns	
	SPI_[0|1]_CLK = PCLK/16	0.1			µs	
	SPI_[0|1]_CLK = PCLK/32	0.19			µs	
	SPI_[0|1]_CLK = PCLK/64	0.39			µs	
	SPI_[0|1]_CLK = PCLK/128	0.77			µs	

Table 310 • **SPI Characteristics for All Devices *(continued)***

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp2	SPI_[0|1]_CLK minimum pulse width high					
	SPI_[0|1]_CLK = PCLK/2	6			ns	
	SPI_[0|1]_CLK = PCLK/4	12.05			ns	
	SPI_[0|1]_CLK = PCLK/8	24.1			ns	
	SPI_[0|1]_CLK = PCLK/16	0.05			µs	
	SPI_[0|1]_CLK = PCLK/32	0.095			µs	
	SPI_[0|1]_CLK = PCLK/64	0.195			µs	
	SPI_[0|1]_CLK = PCLK/128	0.385			µs	
sp3	SPI_[0|1]_CLK minimum pulse width low					
	SPI_[0|1]_CLK = PCLK/2	6			ns	
	SPI_[0|1]_CLK = PCLK/4	12.05			ns	
	SPI_[0|1]_CLK = PCLK/8	24.1			ns	
	SPI_[0|1]_CLK = PCLK/16	0.05			µs	
	SPI_[0|1]_CLK = PCLK/32	0.095			µs	
	SPI_[0|1]_CLK = PCLK/64	0.195			µs	
	SPI_[0|1]_CLK = PCLK/128	0.385			µs	
sp4	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS rise time (10%–90%)[1]		2.77		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
sp5	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS fall time (10%–90%)[1]		2.906		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0|1]_DI setup time[2]	12			ns	
sp9m	SPI_[0|1]_DI hold time[2]	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0|1]_DI setup time[2]	2			ns	
sp9s	SPI_[0|1]_DI hold time[2]	7			ns	