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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 25K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	325-TFBGA, FCBGA
Supplier Device Package	325-FCBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s025t-fcsg325

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2.2 References

The following documents are recommended references:

- *PB0121: IGLOO2 Product Brief*
- *DS0124: IGLOO2 Pin Descriptions*
- *PB0115: SmartFusion2 SoC FPGA Product Brief*
- *DS0115: SmartFusion2 Pin Descriptions*

All product documentation for IGLOO2 and SmartFusion2 is available at:

<http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga>

<http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#overview>

2.3 Electrical Specifications

2.3.1 Operating Conditions

The following table lists the stress limits. Stress applied above the specified limit may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table are not implied.

Table 3 • Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
DC core supply voltage. Must always power this pin.	V_{DD}	-0.3	1.32	V
Power supply for charge pumps (for normal operation and programming). Must always power this pin.	V_{PP}	-0.3	3.63	V
Analog power pad for MDDR PLL	MSS_MDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	HPMS_MDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for FDDR PLL	FDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_MSS_MDDR_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_HPMS_MDDR_VDDA	-0.3	3.63	V
Analog power pad for PLL0-5	CCC_XX[01]_PLL_VDDA	-0.3	3.63	V
High supply voltage for PLL SerDes[01]	SERDES_[01]_PLL_VDDA	-0.3	3.63	V
Analog power for SerDes[01] PLL lane0 to lane3. This is a 2.5 V SerDes internal PLL supply.	SERDES_[01]_L[0123]_VDDAPLL	-0.3	2.75	V
TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply.	SERDES_[01]_L[0123]_VDDAIO	-0.3	1.32	V
PCIe/PCS power supply	SERDES_[01]_VDD	-0.3	1.32	V
DC FPGA I/O buffer supply voltage for MSIO I/O bank	V_{DDIx}	-0.3	3.63	V
DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks	V_{DDIx}	-0.3	2.75	V
I/O Input voltage for MSIO I/O bank	V_I	-0.3	3.63	V
I/O Input voltage for MSIOD/DDRIO I/O bank	V_I	-0.3	2.75	V
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to V_{PP} .	V_{PPNVM}	-0.3	3.63	V
Storage temperature ¹	T_{STG}	-65	150	°C
Junction temperature	T_J	-55	135	°C

1. For flash programming and retention maximum limits, see Table 5, page 7. For recommended operating conditions, see Table 4, page 6.

Table 4 • Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Operating junction temperature	T_J	0	25	85	°C	Commercial
		-40	25	100	°C	Industrial
Programming junction temperatures ¹	T_J	0	25	85	°C	Commercial
		-40	25	100	°C	Industrial
DC core supply voltage. Must always power this pin.	V_{DD}	1.14	1.2	1.26	V	
Power supply for charge pumps (for normal operation and programming) for the 005, 010, 025, 050, 060 devices	V_{PP}	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Power supply for charge pumps (for normal operation and programming) for the 090 and 150 devices	V_{PP}	3.15	3.3	3.45	V	3.3 V range
Analog power pad for MDDR PLL	MSS_MDDR_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for MDDR PLL	HPMS_MDDR_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for FDDR PLL	FDDR_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for MDDR PLL	PLL0_PLL1_MSS_MDDR_V DDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for MDDR PLL	PLL0_PLL1_HPMS_MDDR_ VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for PLL0 to PLL5	CCC_XX[01]_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
High supply voltage for PLL SerDes[01]	SERDES_[01]_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power for SerDes[01] PLL Lane 0 to Lane 3. This is a 2.5 V SerDes internal PLL supply.	SERDES_[01]_L[0123]_VD DAPLL	2.375	2.5	2.625	V	
TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply.	SERDES_[01]_L[0123]_VD DAIO	1.14	1.2	1.26	V	
PCIe/PCS power supply	SERDES_[01]_VDD	1.14	1.2	1.26	V	
1.2 V DC supply voltage	V_{DDix}	1.14	1.2	1.26	V	
1.5 V DC supply voltage	V_{DDix}	1.425	1.5	1.575	V	
1.8 V DC supply voltage	V_{DDix}	1.71	1.8	1.89	V	
2.5 V DC supply voltage	V_{DDix}	2.375	2.5	2.625	V	

Table 4 • Recommended Operating Conditions (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
3.3 V DC supply voltage	V_{DDIX}	3.15	3.3	3.45	V	
LVDS differential I/O	V_{DDIX}	2.375	2.5	3.45	V	
B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O	V_{DDIX}	2.375	2.5	2.625	V	
LVPECL differential I/O	V_{DDIX}	3.15	3.3	3.45	V	
Reference voltage supply for FDDR (Bank0) and MDDR (Bank5)	V_{REFX}	0.49 × V_{DDIX}	0.5 × V_{DDIX}	0.51 × V_{DDIX}	V	
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to V_{PP} .	V_{PPNVM}	2.375 3.15	2.5 3.3	2.625 3.45	V	2.5 V range 3.3 V range

1. Programming at Industrial temperature range is available only with $V_{PP} = 3.3$ V.

Note: Power supply ramps must all be strictly monotonic, without plateaus.

Table 5 • FPGA Operating Limits

Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Digest Temperature	Digest Cycles	Retention (Biased/Unbiased)
Commercial	FPGA	Min $T_J = 0$ °C Max $T_J = 85$ °C	Min $T_J = 0$ °C Max $T_J = 85$ °C	500	Min $T_J = 0$ °C Max $T_J = 85$ °C	2000	20 years
Industrial ¹	FPGA	Min $T_J = -40$ °C Max $T_J = 100$ °C	Min $T_J = -40$ °C Max $T_J = 100$ °C	500	Min $T_J = -40$ °C Max $T_J = 100$ °C	2000	20 years

1. Programming at Industrial temperature range is available only with $V_{PP} = 3.3$ V.

Note: The retention specification is defined as the total number of programming and digest cycles. For example, 20 years of retention after 500 programming cycles.

Note: The digest cycle specification is 2000 digest cycles for every program cycle with a maximum of 500 programming cycles.

Note: If your product qualification requires accelerated programming cycles, see [Microsemi SoC Products Quality and Reliability Report](#) about recommended methodologies.

The following table lists the embedded operating flash limits.

Table 6 • Embedded Operating Flash Limits

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Commercial	Embedded flash	Min $T_J = 0\text{ }^\circ\text{C}$ Max $T_J = 85\text{ }^\circ\text{C}$	Min $T_J = 0\text{ }^\circ\text{C}$ Max $T_J = 85\text{ }^\circ\text{C}$	< 1000 cycles per page, up to two million cycles per eNVM array	20 years
				Min $T_J = 0\text{ }^\circ\text{C}$ Max $T_J = 85\text{ }^\circ\text{C}$	< 10000 cycles per page, up to 20 million cycles per eNVM array
Industrial	Embedded flash	Min $T_J = -40\text{ }^\circ\text{C}$ Max $T_J = 100\text{ }^\circ\text{C}$	Min $T_J = -40\text{ }^\circ\text{C}$ Max $T_J = 100\text{ }^\circ\text{C}$	< 1000 cycles per page, up to two million cycles per eNVM array	20 years
				Min $T_J = -40\text{ }^\circ\text{C}$ Max $T_J = 100\text{ }^\circ\text{C}$	< 10000 cycles per page, up to 20 million cycles per eNVM array

Note: If your product qualification requires accelerated programming cycles, see [Microsemi SoC Products Quality and Reliability Report](#) about recommended methodologies.

Table 7 • Device Storage Temperature and Retention

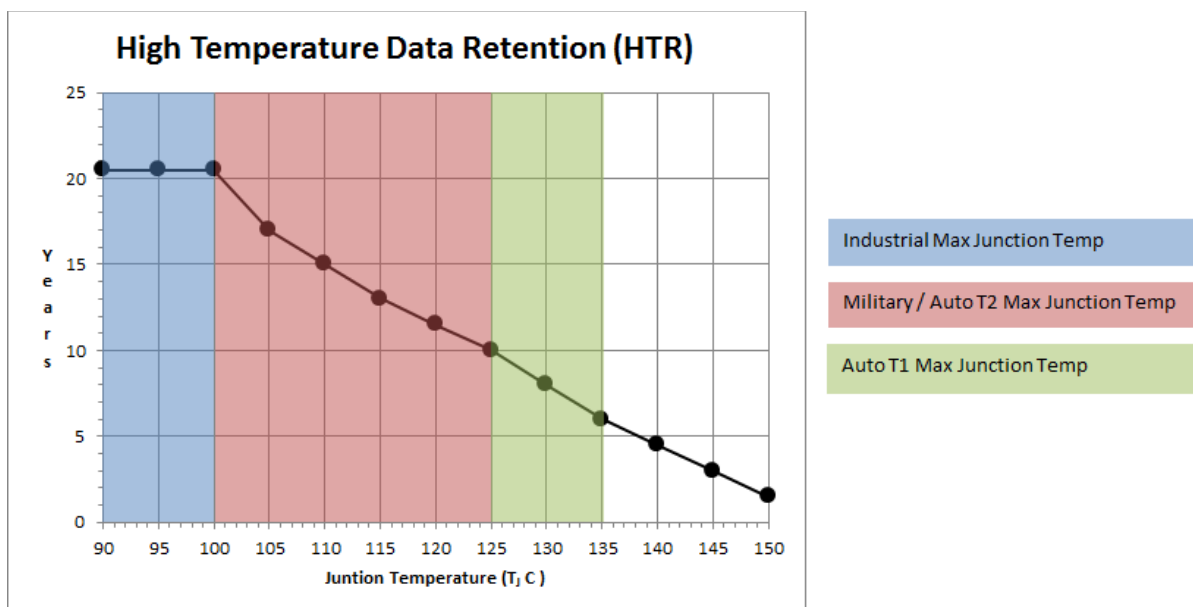
Product Grade	Storage Temperature (Tstg)	Retention
Commercial	Min $T_J = 0\text{ }^\circ\text{C}$ Max $T_J = 85\text{ }^\circ\text{C}$	20 years
Industrial	Min $T_J = -40\text{ }^\circ\text{C}$ Max $T_J = 100\text{ }^\circ\text{C}$	20 years

Table 8 • High Temperature Data Retention (HTR) Lifetime

T_J (C)	HTR Lifetime ¹ (yrs)
90	20.5
95	20.5
100	20.5
105	17.0
110	15.0
115	13.0
120	11.5
125	10.0
130	8.0
135	6.0
140	4.5
145	3.0
150	1.5

1. HTR Lifetime is the period during which a verify failure is not expected due to flash leakage.

Figure 1 • High Temperature Data Retention (HTR)



2.3.1.1 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to V_{CC1} + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

Note: The above specifications do not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant with the PCI standard including the PCI overshoot/undershoot specifications.

2.3.1.2 Thermal Characteristics

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ1 through EQ3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P} \tag{EQ 1}$$

$$\theta_{JB} = \frac{T_J - T_B}{P} \tag{EQ 2}$$

$$\theta_{JC} = \frac{T_J - T_C}{P} \tag{EQ 3}$$

Table 9 • Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices (continued)

Device	Still Air	1.0 m/s	2.5 m/s	θ_{JB}	θ_{JC}	Unit
	θ_{JA}					
150						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W
FCS536	15.01	12.06	10.76	3.69	1.55	°C/W
FCV484	16.21	13.11	11.84	6.73	0.10	°C/W

2.3.1.2.1 Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in the actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package with another.

The maximum power dissipation allowed is calculated using EQ4.

$$\text{Maximum power allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100 °C. EQ5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where:

$$\begin{aligned}\theta_{JA} &= 14.7 \text{ °C/W (taken from Table 9, page 10).} \\ T_A &= 85 \text{ °C}\end{aligned}$$

$$\text{Maximum power allowed} = \frac{100 \text{ °C} - 85 \text{ °C}}{14.7 \text{ °C/W}} = 1.088 \text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink may be attached to the top of the case, or the airflow inside the system must be increased.

2.3.1.2.2 Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from the junction to the board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

2.3.1.2.3 Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable to packages used with external heat sinks. Constant temperature is applied to the surface, which acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

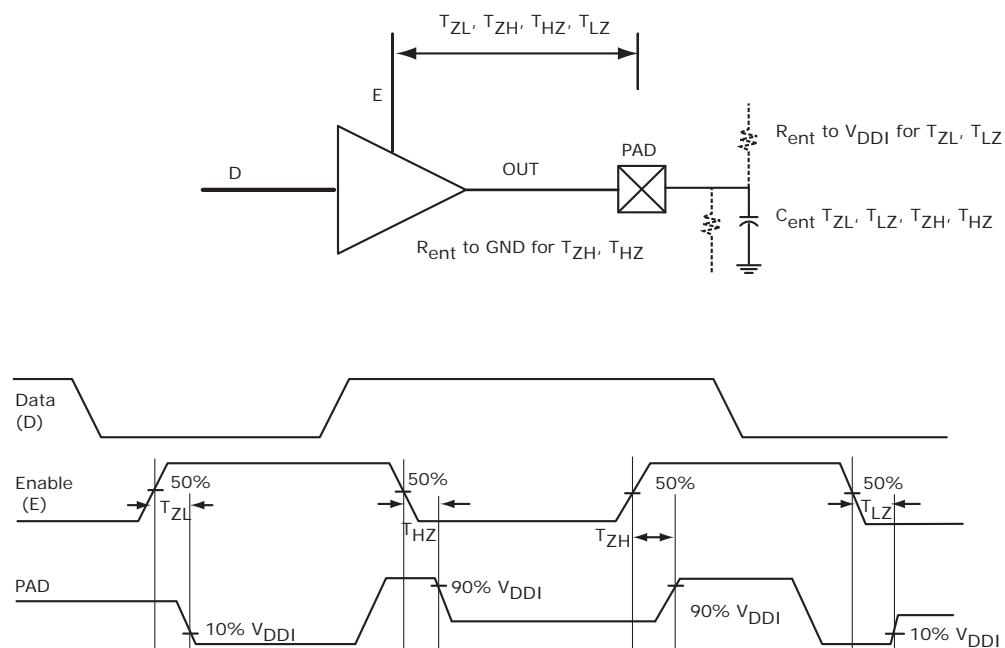
2.3.1.3 ESD Performance

See *RT0001: Microsemi Corporation - SoC Products Reliability Report* for information about ESD.

2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

Figure 5 • Tristate Buffer for Enable Path Test Point



2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

Table 18 • Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	630			Mbps
LVTTL 3.3 V	600			Mbps
LVC MOS 3.3 V	600			Mbps
LVC MOS 2.5 V	410	420	400	Mbps
LVC MOS 1.8 V	295	400	400	Mbps
LVC MOS 1.5 V	160	220	235	Mbps
LVC MOS 1.2 V	120	160	200	Mbps
LPDDR-LVC MOS 1.8 V mode			400	Mbps

Table 122 • SSTL18 DC Differential Voltage Specification

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID} (DC)	0.3	V

Table 123 • SSTL18 AC Differential Voltage Specifications (Applicable to DDRIO Bank Only)

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF} (AC)	0.5		V
AC differential cross point voltage	V_x (AC)	$0.5 \times V_{DDI} - 0.175$	$0.5 \times V_{DDI} + 0.175$	V

Table 124 • SSTL18 Minimum and Maximum AC Switching Speed (Applicable to DDRIO Bank Only)

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	667	Mbps	AC loading: per JEDEC specification

Table 125 • SSTL18 AC Impedance Specifications (Applicable to DDRIO Bank Only)

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	R_{REF}	20, 42	Ω	Reference resistor = 150 Ω
Effective impedance value (ODT)	R_{TT}	50, 75, 150	Ω	Reference resistor = 150 Ω

Table 126 • SSTL18 AC Test Parameter Specifications (Applicable to DDRIO Bank Only)

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.9	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for SSTL18 Class I (T_{DP})	R_{TT_TEST}	50	Ω
Reference resistance for data test path for SSTL18 Class II (T_{DP})	R_{TT_TEST}	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

Table 127 • DDR2/SSTL18 Receiver Characteristics for DDRIO I/O Bank with Fixed Code

	On-Die Termination (ODT)	T_{PY}		Unit
		-1	-Std	
Pseudo differential	None	1.567	1.844	ns
True differential	None	1.588	1.869	ns

Table 131 • SSTL15 DC Output Voltage Specification (for DDRIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DDR3/SSTL15 Class I (DDR3 Reduced Drive)				
DC output logic high	V_{OH}	$0.8 \times V_{DDI}$		V
DC output logic low	V_{OL}		$0.2 \times V_{DDI}$	V
Output minimum source DC current	I_{OH} at V_{OH}	6.5		mA
Output minimum sink current	I_{OL} at V_{OL}	-6.5		mA
DDR3/SSTL15 Class II (DDR3 Full Drive)				
DC output logic high	V_{OH}	$0.8 \times V_{DDI}$		V
DC output logic low	V_{OL}		$0.2 \times V_{DDI}$	V
Output minimum source DC current	I_{OH} at V_{OH}	7.6		mA
Output minimum sink current	I_{OL} at V_{OL}	-7.6		mA

Table 132 • SSTL15 DC Differential Voltage Specification (for DDRIO I/O Bank Only)

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID}	0.2	V

Note: To meet JEDEC electrical compliance, use DDR3 full drive transmitter.

Table 133 • SSTL15 AC SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF} (AC)	0.3		V
AC differential cross point voltage	V_x (AC)	$0.5 \times V_{DDI} - 0.150$	$0.5 \times V_{DDI} + 0.150$	V

Table 134 • SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	667	Mbps	AC loading: per JEDEC specifications

Table 135 • SSTL15 AC Calibrated Impedance Option (for DDRIO I/O Bank Only)

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	R_{REF}	34, 40	Ω	Reference resistor = 240 Ω
Effective impedance value (ODT)	R_{TT}	20, 30, 40, 60, 120	Ω	Reference resistor = 240 Ω

Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers) (continued)

	medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	medium_fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10 mA	slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	medium_fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12 mA	slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	medium_fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16 mA	slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	medium_fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO management).

2.3.7 Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

2.3.7.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

Minimum and Maximum Input and Output Levels

Table 160 • LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{DDI}	2.375	2.5	2.625	V	2.5 V range
Supply voltage	V_{DDI}	3.15	3.3	3.45	V	3.3 V range

Table 161 • LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit	Conditions
DC Input voltage	V_I	0	2.925	V	2.5 V range
DC input voltage	V_I	0	3.45	V	3.3 V range
Input current high ¹	I_{IH} (DC)				
Input current low ¹	I_{IL} (DC)				

1. See Table 24, page 22.

Table 162 • LVDS DC Output Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 163 • LVDS DC Differential Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
Differential output voltage swing	V_{OD}	250	350	450	mV
Output common mode voltage	V_{OCM}	1.125	1.25	1.375	V
Input common mode voltage	V_{ICM}	0.05	1.25	2.35	V
Input differential voltage	V_{ID}	100	350	600	mV

Table 164 • LVDS Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	535	Mbps	AC loading: 12 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank) no pre-emphasis	D_{MAX}	620	Mbps	AC loading: 10 pF / 100 Ω differential load
		700	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 165 • LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Max	Unit
Termination resistance	R_T	100		Ω

Table 166 • LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

LVDS25 AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 167 • LVDS25 Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.774	3.263	ns
100	2.775	3.264	ns

Table 168 • LVDS25 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.554	3.004	ns
100	2.549	2.999	ns

Table 169 • LVDS25 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.136	2.513	2.416	2.842	2.402	2.825	2.423	2.85	2.409	2.833	ns

Table 170 • LVDS25 Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
No pre-emphasis	1.61	1.893	1.749	2.058	1.735	2.041	1.897	2.231	1.866	2.195	ns
Min pre-emphasis	1.527	1.796	1.757	2.067	1.744	2.052	1.905	2.241	1.876	2.207	ns
Med pre-emphasis	1.496	1.76	1.765	2.077	1.751	2.06	1.914	2.252	1.884	2.216	ns

LVDS33 AC Switching Characteristics**Table 171 • LVDS33 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

On Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.572	3.025	ns
100	2.569	3.023	ns

Table 172 • LVDS33 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
1.942	2.284	1.98	2.33	1.97	2.318	1.953	2.298	1.96	2.307	ns

2.3.10.2 Timing Characteristics

The following table lists the combinatorial cell propagation delays in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 223 • Combinatorial Cell Propagation Delays

Combinatorial Cell	Equation	Symbol	-1	-Std	Unit
INV	$Y = !A$	T_{PD}	0.1	0.118	ns
AND2	$Y = A \cdot B$	T_{PD}	0.164	0.193	ns
NAND2	$Y = !(A \cdot B)$	T_{PD}	0.147	0.173	ns
OR2	$Y = A + B$	T_{PD}	0.164	0.193	ns
NOR2	$Y = !(A + B)$	T_{PD}	0.147	0.173	ns
XOR2	$Y = A \oplus B$	T_{PD}	0.164	0.193	ns
XOR3	$Y = A \oplus B \oplus C$	T_{PD}	0.225	0.265	ns
AND3	$Y = A \cdot B \cdot C$	T_{PD}	0.209	0.246	ns
AND4	$Y = A \cdot B \cdot C \cdot D$	T_{PD}	0.287	0.338	ns

2.3.10.3 Sequential Module

IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

Figure 15 • Sequential Module

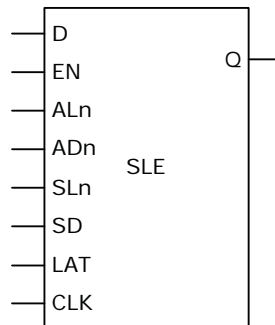


Table 233 • RAM1K18 – Dual-Port Mode for Depth x Width Configuration 4K x 4 (continued)

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register			0.323		0.38	ns
Read access time without pipeline register	T_{CLK2Q}		2.273		2.673	ns
Access time with feed-through write timing			1.511		1.778	ns
Address setup time	T_{ADDRSU}	0.543		0.638		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.334		0.393		ns
Data hold time	T_{DHD}	0.082		0.096		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		1.511		1.778	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.516		0.607		ns
Read enable hold time	T_{RDEHD}	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}		1.507		1.773	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	-0.279		-0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.458		0.539		ns
Write enable hold time	T_{WEHD}	0.048		0.057		ns
Maximum frequency	F_{MAX}		400		340	MHz

2.3.12.2 FPGA Fabric Micro SRAM (μ SRAM)

The following table lists the μ SRAM in 64×18 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 237 • μ SRAM (RAM64x18) in 64×18 Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register				1.677		1.973
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode			1.856		2.184	
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode			-0.778		-0.915	
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)			0.046		0.054	
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)			0.236		0.278	
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.839		0.987	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns

Table 243 • μ SRAM (RAM1024x1) in 1024 x 1 Mode (continued)

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.83		0.98	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.003		0.004		ns
Write input data hold time	T_{DINCHD}	0.137		0.161		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.247		0.29		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	-0.03		-0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

2.3.13 Programming Times

The following tables list the programming times in typical conditions when $T_J = 25\text{ }^\circ\text{C}$, $V_{DD} = 1.2\text{ V}$. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 244 • JTAG Programming (Fabric Only)

M2S/M2GL				
Device	Image size Bytes	Program	Verify	Unit
005	302672	22	10	Sec
010	568784	28	18	Sec
025	1223504	51	26	Sec
050	2424832	66	54	Sec
060	2418896	77	54	Sec
090	3645968	113	126	Sec
150	6139184	155	193	Sec

2.3.24 Power-up to Functional Times

The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 288 • Power-up to Functional Times for SmartFusion2

Symbol	From	To	Description	Maximum Power-up to Functional Time for SmartFusion2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	647	500	531	483	474	524	647
$T_{POR2MSSRST}$	POWER_ON_RESET_N	MSS_RESE T_N_M2F	Fabric to MSS	644	497	528	480	468	518	641
$T_{MSSRST2OUT}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.6	3.6	3.6	3.4	4.9	4.8	4.8
$T_{VDD2OUT}$	V_{DD}	Output available at I/O	V_{DD} at its minimum threshold level to output	3096	2975	3012	2959	2869	2992	3225
$T_{VDD2POR}$	V_{DD}	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	2476	2487	2496	2486	2406	2563	2602
$T_{VDD2MSSRST}$	V_{DD}	MSS_RESE T_N_M2F	V_{DD} at its minimum threshold level to MSS	3093	2972	3008	2956	2864	2987	3220
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see [UG0331: SmartFusion2 Microcontroller Subsystem User Guide](#).

Table 305 • SPI Characteristics for All Devices (continued)

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%–90%) ¹		2.906		ns	IO Configuration: LVCMOS 2.5 V-8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0 1]_DI setup time ²	12			ns	
sp9m	SPI_[0 1]_DI hold time ²	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0 1]_DI setup time ²	2			ns	
sp9s	SPI_[0 1]_DI hold time ²	7			ns	
SPI master configuration (applicable for 060, 090, and 150 devices)						
sp6m	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 7.0			ns	
sp7m	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) – 9.5			ns	
sp8m	SPI_[0 1]_DI setup time ²	15			ns	
sp9m	SPI_[0 1]_DI hold time ²	–2.5			ns	
SPI slave configuration (applicable for 060, 090, and 150 devices)						
sp6s	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 16.0			ns	
sp7s	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) – 3.5			ns	
sp8s	SPI_[0 1]_DI setup time ²	3			ns	
sp9s	SPI_[0 1]_DI hold time ²	2.5			ns	

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. For allowable pclk configurations, see Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.