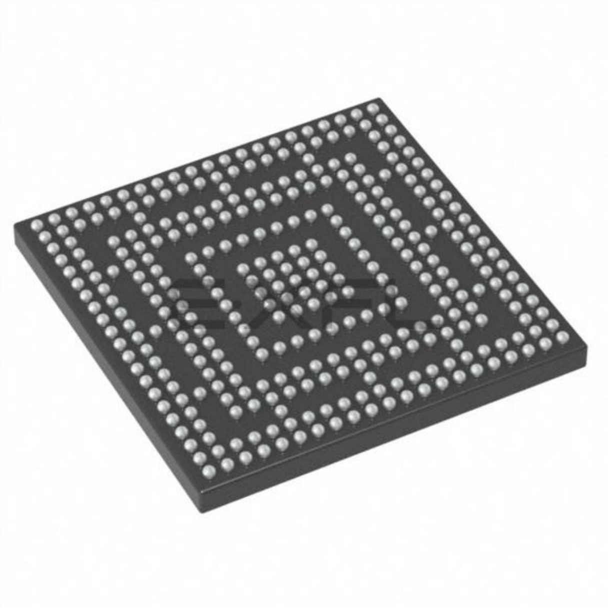

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Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | ARM® Cortex®-M3 |
| Flash Size | 256KB |
| RAM Size | 64KB |
| Peripherals | DDR, PCIe, SERDES |
| Connectivity | CANbus, Ethernet, I²C, SPI, UART/USART, USB |
| Speed | 166MHz |
| Primary Attributes | FPGA - 50K Logic Modules |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 325-TFBGA, FCBGA |
| Supplier Device Package | 325-FCBGA (11x11) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2s050ts-fcs325 |

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# 1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- Updated Table 24, page 22 with minimum and maximum values for input current low and high (SAR 73114 and 80314).
- Added Non-Deterministic Random Bit Generator (NRBG) Characteristics, page 106 (SAR 73114 and 79517).
- Added 060 device in Table 282, page 110 (SAR 79860).
- Added DEVRST_N to Functional Times, page 116 (SAR 73114).
- Added Cryptographic Block Characteristics, page 106 (SAR 73114 and 79516).
- Update Table 296, page 121 with VTX-AMP details (SAR 81756).
- Update note in Table 297, page 122 (SAR 74570 and 80677).
- Update Table 298, page 122 with generic EPCS details (SAR 75307).
- Added Table 308, page 129 (SAR 50424).

## 1.2 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

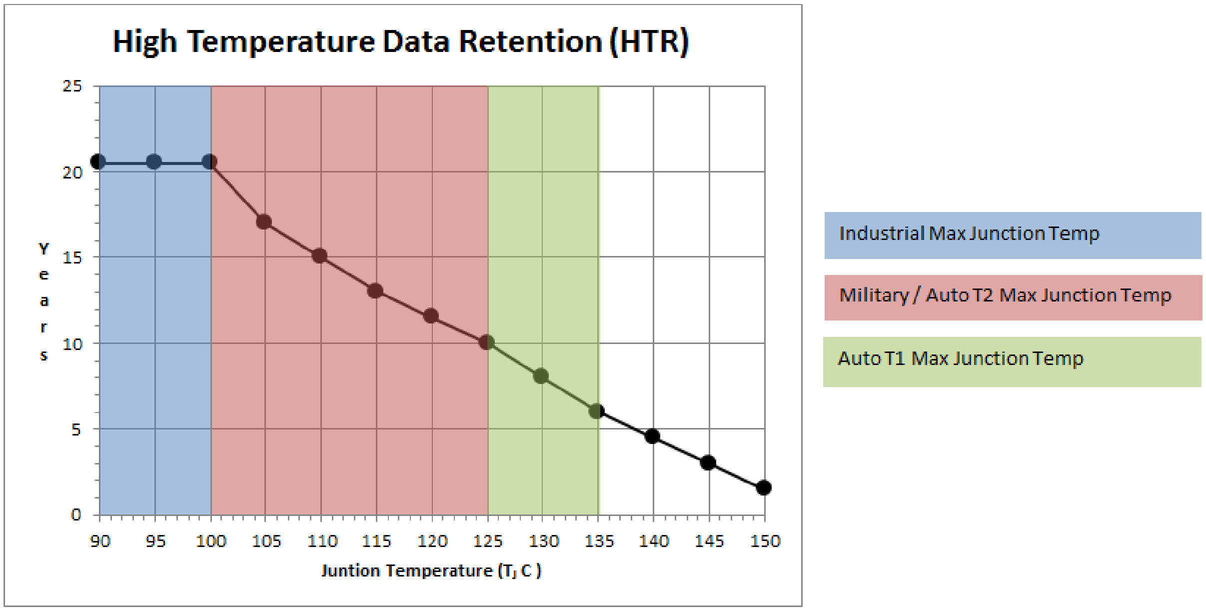
- The Surge Current on VDD during DEVRST_B Assertion and Surge Current on VDD during Digest Check using System Services tables were deleted and added reference to *AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note*. (SAR 76865 and 76623).
- Added 060 device in Table 4, page 6 (SAR 76383).
- Updated Table 24, page 22 for ramp time input (SAR 72103).
- Added 060 device details in Table 284, page 112 (SAR 74927).
- Updated Table 290, page 116 for name change (SAR 74925).
- Updated Table 283, page 111 for 060 FG676 Package details (SAR 78849).
- Updated Table 305, page 126 for SmartFusion2 and Table 310, page 129 for IGLOO2 for SPI timing and Fmax (SAR 56645, 75331).
- Updated Table 293, page 119 for Flash*Freeze entry and exit times (SAR 75329, 75330).
- Updated Table 297, page 122 for RX-CID information (SAR 78271).
- Added Table 8, page 8 and Figure 1, page 9 (SAR 78932).
- Updated Table 223, page 76 for timing characteristics and Table 224, page 77(SAR 75998).
- Added SRAM PUF, page 105 (SAR 64406).
- Added a footnote on digest cycle in Table 5, page 7 (SAR 79812).

## 1.3 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document.

- Added a note in Table 5, page 7 (SAR 71506).
- Added a note in Table 6, page 8 (SAR 74616).
- Added a note in Figure 3, page 17 (SAR 71506).
- Updated Quiescent Supply Current for 060 in Table 11, page 12 and Table 12, page 13 (SAR 74483).
- Updated programming currents for 060 in Table 13, page 13, Table 14, page 13, and Table 15, page 14.
- Added DEVRST_B assertion tables (SAR 74708).
- Updated I/O speeds for LVDS 3.3 V in Table 18, page 19 and Table 21, page 20 (SAR 69829).
- Updated Table 24, page 22 (SAR 69418).
- Updated Table 25, page 22, Table 26, page 23, Table 27, page 23 (SAR 74570).
- Updated all AC/DC table to link to the Input Capacitance, Leakage Current, and Ramp Time, page 22 for reference (SAR 69418).

***Figure 1 •*** **High Temperature Data Retention (HTR)**



## 2.3.1.1 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to –1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to $V_{CCI}$ + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

**Note:** The above specifications do not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant with the PCI standard including the PCI overshoot/undershoot specifications.

## 2.3.1.2 Thermal Characteristics

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ1 through EQ3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

*EQ 1*

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

*EQ 2*

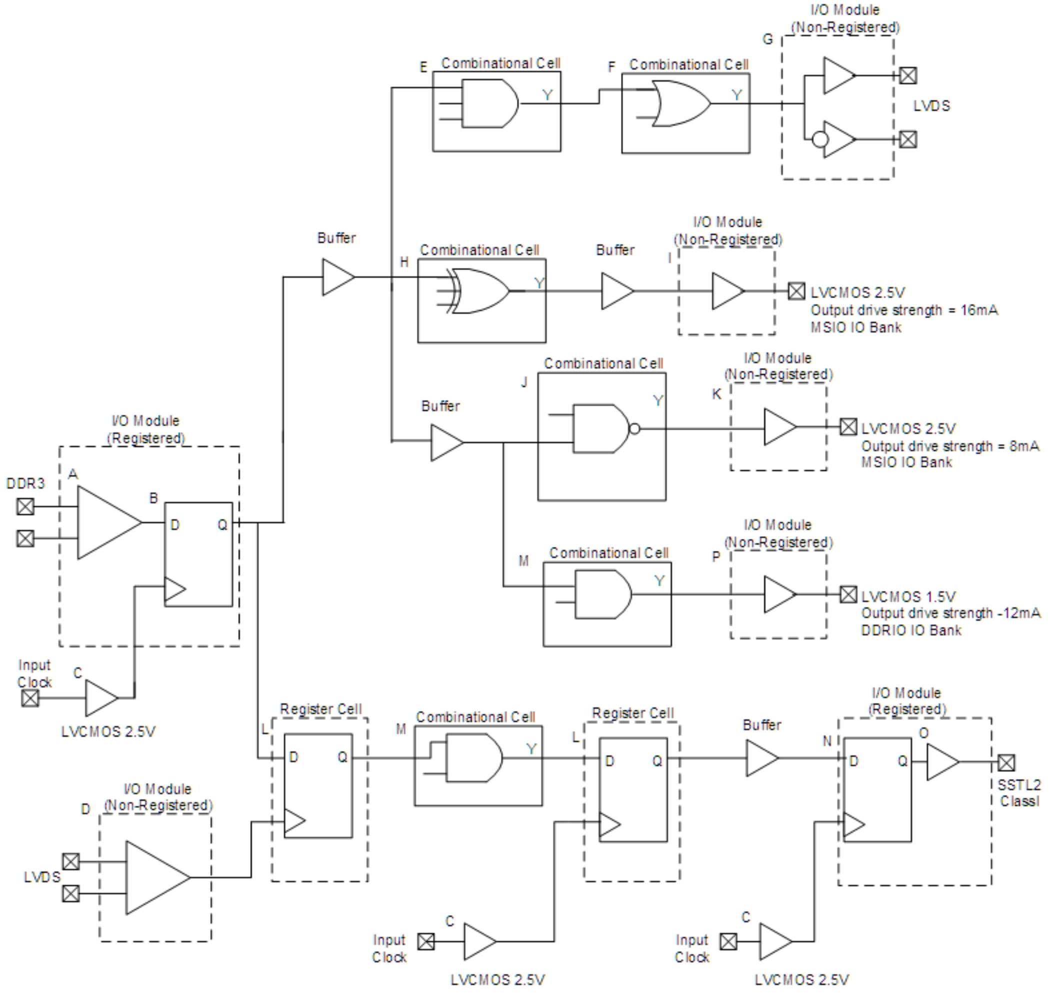
$$\theta_{JC} = \frac{T_J - T_C}{P}$$

*EQ 3*

## 2.3.4 Timing Model

This section describes timing model and timing parameters.

*Figure 2 •* **Timing Model**



The following table lists the timing model parameters in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

*Table 17 •* **Timing Model Parameters**

| Index | Symbol | Description | –1 | Unit | For More Information |
|---|---|---|---|---|---|
| A | $T_{PY}$ | Propagation delay of DDR3 receiver | 1.605 | ns | See Table 137, page 50 |
| B | $T_{ICLKQ}$ | Clock-to-Q of the input data register | 0.16 | ns | See Table 221, page 71 |
| | $T_{ISUD}$ | Setup time of the input data register | 0.357 | ns | See Table 221, page 71 |
| C | $T_{RCKH}$ | Input high delay for global clock | 1.53 | ns | See Table 227, page 78 |
| | $T_{RCKL}$ | Input low delay for global clock | 0.897 | ns | See Table 227, page 78 |
| D | $T_{PY}$ | Input propagation delay of LVDS receiver | 2.774 | ns | See Table 167, page 56 |
| E | $T_{DP}$ | Propagation delay of a three-input AND gate | 0.198 | ns | See Table 223, page 76 |

### 2.3.5.5 Detailed I/O Characteristics

***Table 24 •*** **Input Capacitance, Leakage Current, and Ramp Time**

| Symbol | Description | Maximum | Unit | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | 10 | pF | |
| $I_{IL}$ (dc) | Input current low<br>(Applicable to HSTL/SSTL inputs only) | 400 | µA | $V_{DDI}$ = 2.5 V |
| | | 500 | µA | $V_{DDI}$ = 1.8 V |
| | | 600 | µA | $V_{DDI}$ = 1.5 V[1] |
| | Input current low<br>(Applicable to all other digital inputs) | 10 | µA | |
| $I_{IH}$ (dc) | Input current high<br>(Applicable to HSTL/SSTL inputs only) | 400 | µA | $V_{DDI}$ = 2.5 V |
| | | 500 | µA | $V_{DDI}$ = 1.8 V |
| | | 600 | µA | $V_{DDI}$ = 1.5 V[1] |
| | Input current high<br>(Applicable to all other digital inputs) | 10 | µA | |
| $T_{RAMPIN}$[2] | Input ramp time<br>(Applicable to all digital inputs) | 50 | ns | |

1. Applicable when I/O pair is programmed with an HSTL/SSTL I/O type on IOP and an un-terminated I/O type (LVCMOS, for example) on ION pad.
2. Voltage ramp must be monotonic.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of DDRIO I/O bank at $V_{OH}/V_{OL}$ Level.

***Table 25 •*** **I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank**

| | R(WEAK PULL-UP) at $V_{OH}$ ($\Omega$) | | R(WEAK PULL-DOWN) at $V_{OL}$ ($\Omega$) | |
|---|---|---|---|---|
| $V_{DDI}$ Domain | Min | Max | Min | Max |
| 2.5 V[1, 2] | 10K | 17.8K | 9.98K | 18K |
| 1.8 V[1, 2] | 10.3K | 19.1K | 10.3K | 19.5K |
| 1.5 V[1, 2] | 10.6K | 20.2K | 10.6K | 21.1K |
| 1.2 V[1, 2] | 11.1K | 22.7K | 11.2K | 24.6K |

1. R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX).
2. R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN).

***Table 107 •*** **SSTL2 AC Differential Voltage Specifications**

| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** |
|---|---|---|---|---|
| AC input differential voltage | $V_{DIFF}$ (AC) | 0.7 | | V |
| AC differential cross point voltage | $V_x$ (AC) | 0.5 × $V_{DDI}$ – 0.2 | 0.5 × $V_{DDI}$ + 0.2 | V |

***Table 108 •*** **SSTL2 Minimum and Maximum AC Switching Speeds**

| **Parameter** | **Symbol** | **Max** | **Unit** | **Conditions** |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 400 | Mbps | AC loading: per JEDEC specifications |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 575 | Mbps | AC loading: 17pF load |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 700 | Mbps | AC loading: 3 pF / 50 Ω load |
| | | 510 | Mbps | AC loading: 17pF load |

***Table 109 •*** **SSTL2 AC Impedance Specifications**

| **Parameter** | **Typ** | **Unit** | **Conditions** |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | 20, 42 | Ω | Reference resistor = 150 Ω |

***Table 110 •*** **DDR1/SSTL2 AC Test Parameter Specifications**

| **Parameter** | **Symbol** | **Typ** | **Unit** |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 1.25 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for SSTL2 Class I ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Reference resistance for data test path for SSTL2 Class II ($T_{DP}$) | RTT_TEST | 25 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

### AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V

***Table 111 •*** **SSTL2 Receiver Characteristics for DDRIO I/O Bank (Input Buffers)**

| | **On-Die Termination (ODT)** | **$T_{PY}$** | | |
|---|---|---|---|---|
| | | **–1** | **–Std** | **Unit** |
| Pseudo differential | None | 1.549 | 1.821 | ns |
| True differential | None | 1.589 | 1.87 | ns |

**_Table 185 •_ M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

**_Table 186 •_ M-LVDS Differential Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Differential output voltage swing (for MSIO I/O bank only) | $V_{OD}$ | 300 | 650 | mV |
| Output common mode voltage (for MSIO I/O bank only) | $V_{OCM}$ | 0.3 | 2.1 | V |
| Input common mode voltage | $V_{ICM}$ | 0.3 | 1.2 | V |
| Input differential voltage | $V_{ID}$ | 50 | 2400 | mV |

**_Table 187 •_ M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | 500 | Mbps | AC loading: 2 pF / 100 Ω differential load |

**_Table 188 •_ M-LVDS AC Impedance Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Termination resistance | $R_T$ | 50 | Ω |

**_Table 189 •_ M-LVDS AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | Cross point | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |

### AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V

**_Table 190 •_ M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.738 | 3.221 | ns |
| 100 | 2.735 | 3.218 | ns |

***Table 221* • Input DDR Propagation Delays *(continued)***

| **Symbol** | **Description** | **Measuring Nodes (from, to)** | **–1** | **–Std** | **Unit** |
|---|---|---|---|---|---|
| $T_{DDRIWAL}$ | Asynchronous load minimum pulse width for input DDR | F, F | 0.304 | 0.357 | ns |
| $T_{DDRICKMPWH}$ | Clock minimum pulse width high for input DDR | B, B | 0.075 | 0.088 | ns |
| $T_{DDRICKMPWL}$ | Clock minimum pulse width low for input DDR | B, B | 0.159 | 0.187 | ns |

### 2.3.9.4 Output DDR Module

**Figure 12 • Output DDR Module**

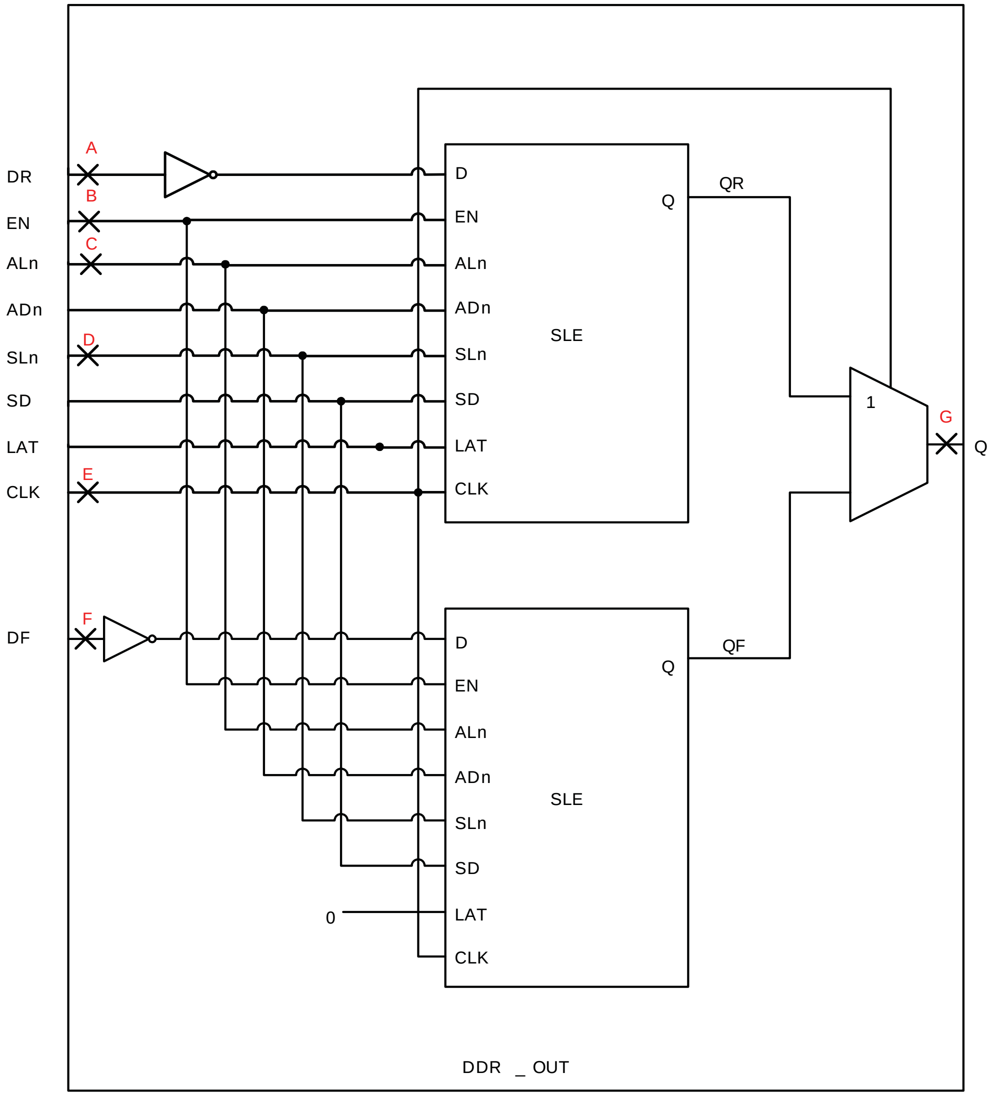


***Table 222 •*** **Output DDR Propagation Delays *(continued)***

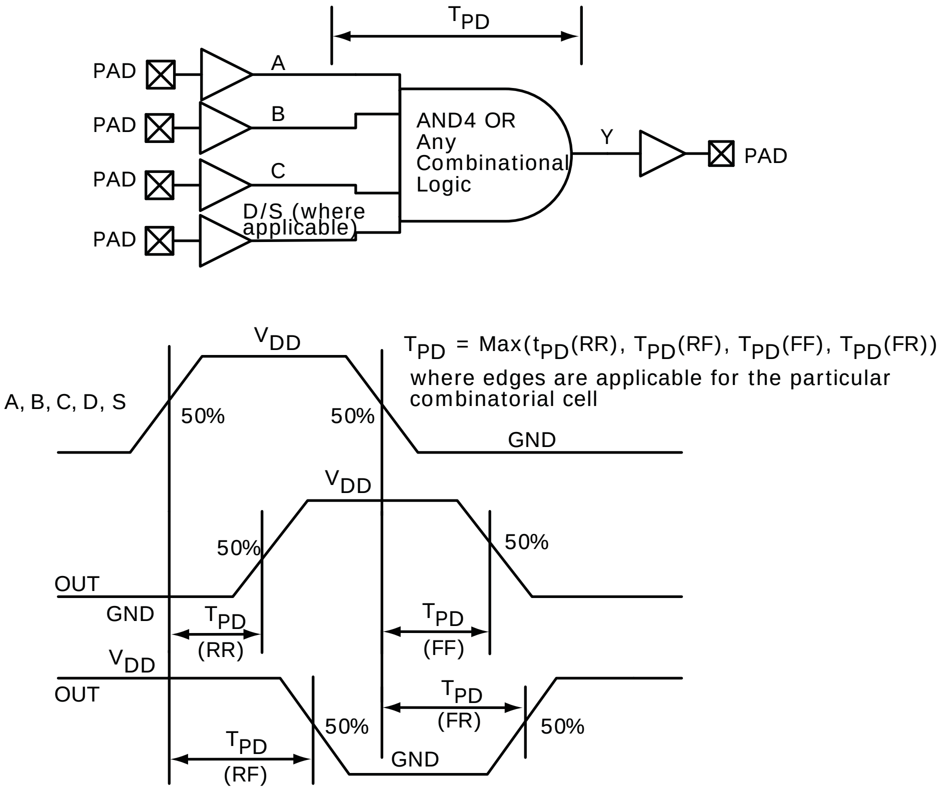
| Symbol | Description | Measuring Nodes (from, to) | –1 | –Std | Unit |
|---|---|---|---|---|---|
| $T_{DDROWAL}$ | Asynchronous load minimum pulse width for output DDR | C, C | 0.304 | 0.357 | ns |
| $T_{DDROCKMPWH}$ | Clock minimum pulse width high for the output DDR | E, E | 0.075 | 0.088 | ns |
| $T_{DDROCKMPWL}$ | Clock minimum pulse width low for the output DDR | E, E | 0.159 | 0.187 | ns |

## 2.3.10 Logic Element Specifications

### 2.3.10.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, see *SmartFusion2 and IGLOO2 Macro Library Guide*.

***Figure 14 •*** **LUT-4**



## 2.3.11 Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for the positions of various global routing resources.

The following table lists the 150 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 225 •*** **150 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.83 | 0.911 | 0.831 | 0.913 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.457 | 1.588 | 1.715 | 1.869 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.131 | | 0.154 | ns |

The following table lists the 090 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 226 •*** **090 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.835 | 0.888 | 0.833 | 0.886 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.405 | 1.489 | 1.654 | 1.752 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.084 | | 0.098 | ns |

The following table lists the 050 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 227 •*** **050 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.827 | 0.897 | 0.826 | 0.896 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.419 | 1.53 | 1.671 | 1.8 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.111 | | 0.129 | ns |

The following table lists the 025 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 228 •*** **025 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.747 | 0.799 | 0.745 | 0.797 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.294 | 1.378 | 1.522 | 1.621 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.084 | | 0.099 | ns |

The following table lists the 010 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

**Table 229 • 010 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.626 | 0.669 | 0.627 | 0.668 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.112 | 1.182 | 1.308 | 1.393 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.07 | | 0.085 | ns |

The following table lists the 005 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

**Table 230 • 005 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.625 | 0.66 | 0.628 | 0.66 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.126 | 1.187 | 1.325 | 1.397 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.061 | | 0.072 | ns |

## 2.3.12 FPGA Fabric SRAM

See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for more information.

### 2.3.12.1 FPGA Fabric Large SRAM (LSRAM)

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 1K × 18 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

**Table 231 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.334 | | 0.393 | ns |
| Read access time without pipeline register | | | 2.273 | | 2.674 | ns |
| Access time with feed-through write timing | | | 1.529 | | 1.799 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.441 | | 0.519 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.341 | | 0.401 | | ns |
| Data hold time | $T_{DHD}$ | 0.107 | | 0.126 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |

**Table 239 •** **µSRAM (RAM128x9) in 128 × 9 Mode *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.023 | | –0.027 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.835 | | 0.982 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.115 | | 0.135 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.15 | | 0.177 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.128 | | 0.15 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.026 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 128 × 8 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

**Table 240 •** **µSRAM (RAM128x8) in 128 × 8 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.266 | | 0.313 | ns |
| Read access time without pipeline register | | | 1.677 | | 1.973 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.856 | | 2.184 | | ns |

The following table lists the µSRAM in 256 × 4 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 241 •*** **µSRAM (RAM256x4) in 256 × 4 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.27 | | 0.31 | ns |
| Read access time without pipeline register | | | 1.75 | | 2.06 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.931 | | 2.272 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.121 | | 0.142 | | ns |
| Read address hold time in asynchronous mode | | –0.65 | | –0.76 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.77 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.09 | | 2.46 | ns |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.02 | | –0.03 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.83 | | 0.98 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.101 | | 0.118 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.137 | | 0.161 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |

***Table 245 •*** **JTAG Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 137536 | 39 | 4 | Sec |
| 010 | 274816 | 78 | 9 | Sec |
| 025 | 274816 | 78 | 9 | Sec |
| 050 | 278528 | 84 | 8 | Sec |
| 060 | 268480 | 76 | 8 | Sec |
| 090 | 544496 | 154 | 15 | Sec |
| 150 | 544496 | 155 | 15 | Sec |

***Table 246 •*** **JTAG Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 439296 | 59 | 11 | Sec |
| 010 | 842688 | 107 | 20 | Sec |
| 025 | 1497408 | 120 | 35 | Sec |
| 050 | 2695168 | 162 | 59 | Sec |
| 060 | 2686464 | 158 | 70 | Sec |
| 090 | 4190208 | 266 | 147 | Sec |
| 150 | 6682768 | 316 | 231 | Sec |

***Table 247 •*** **2 Step IAP Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 302672 | 4 | 17 | 6 | Sec |
| 010 | 568784 | 7 | 23 | 12 | Sec |
| 025 | 1223504 | 14 | 33 | 23 | Sec |
| 050 | 2424832 | 29 | 52 | 40 | Sec |
| 060 | 2418896 | 39 | 61 | 50 | Sec |
| 090 | 3645968 | 60 | 84 | 73 | Sec |
| 150 | 6139184 | 100 | 132 | 120 | Sec |

***Table 277 •*** **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)** ***(continued)***

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 0.8 | ms | 005, 010, 025, and 050 devices |
| | | | | 1.0 | ms | 090 and 150 devices |

***Table 278 •*** **Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 2 | | MHz | |
| Accuracy | ACCXTAL | | | 0.00105 | % | 050 devices |
| | | | | 0.003 | % | 005, 010, 025, 090, and 150 devices |
| | | | | 0.004 | % | 060 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 1 | 5 | ns | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 1 | 5 | ns | |
| Operating current | IDYNXTAL | | 0.3 | | mA | |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 4.5 | ms | 010 and 050 devices |
| | | | | 5 | ms | 005 and 025 devices |
| | | | | 7 | ms | 090 and 150 devices |

***Table 279 •*** **Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 32 | | kHz | |
| Accuracy | ACCXTAL | | | 0.004 | % | 005, 010, 025, 050, 060, and 090 devices |
| | | | | 0.005 | % | 150 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 150 | 300 | ns | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 150 | 300 | ns | |
| Operating current | IDYNXTAL | | 0.044 | | mA | 010 and 050 devices |
| | | | 0.060 | | mA | 005, 025, 060, 090, and 150 devices |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 115 | ms | 005, 025, 050, 090, and 150 devices |
| | | | | 126 | ms | 010 devices |

## 2.3.21 Clock Conditioning Circuits (CCC)

The following table lists the CCC/PLL specifications in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 282 •*** **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Clock conditioning circuitry input frequency $F_{IN\_CCC}$ | 1 | | 200 | MHz | All CCC |
| | 0.032 | | 200 | MHz | 32 kHz capable CCC |
| Clock conditioning circuitry output frequency $F_{OUT\_CCC}$[1] | 0.078 | | 400 | MHz | |
| PLL VCO frequency[2] | 500 | | 1000 | MHz | |
| Delay increments in programmable delay blocks | | 75 | 100 | ps | |
| Number of programmable values in each programmable delay block | | | 64 | | |
| Acquisition time | | 70 | 100 | µs | $F_{IN}$ >= 1 MHz |
| | | 1 | 16 | ms | $F_{IN}$ = 32 kHz |
| Input duty cycle (reference clock) | | | | | Internal Feedback |
| | 10 | | 90 | % | 1 MHz ≤ $F_{IN\_CCC}$ ≤ 25 MHz |
| | 25 | | 75 | % | 25 MHz ≤ $F_{IN\_CCC}$≤ 100 MHz |
| | 35 | | 65 | % | 100 MHz ≤ $F_{IN\_CCC}$ ≤ 150 MHz |
| | 45 | | 55 | % | 150 MHz ≤ $F_{IN\_CCC}$ ≤ 200 MHz |
| | | | | | External Feedback (CCC, FPGA, Off-chip) |
| | 25 | | 75 | % | 1 MHz ≤ $F_{IN\_CCC}$ ≤ 25 MHz |
| | 35 | | 65 | % | 25 MHz ≤ $F_{IN\_CCC}$ ≤ 35 MHz |
| | 45 | | 55 | % | 35 MHz ≤ $F_{IN\_CCC}$ ≤ 50 MHz |
| Output duty cycle | 48 | | 52 | % | 050 devices $F_{OUT}$ ≤ 400 MHz |
| | 48 | | 52 | % | 005, 010, and 025 devices $F_{OUT}$ < 350 MHz |
| | 46 | | 54 | % | 005, 010, and 025 devices 350 MHz ≤ $F_{out}$ ≤ 400 MHz |
| | 48 | | 52 | % | 060 and 090 devices $F_{OUT}$ ≤ 100 MHz |
| | 44 | | 52 | % | 060 and 090 devices 100 MHz ≤ $F_{OUT}$ ≤ 400 MHz |
| | 48 | | 52 | % | 150 devices $F_{OUT}$ ≤ 120 MHz |
| | 45 | | 52 | % | 150 devices 120 MHz ≤ $F_{OUT}$ ≤ 400 MHz |
| **Spread Spectrum Characteristics** | | | | | |
| Modulation frequency range | 25 | 35 | 50 | k | |
| Modulation depth range | 0 | | 1.5 | % | |
| Modulation depth control | | 0.5 | | % | |

## 2.3.24 Power-up to Functional Times

The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 288 •*** **Power-up to Functional Times for SmartFusion2**

| | | | | Maximum Power-up to Functional Time for SmartFusion2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **From** | **To** | **Description** | **005** | **010** | **025** | **050** | **060** | **090** | **150** |
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 647 | 500 | 531 | 483 | 474 | 524 | 647 |
| $T_{POR2MSSRST}$ | POWER_ON_RESET_N | MSS_RESET_N_M2F | Fabric to MSS | 644 | 497 | 528 | 480 | 468 | 518 | 641 |
| $T_{MSSRST2OUT}$ | MSS_RESET_N_M2F | Output available at I/O | MSS to output | 3.6 | 3.6 | 3.6 | 3.4 | 4.9 | 4.8 | 4.8 |
| $T_{VDD2OUT}$ | $V_{DD}$ | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 3096 | 2975 | 3012 | 2959 | 2869 | 2992 | 3225 |
| $T_{VDD2POR}$ | $V_{DD}$ | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 2476 | 2487 | 2496 | 2486 | 2406 | 2563 | 2602 |
| $T_{VDD2MSSRST}$ | $V_{DD}$ | MSS_RESET_N_M2F | $V_{DD}$ at its minimum threshold level to MSS | 3093 | 2972 | 3008 | 2956 | 2864 | 2987 | 3220 |
| $T_{VDD2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2500 | 2487 | 2509 | 2475 | 2507 | 2519 | 2617 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2504 | 2491 | 2510 | 2478 | 2517 | 2525 | 2620 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2479 | 2468 | 2493 | 2458 | 2486 | 2499 | 2595 |

**Note:** For more information about power-up times, see *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

### 2.3.31.2 SmartFusion2 Inter-Integrated Circuit ($I^2C$) Characteristics

This section describes the DC and switching of the $I^2C$ interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, see Figure 21, page 125.

The following table lists the $I^2C$ characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V

***Table 303 •*** **I2C Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Input low voltage | $V_{IL}$ | –0.3 | | 0.8 | V | See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive. |
| Input high voltage | $V_{IH}$ | 2 | | 3.45 | V | See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive. |
| Hysteresis of schmitt triggered inputs for $V_{DDI}$ > 2 V | $V_{HYS}$ | $0.05 \times V_{DDI}$ | | | V | See Table 28, page 23 for more information. |
| Input current high | $I_{IL}$ | | | 10 | µA | See Single-Ended I/O Standards, page 24 for more information. |
| Input current low | $I_{IH}$ | | | 10 | µA | See Single-Ended I/O Standards, page 24 for more information. |
| Input rise time | $T_{ir}$ | | | 1000 | ns | Standard mode |
| | | | | 300 | ns | Fast mode |
| Input fall time | $T_{if}$ | | | 300 | ns | Standard mode |
| | | | | 300 | ns | Fast mode |
| Maximum output voltage low (open drain) at 3 mA sink current for $V_{DDI}$ > 2 V | $V_{OL}$ | | | 0.4 | V | See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive. |
| Pin capacitance | Cin | | | 10 | pF | $V_{IN}$ = 0, f = 1.0 MHz |
| Output fall time from VIHMin to VILMax[1] | $t_{OF}$[1] | | 21.04 | | ns | $V_{IHmin}$ to $V_{ILMax}$, CLOAD = 400 pF |
| | | | 5.556 | | ns | $V_{IHmin}$ to $V_{ILMax}$, CLOAD = 100 pF |
| Output rise time from VILMax to VIHMin[1] | $t_{OR}$ [1] | | 19.887 | | ns | $V_{ILMax}$ to $V_{IHmin}$, CLOAD = 400 pF |
| | | | 5.218 | | ns | $V_{ILMax}$ to $V_{IHmin}$, CLOAD = 100 pF |
| Output buffer maximum pull-down resistance[2, 3] | $R_{pull-up}$[2,3] | | | 50 | Ω | |
| Output buffer maximum pull-up resistance[2, 4] | $R_{pull-down}$[2,4] | | | 131.25 | Ω | |