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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 50K Logic Modules
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	325-TFBGA, FCBGA
Supplier Device Package	325-FCBGA (11x11)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s050ts-fcsg325i">https://www.e-xfl.com/product-detail/microchip-technology/m2s050ts-fcsg325i</a>

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## 2.2 References

The following documents are recommended references:

- *PB0121: IGLOO2 Product Brief*
- *DS0124: IGLOO2 Pin Descriptions*
- *PB0115: SmartFusion2 SoC FPGA Product Brief*
- *DS0115: SmartFusion2 Pin Descriptions*

All product documentation for IGLOO2 and SmartFusion2 is available at:

<http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga>

<http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#overview>

## 2.3 Electrical Specifications

### 2.3.1 Operating Conditions

The following table lists the stress limits. Stress applied above the specified limit may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table are not implied.

**Table 3 • Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Unit
DC core supply voltage. Must always power this pin.	$V_{DD}$	-0.3	1.32	V
Power supply for charge pumps (for normal operation and programming). Must always power this pin.	$V_{PP}$	-0.3	3.63	V
Analog power pad for MDDR PLL	MSS_MDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	HPMS_MDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for FDDR PLL	FDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_MSS_MDDR_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_HPMS_MDDR_VDDA	-0.3	3.63	V
Analog power pad for PLL0-5	CCC_XX[01]_PLL_VDDA	-0.3	3.63	V
High supply voltage for PLL SerDes[01]	SERDES_[01]_PLL_VDDA	-0.3	3.63	V
Analog power for SerDes[01] PLL lane0 to lane3. This is a 2.5 V SerDes internal PLL supply.	SERDES_[01]_L[0123]_VDDAPLL	-0.3	2.75	V
TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply.	SERDES_[01]_L[0123]_VDDAIO	-0.3	1.32	V
PCIe/PCS power supply	SERDES_[01]_VDD	-0.3	1.32	V
DC FPGA I/O buffer supply voltage for MSIO I/O bank	$V_{DDIx}$	-0.3	3.63	V
DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks	$V_{DDIx}$	-0.3	2.75	V
I/O Input voltage for MSIO I/O bank	$V_I$	-0.3	3.63	V
I/O Input voltage for MSIOD/DDRIO I/O bank	$V_I$	-0.3	2.75	V
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to $V_{PP}$ .	$V_{PPNVM}$	-0.3	3.63	V
Storage temperature <sup>1</sup>	$T_{STG}$	-65	150	°C
Junction temperature	$T_J$	-55	135	°C

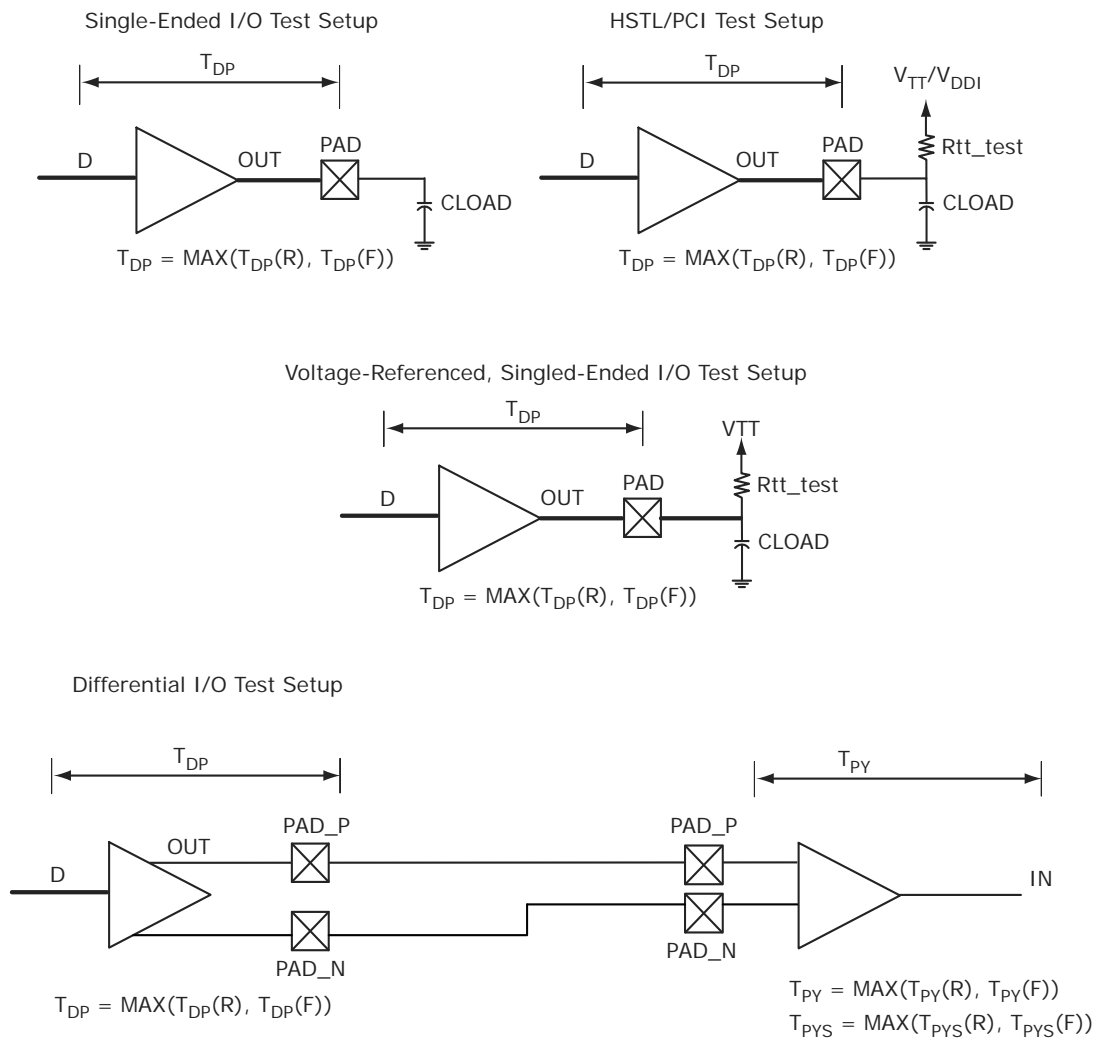
**Table 17 • Timing Model Parameters (continued)**

Index	Symbol	Description	-1	Unit	For More Information
F	$T_{DP}$	Propagation delay of an OR gate	0.179	ns	See Table 223, page 76
G	$T_{DP}$	Propagation delay of an LVDS transmitter	2.136	ns	See Table 169, page 57
H	$T_{DP}$	Propagation delay of a three-input XOR Gate	0.241	ns	See Table 223, page 76
I	$T_{DP}$	Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 16 mA on the MSIO bank	2.412	ns	See Table 46, page 27
J	$T_{DP}$	Propagation delay of a two-input NAND gate	0.179	ns	See Table 223, page 76
K	$T_{DP}$	Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 8 mA on the MSIO bank	2.309	ns	See Table 46, page 27
L	$T_{CLKQ}$	Clock-to-Q of the data register	0.108	ns	See Table 224, page 77
	$T_{SUD}$	Setup time of the data register	0.254	ns	See Table 224, page 77
M	$T_{DP}$	Propagation delay of a two-input AND gate	0.179	ns	See Table 223, page 76
N	$T_{OCLKQ}$	Clock-to-Q of the output data register	0.263	ns	See Table 220, page 69
	$T_{OSUD}$	Setup time of the output data register	0.19	ns	See Table 220, page 69
O	$T_{DP}$	Propagation delay of SSTL2, Class I transmitter on the MSIO bank	2.055	ns	See Table 114, page 45
P	$T_{DP}$	Propagation delay of LVCMOS 1.5 V transmitter, drive strength of 12 mA, fast slew on the DDRIO bank	3.316	ns	See Table 70, page 34

### 2.3.5.2 Output Buffer and AC Loading

The following figure shows the output buffer and AC loading.

**Figure 4 • Output Buffer AC Loading**



**Table 43 • LVCMOS 2.5 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	1.2	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega\sigma$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**Table 44 • LVCMOS 2.5 V Transmitter Drive Strength Specifications**

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (With Software Default Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	4 mA	4 mA	$V_{DDI} - 0.4$	0.4	4	4
6 mA	6 mA	6 mA	$V_{DDI} - 0.4$	0.4	6	6
8 mA	8 mA	8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	12 mA	12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA		16 mA	$V_{DDI} - 0.4$	0.4	16	16

**Note:** For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at:  
[www.microsemi.com/soc/download/ibis/default.aspx](http://www.microsemi.com/soc/download/ibis/default.aspx).

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

**Table 45 • LVCMOS 2.5 V Receiver Characteristics (Input Buffers)**

	On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
		-1	-Std	-1	-Std	
LVCMOS 2.5 V (for DDRIO I/O bank)	None	1.823	2.145	1.932	2.274	ns
LVCMOS 2.5 V (for MSIO I/O bank)	None	2.486	2.925	2.495	2.935	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	None	2.29	2.694	2.305	2.712	ns

**Table 46 • LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.657	4.302	3.393	3.991	3.675	4.323	3.894	4.582	3.552	4.18	ns
	Medium	3.374	3.97	3.139	3.693	3.396	3.995	3.635	4.277	3.253	3.828	ns
	Medium fast	3.239	3.811	3.036	3.572	3.261	3.836	3.519	4.141	3.128	3.681	ns
	Fast	3.224	3.793	3.029	3.563	3.246	3.818	3.512	4.132	3.119	3.67	ns

**Table 118 • DDR1/SSTL2 Class II Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.29	2.693	1.988	2.338	1.978	2.326	1.989	2.34	1.979	2.328	ns
Differential	2.418	2.846	2.304	2.711	2.297	2.702	2.131	2.506	2.124	2.499	ns

#### 2.3.6.4 Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 119 • SSTL18 DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	1.71	1.8	1.89	V
Termination voltage	$V_{TT}$	0.838	0.900	0.964	V
Input reference voltage	$V_{REF}$	0.838	0.900	0.964	V

**Table 120 • SSTL18 DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}$ (DC)	$V_{REF} + 0.125$	1.89	V
DC input logic low	$V_{IL}$ (DC)	-0.3	$V_{REF} - 0.125$	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 121 • SSTL18 DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
<b>SSTL18 Class I (DDR2 Reduced Drive)</b>				
DC output logic high	$V_{OH}$	$V_{TT} + 0.603$		V
DC output logic low	$V_{OL}$		$V_{TT} - 0.603$	V
Output minimum source DC current (DDRIO I/O bank only)	$I_{OH}$ at $V_{OH}$	6.5		mA
Output minimum sink current (DDRIO I/O bank only)	$I_{OL}$ at $V_{OL}$	-6.5		mA
<b>SSTL18 Class II (DDR2 Full Drive)<sup>1</sup></b>				
DC output logic high	$V_{OH}$	$V_{TT} + 0.603$		V
DC output logic low	$V_{OL}$		$V_{TT} - 0.603$	V
Output minimum source DC current (DDRIO I/O bank only)	$I_{OH}$ at $V_{OH}$	13.4		mA
Output minimum sink current (DDRIO I/O bank only)	$I_{OL}$ at $V_{OL}$	-13.4		mA

1. To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.



**Table 144 • LPDDR AC Differential Voltage Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	$V_{DIFF}$	$0.6 \times V_{DDI}$		V
AC differential cross point voltage	$V_x$	$0.4 \times V_{DDI}$	$0.6 \times V_{DDI}$	V

**Table 145 • LPDDR AC Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	$D_{MAX}$	400	Mbps	AC loading: per JEDEC specifications

**Table 146 • LPDDR AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	$R_{REF}$	20, 42	$\Omega$	Reference resistor = 150 $\Omega$
Effective impedance value (ODT)	$R_{TT}$	50, 70, 150	$\Omega$	Reference resistor = 150 $\Omega$

**Table 147 • LPDDR AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	0.9	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Reference resistance for data test path for LPDDR ( $T_{DP}$ )	$R_{TT\_TEST}$	50	$\Omega$
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	$\Omega$

#### AC Switching Characteristics

Worst-case commercial conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ , worst-case  $V_{DDI}$ .

**Table 148 • LPDDR Receiver Characteristics for DDRIO I/O Bank with Fixed Codes**

		$T_{PY}$		Unit
		On-Die Termination (ODT) -1	-Std	
Pseudo differential	None	1.568	1.845	ns
True differential	None	1.588	1.869	ns

**Table 149 • LPDDR Reduced Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ENZL}$		$T_{ENZH}$		$T_{ENHZ}$		$T_{ENLZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.383	2.804	2.23	2.623	2.229	2.622	2.202	2.591	2.201	2.59	ns
Differential	2.396	2.819	2.764	3.252	2.764	3.252	2.255	2.653	2.255	2.653	ns

**Table 191 • M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

On-Die Termination (ODT)	T <sub>PY</sub>		Unit
	-1	-Std	
None	2.495	2.934	ns
100	2.495	2.935	ns

**Table 192 • M-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub>		T <sub>LZ</sub>		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.258	2.656	2.348	2.762	2.334	2.746	2.123	2.497	2.125	2.5	ns

### 2.3.7.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

#### Mini-LVDS Minimum and Maximum Input and Output Levels

**Table 193 • Mini-LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>DDI</sub>	2.375	2.5	2.625	V

**Table 194 • Mini-LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	V <sub>I</sub>	0	2.925	V

**Table 195 • Mini-LVDS DC Output Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V <sub>OH</sub>	1.25	1.425	1.6	V
DC output logic low	V <sub>OL</sub>	0.9	1.075	1.25	V

**Table 196 • Mini-LVDS DC Differential Voltage Specification**

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing	V <sub>OD</sub>	300	600	mV
Output common mode voltage	V <sub>OCM</sub>	1	1.4	V
Input common mode voltage	V <sub>ICM</sub>	0.3	1.2	V
Input differential voltage	V <sub>ID</sub>	100	600	mV

**Table 197 • Mini-LVDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D <sub>MAX</sub>	520	Mbps	AC loading: 2 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank)	D <sub>MAX</sub>	700	Mbps	AC loading: 2 pF / 100 Ω differential load

**Table 215 • LVPECL DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	$V_I$	0	3.45	V

**Table 216 • LVPECL DC Differential Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
Input common mode voltage	$V_{ICM}$	0.3		2.8	V
Input differential voltage	$V_{IDIFF}$	100	300	1,000	mV

**Table 217 • LVPECL Minimum and Maximum AC Switching Speeds**

Parameter	Symbol	Max	Unit
Maximum data rate	$D_{MAX}$	900	Mbps

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$ .

**Table 218 • LVPECL Receiver Characteristics for MSIO I/O Bank**

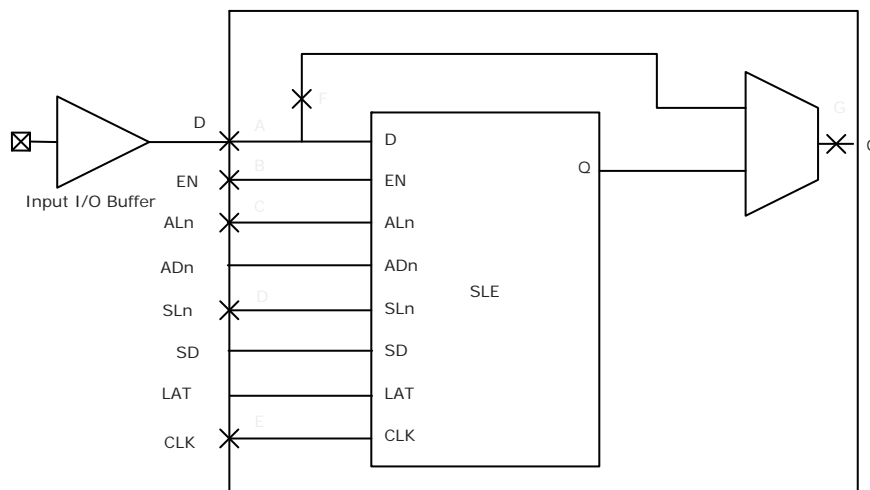
On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.572	3.025	ns
100	2.569	3.023	ns

**2.3.8 I/O Register Specifications**

This section describes input and output register specifications.

**2.3.8.1 Input Register**

**Figure 6 • Timing Model for Input Register**



**Table 222 • Output DDR Propagation Delays (continued)**

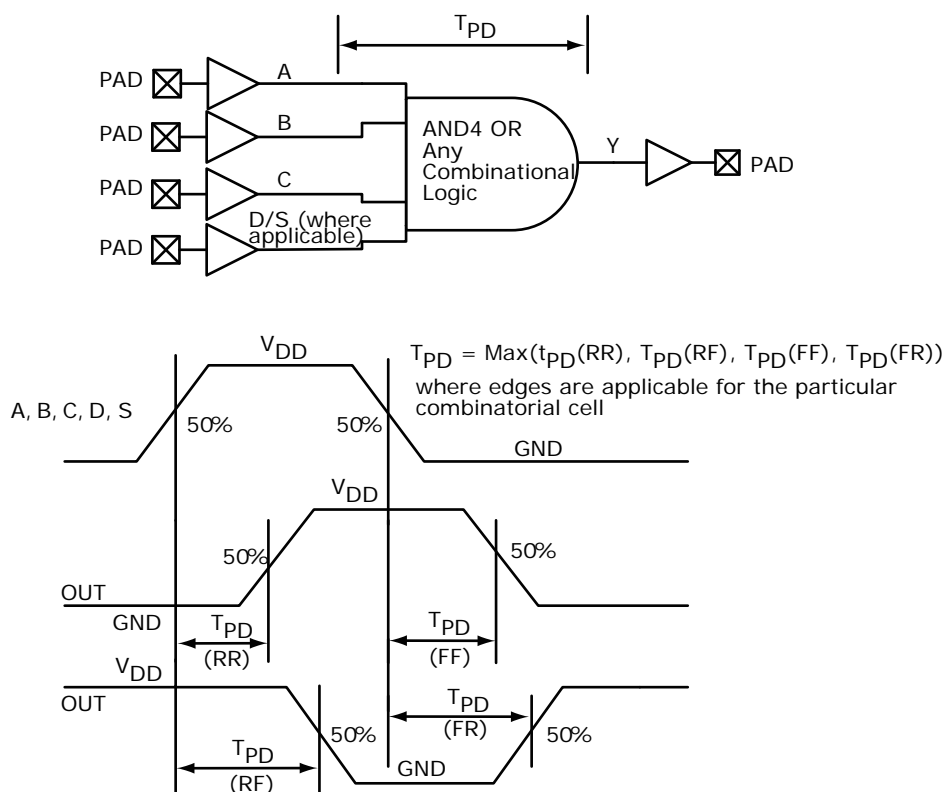
Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDROWAL}$	Asynchronous load minimum pulse width for output DDR	C, C	0.304	0.357	ns
$T_{DDROCKMPWH}$	Clock minimum pulse width high for the output DDR	E, E	0.075	0.088	ns
$T_{DDROCKMPWL}$	Clock minimum pulse width low for the output DDR	E, E	0.159	0.187	ns

## 2.3.10 Logic Element Specifications

### 2.3.10.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, see *SmartFusion2 and IGLOO2 Macro Library Guide*.

**Figure 14 • LUT-4**



**Table 233 • RAM1K18 – Dual-Port Mode for Depth x Width Configuration 4K x 4 (continued)**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register			0.323		0.38	ns
Read access time without pipeline register	$T_{CLK2Q}$		2.273		2.673	ns
Access time with feed-through write timing			1.511		1.778	ns
Address setup time	$T_{ADDRSU}$	0.543		0.638		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.334		0.393		ns
Data hold time	$T_{DHD}$	0.082		0.096		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns
Block select hold time	$T_{BLKHD}$	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		1.511		1.778	ns
Block select minimum pulse width	$T_{BLKMPW}$	0.186		0.219		ns
Read enable setup time	$T_{RDESU}$	0.516		0.607		ns
Read enable hold time	$T_{RDEHD}$	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	$T_{R2Q}$		1.507		1.773	ns
Asynchronous reset removal time	$T_{RSTREM}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTREC}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	$T_{RSTMPW}$	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTSU}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTHD}$	0.036		0.043		ns
Write enable setup time	$T_{WESU}$	0.458		0.539		ns
Write enable hold time	$T_{WEHD}$	0.048		0.057		ns
Maximum frequency	$F_{MAX}$		400		340	MHz

**Table 240 •  $\mu$ SRAM (RAM128x8) in 128 x 8 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.091		0.107		ns
Read address hold time in asynchronous mode		-0.778		-0.915		ns
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHD}$	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	$T_{RSTREM}$	-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	$T_{RSTREC}$	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	$T_{R2Q}$		0.835		0.982	ns
Read synchronous reset setup time	$T_{SRSTSU}$	0.271		0.319		ns
Read synchronous reset hold time	$T_{SRSTHD}$	0.061		0.071		ns
Write clock period	$T_{CCY}$	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	$T_{BLKCSU}$	0.404		0.476		ns
Write block hold time	$T_{BLKCHD}$	0.007		0.008		ns
Write input data setup time	$T_{DINCSU}$	0.115		0.135		ns
Write input data hold time	$T_{DINCHD}$	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.026		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

**Table 254 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only) (continued)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	Unit
	100 kHz	25 MHz	12.5 MHz	
150	161	161	161	Sec

**Table 255 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	Unit
	100 kHz	25 MHz	12.5 MHz	
005	47	27	28	Sec
010	77	35	35	Sec
025	150	42	41	Sec
050	33 <sup>1</sup>	Not Supported	Not Supported	Sec
060	291	83	82	Sec
090	427	109	108	Sec
150	708	157	160	Sec
005	41	48	49	Sec
010	86	87	87	Sec
025	87	85	86	Sec
050	85	Not Supported	Not Supported	Sec
060	78	86	86	Sec
090	154	162	162	Sec
150	161	161	161	Sec
005	87	67	66	Sec
010	161	113	113	Sec
025	229	120	121	Sec
050	112	Not Supported	Not Supported	Sec
060	368	161	158	Sec
090	582	261	260	Sec
150	867	309	310	Sec

1. Auto Programming in 050 device is done through SC\_SPI, and SPI CLK is set to 6.25 MHz.

The following table lists the programming times in worst-case conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ . External SPI flash part# AT25DF641-s3H is used during this measurement.

**Table 256 • JTAG Programming (Fabric Only)**

M2S/M2GL Device	Image size		Program	Verify	Unit
	Bytes				
005	302672		44	10	Sec
010	568784		50	18	Sec
025	1223504		73	26	Sec
050	2424832		88	54	Sec
060	2418896		99	54	Sec
090	3645968		135	126	Sec
150	6139184		177	193	Sec

**Table 257 • JTAG Programming (eNVM Only)**

M2S/M2GL Device	Image size		Program	Verify	Unit
	Bytes				
005	137536		61	4	Sec
010	274816		100	9	Sec
025	274816		100	9	Sec
050	2,78,528		106	8	Sec
060	268480		98	8	Sec
090	544496		176	15	Sec
150	544496		177	15	Sec

**Table 258 • JTAG Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size		Program	Verify	Unit
	Bytes				
005	439296		71	11	Sec
010	842688		129	20	Sec
025	1497408		142	35	Sec
050	2695168		184	59	Sec
060	2686464		180	70	Sec
090	4190208		288	147	Sec
150	6682768		338	231	Sec



## 2.3.17 Non-Deterministic Random Bit Generator (NRBG) Characteristics

For more information about NRBG, see *AC407: Using NRBG Services in SmartFusion2 and IGLOO2 Devices Application Note*. The following table lists the NRBG in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 275 • Non-Deterministic Random Bit Generator (NRBG)**

Service	Timing	Unit	Conditions	
			Prediction Resistance	Additional Input
Instantiate	85	ms	OFF	X
Generate (after Instantiate) <sup>1</sup>	4.5 ms + (6.25 us/byte x No. of Bytes)		OFF	0
	6.0 ms + (6.25 us/byte x No. of Bytes)		OFF	64
	7.0 ms + (6.25 us/byte x No. of Bytes)		OFF	128
Generate (after Instantiate)	47	ms	ON	X
Generate (subsequent) <sup>1</sup>	0.5 ms + (6.25 us/byte x No. of Bytes)		OFF	0
	2.0 ms + (6.25 us/byte x No. of Bytes)		OFF	64
	3.0 ms + (6.25 us/byte x No. of Bytes)		OFF	128
Generate (subsequent)	43	ms	ON	X
Reseed	40	ms		
Uninstantiate	0.16	ms		
Reset	0.10	ms		
Self test	20	ms	First time after power-up	
	6	ms	Subsequent	

1. If PUF\_OFF, generate will incur additional PUF delay time for consecutive service calls.

## 2.3.18 Cryptographic Block Characteristics

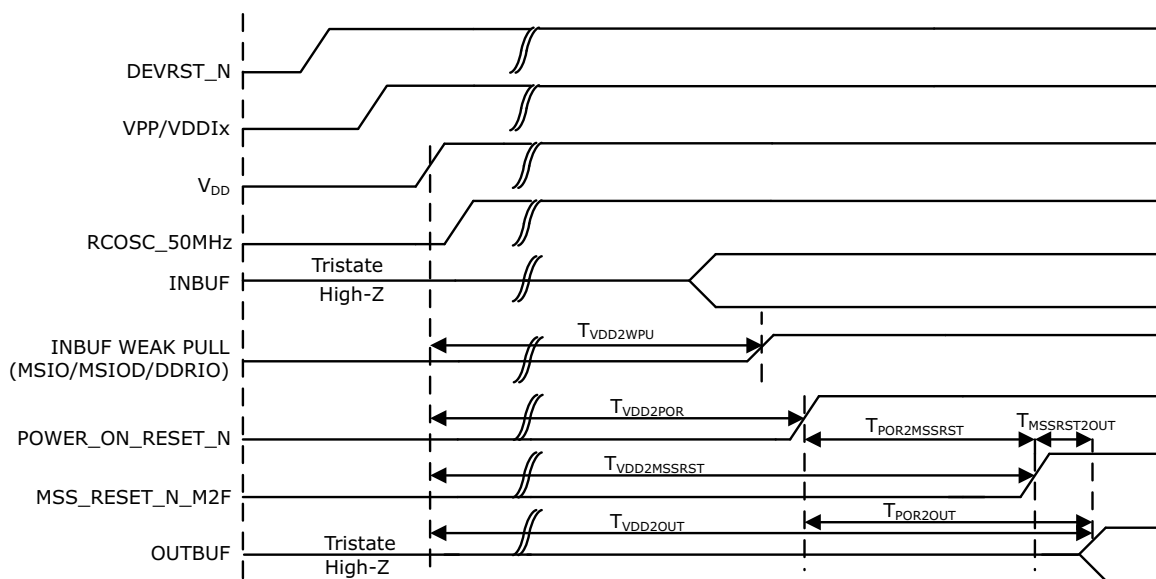
For more information about cryptographic block and associated services, see *AC410: Using AES System Services in SmartFusion2 and IGLOO2 Devices Application Note* and *AC432: Using SHA-256 System Services in SmartFusion2 and IGLOO2 Devices Application Note*.

The following table lists the cryptographic block characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 276 • Cryptographic Block Characteristics**

Service	Conditions	Timing	Unit
Any service	First certificate check penalty at boot	11.5	ms
AES128/256 (encoding / decoding) <sup>1</sup>	100 blocks up to 64k blocks	700	kbps

**Figure 17 • Power-up to Functional Timing Diagram for SmartFusion2**



The following table lists the IGLOO2 power-up to functional times in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 289 • Power-up to Functional Times for IGLOO2**

Symbol	From	To	Description	Maximum Power-up to Functional Time for IGLOO2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	114	114	113	114	114	114
$T_{VDD2OUT}$	$V_{DD}$	Output available at I/O	$V_{DD}$ at its minimum threshold level to output	2587	2600	2607	2558	2591	2600	2699
$T_{VDD2POR}$	$V_{DD}$	POWER_ON_RESET_N	$V_{DD}$ at its minimum threshold level to fabric	2474	2486	2493	2445	2477	2486	2585
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

**Note:** For more information about power-up times, see *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide*.

**Table 305 • SPI Characteristics for All Devices (continued)**

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%–90%) <sup>1</sup>		2.906		ns	IO Configuration: LVCMOS 2.5 V-8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0 1]_DI setup time <sup>2</sup>	12			ns	
sp9m	SPI_[0 1]_DI hold time <sup>2</sup>	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0 1]_DI setup time <sup>2</sup>	2			ns	
sp9s	SPI_[0 1]_DI hold time <sup>2</sup>	7			ns	
SPI master configuration (applicable for 060, 090, and 150 devices)						
sp6m	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 7.0			ns	
sp7m	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 9.5			ns	
sp8m	SPI_[0 1]_DI setup time <sup>2</sup>	15			ns	
sp9m	SPI_[0 1]_DI hold time <sup>2</sup>	–2.5			ns	
SPI slave configuration (applicable for 060, 090, and 150 devices)						
sp6s	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 16.0			ns	
sp7s	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 3.5			ns	
sp8s	SPI_[0 1]_DI setup time <sup>2</sup>	3			ns	
sp9s	SPI_[0 1]_DI hold time <sup>2</sup>	2.5			ns	

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. For allowable pclk configurations, see Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

## 2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 308 • MMUART Characteristics**

Parameter	Description	-1	-Std	Unit
FMMUART_REF_CLK	Internally sourced MMUART reference clock frequency.	166	142	MHz
BAUDMMUARTTx	Maximum transmit baud rate	10.375	8.875	Mbps
BAUDMMUARTRx	Maximum receive baud rate	10.375	8.875	Mbps

## 2.3.35 IGLOO2 Specifications

### 2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 309 • Maximum Frequency for HPMS Main Clock**

Symbol	Description	-1	-Std	Unit
HPMS_CLK	Maximum frequency for the HPMS main clock	166	142	MHz

### 2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI\_0\_CLK. For timing parameter definitions, see Figure 23, page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 310 • SPI Characteristics for All Devices**

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPIFMAX	Maximum operating frequency of SPI interface			20	MHz	
sp1	SPI_[0 1]_CLK minimum period					
	SPI_[0 1]_CLK = PCLK/2	12			ns	
	SPI_[0 1]_CLK = PCLK/4	24.1			ns	
	SPI_[0 1]_CLK = PCLK/8	48.2			ns	
	SPI_[0 1]_CLK = PCLK/16	0.1			$\mu\text{s}$	
	SPI_[0 1]_CLK = PCLK/32	0.19			$\mu\text{s}$	
	SPI_[0 1]_CLK = PCLK/64	0.39			$\mu\text{s}$	
SPI_[0 1]_CLK = PCLK/128	0.77			$\mu\text{s}$		

**Table 310 • SPI Characteristics for All Devices (continued)**

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp2	SPI_[0 1]_CLK minimum pulse width high					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			µs	
	SPI_[0 1]_CLK = PCLK/32	0.095			µs	
	SPI_[0 1]_CLK = PCLK/64	0.195			µs	
	SPI_[0 1]_CLK = PCLK/128	0.385			µs	
sp3	SPI_[0 1]_CLK minimum pulse width low					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			µs	
	SPI_[0 1]_CLK = PCLK/32	0.095			µs	
	SPI_[0 1]_CLK = PCLK/64	0.195			µs	
	SPI_[0 1]_CLK = PCLK/128	0.385			µs	
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) <sup>1</sup>		2.77		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%–90%) <sup>1</sup>		2.906		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0 1]_DI setup time <sup>2</sup>	12			ns	
sp9m	SPI_[0 1]_DI hold time <sup>2</sup>	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0 1]_DI setup time <sup>2</sup>	2			ns	
sp9s	SPI_[0 1]_DI hold time <sup>2</sup>	7			ns	