



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 50K Logic Modules
Operating Temperature	-40°C ~ 100°C (Tj)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s050ts-fg896i">https://www.e-xfl.com/product-detail/microchip-technology/m2s050ts-fg896i</a>



**Power Matters.™**

**Microsemi Corporate Headquarters**

One Enterprise, Aliso Viejo,  
CA 92656 USA

Within the USA: +1 (800) 713-4113

Outside the USA: +1 (949) 380-6100

Fax: +1 (949) 215-4996

Email: [sales.support@microsemi.com](mailto:sales.support@microsemi.com)

[www.microsemi.com](http://www.microsemi.com)

© 2016 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

**About Microsemi**

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at [www.microsemi.com](http://www.microsemi.com).

# Contents

---

<b>1</b>	<b>Revision History</b>	<b>1</b>
1.1	Revision 11.0	1
1.2	Revision 10.0	1
1.3	Revision 9.0	1
1.4	Revision 8.0	2
1.5	Revision 7.0	2
1.6	Revision 6.0	2
1.7	Revision 5.0	2
1.8	Revision 4.0	2
1.9	Revision 3.0	3
1.10	Revision 2.0	3
1.11	Revision 1.0	3
<b>2</b>	<b>IGLOO2 FPGA and SmartFusion2 SoC FPGA</b>	<b>4</b>
2.1	Device Status	4
2.2	References	5
2.3	Electrical Specifications	5
2.3.1	Operating Conditions	5
2.3.2	Power Consumption	12
2.3.3	Average Fabric Temperature and Voltage Derating Factors	14
2.3.4	Timing Model	15
2.3.5	User I/O Characteristics	17
2.3.6	Logic Element Specifications	75
2.3.7	Global Resource Characteristics	78
2.3.8	FPGA Fabric SRAM	79
2.3.9	Programming Times	94
2.3.10	Math Block Timing Characteristics	103
2.3.11	Embedded NVM (eNVM) Characteristics	104
2.3.12	SRAM PUF	105
2.3.13	Non-Deterministic Random Bit Generator (NRBG) Characteristics	106
2.3.14	Cryptographic Block Characteristics	106
2.3.15	Crystal Oscillator	107
2.3.16	On-Chip Oscillator	109
2.3.17	Clock Conditioning Circuits (CCC)	110
2.3.18	JTAG	112
2.3.19	System Controller SPI Characteristics	113
2.3.20	Power-up to Functional Times	114
2.3.21	DEVRST_N Characteristics	116
2.3.22	DEVRST_N to Functional Times	116
2.3.23	Flash*Freeze Timing Characteristics	119
2.3.24	DDR Memory Interface Characteristics	120
2.3.25	SFP Transceiver Characteristics	120
2.3.26	SerDes Electrical and Timing AC and DC Characteristics	121
2.3.27	SmartFusion2 Specifications	123
2.3.28	CAN Controller Characteristics	128
2.3.29	USB Characteristics	128
2.3.30	MMUART Characteristics	129
2.3.31	IGLOO2 Specifications	129

# Tables

Table 1	IGLOO2 and SmartFusion2 Design Security Densities	4
Table 2	IGLOO2 and SmartFusion2 Data Security Densities	4
Table 3	Absolute Maximum Ratings	5
Table 4	Recommended Operating Conditions	6
Table 5	FPGA Operating Limits	7
Table 6	Embedded Operating Flash Limits	8
Table 7	Device Storage Temperature and Retention	8
Table 8	High Temperature Data Retention (HTR) Lifetime	8
Table 9	Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices	10
Table 10	Quiescent Supply Current Characteristics	12
Table 11	SmartFusion2 and IGLOO2 Quiescent Supply Current ( $V_{DD} = 1.2\text{ V}$ ) – Typical Process	12
Table 12	Currents During Program Cycle, $0\text{ }^{\circ}\text{C} \leq T_J \leq 85\text{ }^{\circ}\text{C}$ – Typical Process	13
Table 13	Currents During Verify Cycle, $0\text{ }^{\circ}\text{C} \leq T_J \leq 85\text{ }^{\circ}\text{C}$ – Typical Process	13
Table 14	SmartFusion2 and IGLOO2 Quiescent Supply Current ( $V_{DD} = 1.26\text{ V}$ ) – Worst-Case Process	13
Table 15	Average Junction Temperature and Voltage Derating Factors for Fabric Timing Delays	14
Table 16	Inrush Currents at Power up, $-40\text{ }^{\circ}\text{C} \leq T_J \leq 100\text{ }^{\circ}\text{C}$ – Typical Process	14
Table 17	Timing Model Parameters	15
Table 18	Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions	19
Table 19	Maximum Data Rate Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions	20
Table 20	Maximum Data Rate Summary Table for Differential I/O in Worst-Case Industrial Conditions	20
Table 21	Maximum Frequency Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions	20
Table 22	Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions	21
Table 23	Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions	21
Table 24	Input Capacitance, Leakage Current, and Ramp Time	22
Table 25	I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank	22
Table 26	I/O Weak Pull-up/Pull-down Resistances for MSIO I/O Bank	23
Table 27	I/O Weak Pull-up/Pull-down Resistances for MSIOD I/O Bank	23
Table 28	Schmitt Trigger Input Hysteresis	23
Table 29	LVTTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)	24
Table 30	LVTTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)	24
Table 31	LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)	24
Table 32	LVTTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)	24
Table 33	LVTTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)	24
Table 34	LVTTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)	25
Table 35	LVTTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)	25
Table 36	LVTTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only)	25
Table 37	LVTTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank	25
Table 38	LVCMOS 2.5 V DC Recommended DC Operating Conditions	26
Table 39	LVCMOS 2.5 V DC Input Voltage Specification	26
Table 40	LVCMOS 2.5 V DC Output Voltage Specification	26
Table 41	LVCMOS 2.5 V AC Minimum and Maximum Switching Speed	26
Table 42	LVCMOS 2.5 V AC Calibrated Impedance Option	26
Table 43	LVCMOS 2.5 V Receiver Characteristics (Input Buffers)	27
Table 44	LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)	27
Table 45	LVCMOS 2.5 V AC Test Parameter Specifications	27
Table 46	LVCMOS 2.5 V Transmitter Drive Strength Specifications	27
Table 47	LVCMOS 2.5 V Transmitter Characteristics for MSIO Bank (Output and Tristate Buffers)	28
Table 48	LVCMOS 1.8 V DC Recommended Operating Conditions	29
Table 49	LVCMOS 1.8 V DC Input Voltage Specification	29
Table 50	LVCMOS 1.8 V DC Output Voltage Specification	29

# 1 Revision History

---

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- Updated [Table 24](#), page 22 with minimum and maximum values for input current low and high (SAR 73114 and 80314).
- Added [Non-Deterministic Random Bit Generator \(NRBG\) Characteristics](#), page 106 (SAR 73114 and 79517).
- Added 060 device in [Table 282](#), page 110 (SAR 79860).
- Added [DEVRST\\_N to Functional Times](#), page 116 (SAR 73114).
- Added [Cryptographic Block Characteristics](#), page 106 (SAR 73114 and 79516).
- Update [Table 296](#), page 121 with VTX-AMP details (SAR 81756).
- Update note in [Table 297](#), page 122 (SAR 74570 and 80677).
- Update [Table 298](#), page 122 with generic EPCS details (SAR 75307).
- Added [Table 308](#), page 129 (SAR 50424).

## 1.2 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- The Surge Current on VDD during DEVRST\_B Assertion and Surge Current on VDD during Digest Check using System Services tables were deleted and added reference to [AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note](#). (SAR 76865 and 76623).
- Added 060 device in [Table 4](#), page 6 (SAR 76383).
- Updated [Table 24](#), page 22 for ramp time input (SAR 72103).
- Added 060 device details in [Table 284](#), page 112 (SAR 74927).
- Updated [Table 290](#), page 116 for name change (SAR 74925).
- Updated [Table 283](#), page 111 for 060 FG676 Package details (SAR 78849).
- Updated [Table 305](#), page 126 for SmartFusion2 and [Table 310](#), page 129 for IGLOO2 for SPI timing and Fmax (SAR 56645, 75331).
- Updated [Table 293](#), page 119 for Flash\*Freeze entry and exit times (SAR 75329, 75330).
- Updated [Table 297](#), page 122 for RX-CID information (SAR 78271).
- Added [Table 8](#), page 8 and [Figure 1](#), page 9 (SAR 78932).
- Updated [Table 223](#), page 76 for timing characteristics and [Table 224](#), page 77 (SAR 75998).
- Added [SRAM PUF](#), page 105 (SAR 64406).
- Added a footnote on digest cycle in [Table 5](#), page 7 (SAR 79812).

## 1.3 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document.

- Added a note in [Table 5](#), page 7 (SAR 71506).
- Added a note in [Table 6](#), page 8 (SAR 74616).
- Added a note in [Figure 3](#), page 17 (SAR 71506).
- Updated Quiescent Supply Current for 060 in [Table 11](#), page 12 and [Table 12](#), page 13 (SAR 74483).
- Updated programming currents for 060 in [Table 13](#), page 13, [Table 14](#), page 13, and [Table 15](#), page 14.
- Added DEVRST\_B assertion tables (SAR 74708).
- Updated I/O speeds for LVDS 3.3 V in [Table 18](#), page 19 and [Table 21](#), page 20 (SAR 69829).
- Updated [Table 24](#), page 22 (SAR 69418).
- Updated [Table 25](#), page 22, [Table 26](#), page 23, [Table 27](#), page 23 (SAR 74570).
- Updated all AC/DC table to link to the [Input Capacitance, Leakage Current, and Ramp Time](#), page 22 for reference (SAR 69418).

**Table 48 • LVCMOS 2.5 V Transmitter Characteristics for MSIOD Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	2.206	2.596	2.678	3.15	2.64	3.106	4.935	5.805	4.74	5.576	ns
4 mA	Slow	1.835	2.159	2.242	2.637	2.256	2.654	5.413	6.368	5.15	6.059	ns
6 mA	Slow	1.709	2.01	2.132	2.508	2.167	2.549	5.813	6.838	5.499	6.469	ns
8 mA	Slow	1.63	1.918	1.958	2.303	2.012	2.367	6.226	7.324	5.816	6.842	ns
12 mA	Slow	1.648	1.939	1.86	2.187	1.921	2.259	6.519	7.669	6.027	7.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.8 1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 49 • LVCMOS 1.8 V DC Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
<b>LVCMOS 1.8 V DC Recommended Operating Conditions</b>					
Supply voltage	$V_{DDI}$	1.710	1.8	1.89	V

**Table 50 • LVCMOS 1.8 V DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	$V_{IH}$ (DC)	$0.65 \times V_{DDI}$	1.89	V
DC input logic high (for MSIO I/O bank)	$V_{IH}$ (DC)	$0.65 \times V_{DDI}$	3.45	V
DC input logic low	$V_{IL}$ (DC)	-0.3	$0.35 \times V_{DDI}$	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			-
Input current low <sup>1</sup>	$I_{IL}$ (DC)			-

1. See Table 24, page 22.

**Table 51 • LVCMOS 1.8 V DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	$V_{OH}$	$V_{DDI} - 0.45$		V
DC output logic low	$V_{OL}$		0.45	V

**Table 52 • LVCMOS 1.8 V Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank) <sup>1</sup>	$D_{MAX}$	400	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	295	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank) <sup>1</sup>	$D_{MAX}$	400	Mbps	AC loading: 17 pF load, maximum drive/slew

1. Maximum Data Rate applies for Drive Strength 8 mA and above, All Slews.

**Table 100 • HSTL AC Test Parameter Specification**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	0.75	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Reference resistance for data test path for HSTL15 Class I ( $T_{DP}$ )	$RTT\_TEST$	50	$\Omega$
Reference resistance for data test path for HSTL15 Class II ( $T_{DP}$ )	$RTT\_TEST$	25	$\Omega$
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**AC Switching Characteristics**

Worst-case commercial conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ , worst-case  $V_{DDI}$ .

**Table 101 • HSTL Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)**

		$T_{PY}$		
		-1	-Std	Unit
Pseudo differential	None	1.605	1.888	ns
	47.8	1.614	1.898	ns
True differential	None	1.622	1.909	ns
	47.8	1.628	1.916	ns

**Table 102 • HSTL Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
<b>HSTL Class I</b>											
Single-ended	2.6	3.059	2.514	2.958	2.514	2.958	2.431	2.86	2.431	2.86	ns
Differential	2.621	3.083	2.648	3.115	2.647	3.113	2.925	3.442	2.923	3.44	ns
<b>HSTL Class II</b>											
Single-ended	2.511	2.954	2.488	2.927	2.49	2.93	2.409	2.833	2.411	2.836	ns
Differential	2.528	2.974	2.552	3.003	2.551	3.001	2.897	3.409	2.896	3.408	ns

**2.3.6.2 Stub-Series Terminated Logic**

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

**Table 156 • LPDDR-LVCMOS 1.8 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	0.9	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**Table 157 • LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification for DDRIO Bank**

Output Drive Selection	$V_{OH}$ (V) Min	$V_{OL}$ (V) Max	$I_{OH}$ (at $V_{OH}$ ) mA	$I_{OL}$ (at $V_{OL}$ ) mA
2 mA	$V_{DDI} - 0.45$	0.45	2	2
4 mA	$V_{DDI} - 0.45$	0.45	4	4
6 mA	$V_{DDI} - 0.45$	0.45	6	6
8 mA	$V_{DDI} - 0.45$	0.45	8	8
10 mA	$V_{DDI} - 0.45$	0.45	10	10
12 mA	$V_{DDI} - 0.45$	0.45	12	12
16 mA <sup>1</sup>	$V_{DDI} - 0.45$	0.45	16	16

1. 16 mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance.

**Table 158 • LPDDR-LVCMOS 1.8V AC Switching Characteristics for Receiver (for DDRIO I/O Bank with Fixed Code - Input Buffers)**

ODT (On Die Termination)	-1	-Std	-1	-Std	Unit
None	1.968	2.315	2.099	2.47	ns

**Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	medium_fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4 mA	slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	medium_fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6 mA	slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	medium_fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns
8 mA	slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns



**Table 162 • LVDS DC Output Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	$V_{OH}$	1.25	1.425	1.6	V
DC output logic low	$V_{OL}$	0.9	1.075	1.25	V

**Table 163 • LVDS DC Differential Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
Differential output voltage swing	$V_{OD}$	250	350	450	mV
Output common mode voltage	$V_{OCM}$	1.125	1.25	1.375	V
Input common mode voltage	$V_{ICM}$	0.05	1.25	2.35	V
Input differential voltage	$V_{ID}$	100	350	600	mV

**Table 164 • LVDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	535	Mbps	AC loading: 12 pF / 100 $\Omega$ differential load
Maximum data rate (for MSIOD I/O bank) no pre-emphasis	$D_{MAX}$	620	Mbps	AC loading: 10 pF / 100 $\Omega$ differential load
		700	Mbps	AC loading: 2 pF / 100 $\Omega$ differential load

**Table 165 • LVDS AC Impedance Specifications**

Parameter	Symbol	Typ	Max	Unit
Termination resistance	$R_T$	100		$\Omega$

**Table 166 • LVDS AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	Cross point	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF

**LVDS25 AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

**Table 167 • LVDS25 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.774	3.263	ns
100	2.775	3.264	ns

### AC Switching Characteristics

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$ .

**Table 180 • B-LVDS AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.738	3.221	ns
100	2.735	3.218	ns

**Table 181 • B-LVDS AC Switching Characteristics for Receiver for MSIOD I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.495	2.934	ns
100	2.495	2.935	ns

**Table 182 • B-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.258	2.656	2.343	2.756	2.329	2.74	2.12	2.494	2.123	2.497	ns

#### 2.3.7.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

#### Minimum and Maximum Input and Output Levels

**Table 183 • M-LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage <sup>1</sup>	$V_{DDI}$	2.375	2.5	2.625	V

1. Only M-LVDS TYPE I is supported.

**Table 184 • M-LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	$V_I$	0	2.925	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>2</sup>	$I_{IL}$ (DC)			

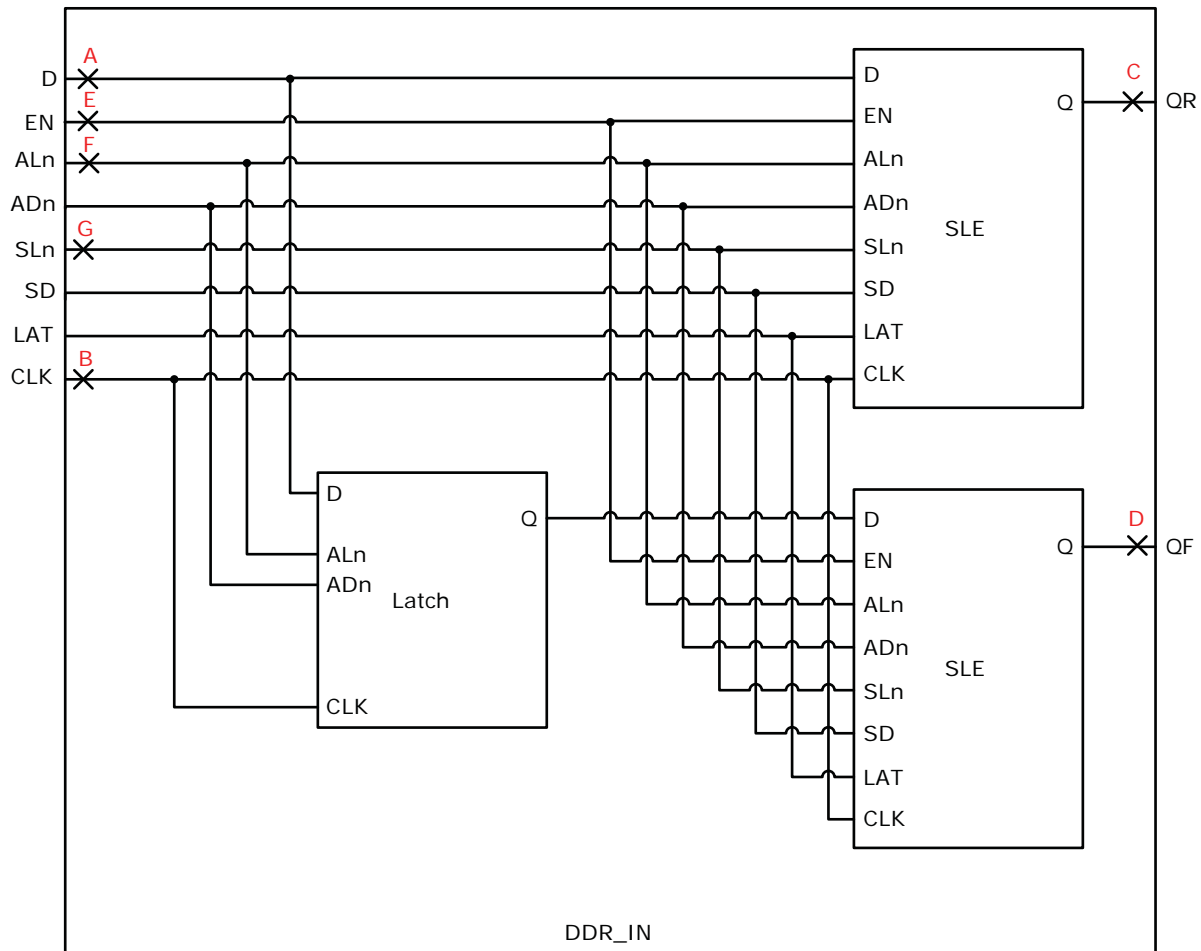
1. See Table 24, page 22.

### 2.3.9 DDR Module Specification

This section describes input and output DDR module and timing specifications.

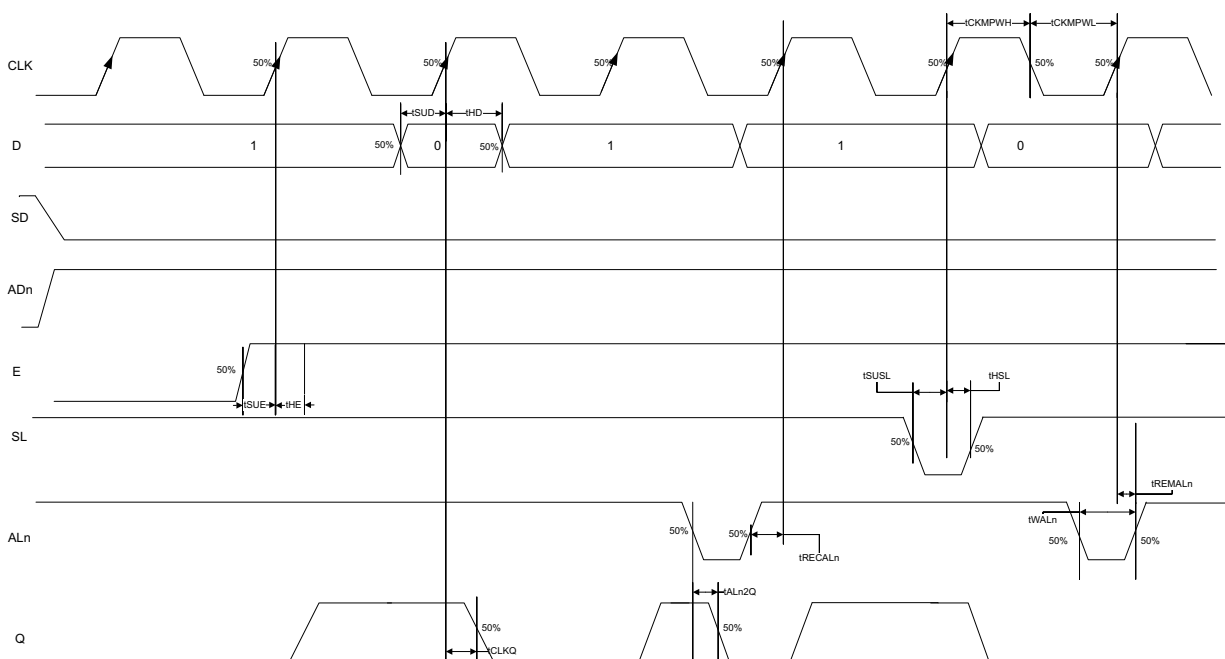
#### 2.3.9.1 Input DDR Module

Figure 10 • Input DDR Module



The following figure shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

**Figure 16 • Sequential Module Timing Diagram**



### 2.3.10.3.1 Timing Characteristics

The following table lists the register delays in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 224 • Register Delays**

Parameter	Symbol	-1	-Std	Unit
Clock-to-Q of the core register	$T_{CLKQ}$	0.108	0.127	ns
Data setup time for the core register	$T_{SUD}$	0.254	0.298	ns
Data hold time for the core register	$T_{HD}$	0	0	ns
Enable setup time for the core register	$T_{SUE}$	0.335	0.394	ns
Enable hold time for the core register	$T_{HE}$	0	0	ns
Synchronous load setup time for the core register	$T_{SUSL}$	0.335	0.394	ns
Synchronous load hold time for the core register	$T_{HSL}$	0	0	ns
Asynchronous Clear-to-Q of the core register (ADn = 1)	$T_{ALn2Q}$	0.473	0.556	ns
Asynchronous preset-to-Q of the core register (ADn = 0)		0.451	0.531	ns
Asynchronous load removal time for the core register	$T_{REMAln}$	0	0	ns
Asynchronous load recovery time for the core register	$T_{RECALn}$	0.353	0.415	ns
Asynchronous load minimum pulse width for the core register	$T_{WALn}$	0.266	0.313	ns
Clock minimum pulse width high for the core register	$T_{CKMPWH}$	0.065	0.077	ns
Clock minimum pulse width low for the core register	$T_{CKMPWL}$	0.139	0.164	ns

**Table 232 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 (continued)**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Address setup time	$T_{ADDRSU}$	0.475		0.559		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.336		0.395		ns
Data hold time	$T_{DHD}$	0.082		0.096		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns
Block select hold time	$T_{BLKHD}$	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		1.529		1.799	ns
Block select minimum pulse width	$T_{BLKMPW}$	0.186		0.219		ns
Read enable setup time	$T_{RDESU}$	0.485		0.57		ns
Read enable hold time	$T_{RDEHD}$	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	$T_{R2Q}$		1.514		1.781	ns
Asynchronous reset removal time	$T_{RSTREM}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTREC}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	$T_{RSTMPW}$	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTSU}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTHD}$	0.036		0.043		ns
Write enable setup time	$T_{WESU}$	0.415		0.488		ns
Write enable hold time	$T_{WEHD}$	0.048		0.057		ns
Maximum frequency	$F_{MAX}$		400		340	MHz

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 233 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	$T_{CY}$	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	$T_{PLCY}$	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns

**Table 242 •  $\mu$ SRAM (RAM512x2) in 512 x 2 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Write clock period	$T_{CCY}$	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	$T_{BLKCSU}$	0.404		0.476		ns
Write block hold time	$T_{BLKCHD}$	0.007		0.008		ns
Write input data setup time	$T_{DINCSU}$	0.101		0.118		ns
Write input data hold time	$T_{DINCHD}$	0.137		0.161		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.247		0.29		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.03		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

The following table lists the  $\mu$ SRAM in 1024 x 1 mode in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 243 •  $\mu$ SRAM (RAM1024x1) in 1024 x 1 Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	$T_{CY}$	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	$T_{PLCY}$	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	$T_{CLK2Q}$		0.27		0.31	ns
Read access time without pipeline register				1.78		2.1
Read address setup time in synchronous mode	$T_{ADDRSU}$	0.301		0.354		ns
Read address setup time in asynchronous mode			1.978		2.327	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.137		0.161		ns
Read address hold time in asynchronous mode			-0.6		-0.71	
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHHD}$	-0.65		-0.77		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.16		2.54	ns
Read asynchronous reset removal time (pipelined clock)	$T_{RSTREM}$	-0.02		-0.03		ns
Read asynchronous reset removal time (non-pipelined clock)			0.046		0.054	

**Table 251 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only) (continued)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
150	544496	10	158	15	Sec

**Table 252 • SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	9	61	11	Sec
010	842688	15	107	21	Sec
025	1497408	26	121	35	Sec
050	2695168	43	141	55	Sec
060	2686464	48	143	60	Sec
090	4190208	75	244	91	Sec
150	6682768	117	296	141	Sec

**Table 253 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	Unit
	100 kHz	25 MHz	12.5 MHz	
005	47	27	28	Sec
010	77	35	35	Sec
025	150	42	41	Sec
050	33 <sup>1</sup>	Not Supported	Not Supported	Sec
060	291	83	82	Sec
090	427	109	108	Sec
150	708	157	160	Sec

1. Auto Programming in 050 device is done through SC\_SPI, and SPI CLK is set to 6.25 MHz.

**Table 254 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	Unit
	100 kHz	25 MHz	12.5 MHz	
005	41	48	49	Sec
010	86	87	87	Sec
025	87	85	86	Sec
050	85	Not Supported	Not Supported	Sec
060	78	86	86	Sec
090	154	162	162	Sec

**Table 262 • SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

<b>M2S/M2GL Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	302672	6	41	8	Sec
010	568784	10	48	14	Sec
025	1223504	21	61	29	Sec
050	2424832	39	82	50	Sec
060	2418896	44	87	54	Sec
090	3645968	66	112	79	Sec
150	6139184	108	162	128	Sec

**Table 263 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

<b>M2S/M2GL Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	137536	3	64	4	Sec
010	274816	4	104	7	Sec
025	274816	4	104	8	Sec
050	2,78,528	4	102	8	Sec
060	268480	6	102	8	Sec
090	544496	10	179	15	Sec
150	544496	10	180	15	Sec

**Table 264 • SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

<b>M2S/M2GL Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	439296	9	83	11	Sec
010	842688	15	129	21	Sec
025	1497408	26	143	35	Sec
050	2695168	43	163	55	Sec
060	2686464	48	165	60	Sec
090	4190208	75	266	91	Sec
150	6682768	117	318	141	Sec



1. The minimum output clock frequency is limited by the PLL. For more information, see [UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide](#).
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance is limited by the CCC output frequency.

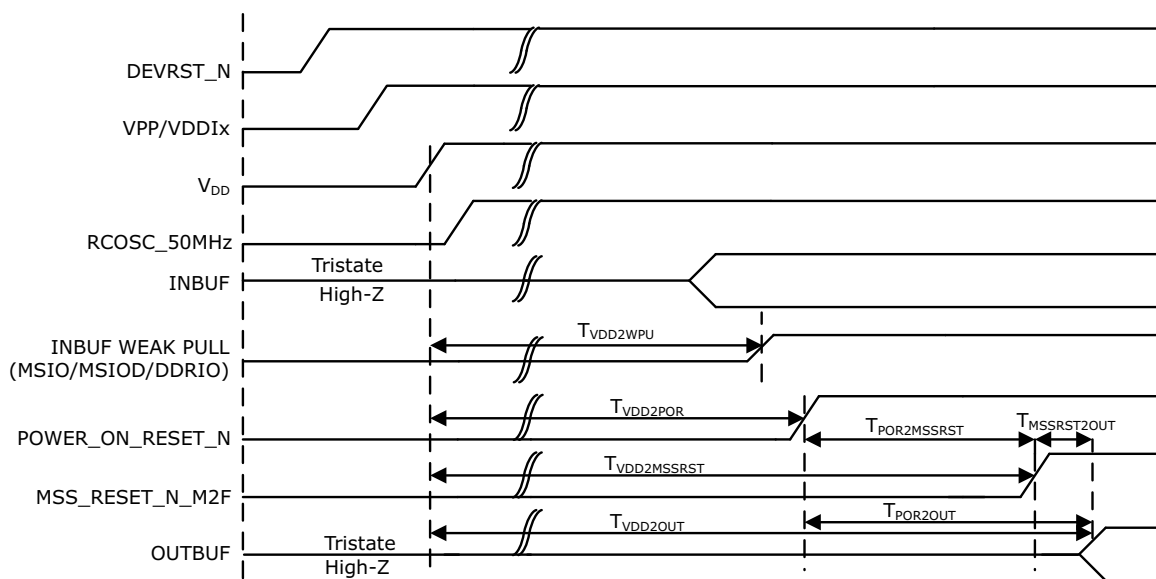
The following table lists the CCC/PLL jitter specifications in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 283 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications**

CCC Output Maximum Peak-to-Peak Period Jitter $F_{OUT\_CCC}$						
Parameter	Conditions/Package Combinations				Unit	
<b>10 FG484, 050 FG896/FG484/FCS325 Packages<sup>1</sup></b>	SSO = 0	$0 < SSO \leq 2$	$SSO \leq 4$	$SSO \leq 8$	$SSO \leq 16$	
20 MHz to 100 MHz	$\text{Max}(110, \pm 1\% \times (1/F_{OUT\_CCC}))$	$\text{Max}(150, \pm 1\% \times (1/F_{OUT\_CCC}))$				ps
100 MHz to 400 MHz	$\text{Max}(120, \pm 1\% \times (1/F_{OUT\_CCC}))$	$\text{Max}(150, \pm 1\% \times (1/F_{OUT\_CCC}))$		$\text{Max}(170, \pm 1\% \times (1/F_{OUT\_CCC}))$		ps
<b>025 FG484/FCS325 Package<sup>1</sup></b>	$0 < SSO \leq 16$					
20 MHz to 74 MHz	$\pm 1\% \times (1/F_{OUT\_CCC})$					ps
74 MHz to 400 MHz	210					ps
<b>005 FG484 Package<sup>1</sup></b>	$0 < SSO \leq 16$					
20 MHz to 53 MHz	$\pm 1\% \times (1/F_{OUT\_CCC})$					ps
53 MHz to 400 MHz	270					ps
<b>090 FG676 and FC325 Package<sup>1</sup></b>	$0 < SSO \leq 16$					
20 MHz to 100 MHz	$\pm 1\% \times (1/F_{OUT\_CCC})$					ps
100 MHz to 400 MHz	150					ps
<b>060 FG676 Package<sup>1</sup></b>	$0 < SSO \leq 16$					
20 MHz to 100 MHz	$\pm 1\% \times (1/F_{OUT\_CCC})$					ps
100 MHz to 400 MHz	150					ps
<b>150 FC1152 Package<sup>1</sup></b>	$0 < SSO \leq 16$					
20 MHz to 100 MHz	$\pm 1\% \times (1/F_{OUT\_CCC})$					ps
100 MHz to 400 MHz	120					ps

1. SSO data is based on LVCMOS 2.5 V MSIO and/or MSIOD bank I/Os.

**Figure 17 • Power-up to Functional Timing Diagram for SmartFusion2**



The following table lists the IGLOO2 power-up to functional times in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 289 • Power-up to Functional Times for IGLOO2**

Symbol	From	To	Description	Maximum Power-up to Functional Time for IGLOO2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	114	114	113	114	114	114
$T_{VDD2OUT}$	$V_{DD}$	Output available at I/O	$V_{DD}$ at its minimum threshold level to output	2587	2600	2607	2558	2591	2600	2699
$T_{VDD2POR}$	$V_{DD}$	POWER_ON_RESET_N	$V_{DD}$ at its minimum threshold level to fabric	2474	2486	2493	2445	2477	2486	2585
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

**Note:** For more information about power-up times, see [UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide](#).

The following table lists the IGLOO2 DEVRST\_N to functional times in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 292 • DEVRST\_N to Functional Times for IGLOO2**

Symbol	From	To	Description	Maximum Power-up to Functional Time for IGLOO2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	116	113	113	115	115	114
$T_{DEVRST2OUT}$	DEVRST_N	Output available at I/O	$V_{DD}$ at its minimum threshold level to output	314	353	314	307	343	341	341
$T_{DEVRST2POR}$	DEVRST_N	POWER_ON_RESET_N	$V_{DD}$ at its minimum threshold level to fabric	200	238	201	195	230	229	227
$T_{DEVRST2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215

**Table 310 • SPI Characteristics for All Devices (continued)**

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp2	SPI_[0 1]_CLK minimum pulse width high					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			µs	
	SPI_[0 1]_CLK = PCLK/32	0.095			µs	
	SPI_[0 1]_CLK = PCLK/64	0.195			µs	
	SPI_[0 1]_CLK = PCLK/128	0.385			µs	
sp3	SPI_[0 1]_CLK minimum pulse width low					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			µs	
	SPI_[0 1]_CLK = PCLK/32	0.095			µs	
	SPI_[0 1]_CLK = PCLK/64	0.195			µs	
	SPI_[0 1]_CLK = PCLK/128	0.385			µs	
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) <sup>1</sup>		2.77		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%–90%) <sup>1</sup>		2.906		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0 1]_DI setup time <sup>2</sup>	12			ns	
sp9m	SPI_[0 1]_DI hold time <sup>2</sup>	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0 1]_DI setup time <sup>2</sup>	2			ns	
sp9s	SPI_[0 1]_DI hold time <sup>2</sup>	7			ns	

**Table 310 • SPI Characteristics for All Devices (continued)**

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPI master configuration (applicable for 060, 090, and 150 devices)						
sp6m	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 7.0			ns	
sp7m	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 9.5			ns	
sp8m	SPI_[0 1]_DI setup time <sup>2</sup>	15			ns	
sp9m	SPI_[0 1]_DI hold time <sup>2</sup>	–2.5			ns	
SPI slave configuration (applicable for 060, 090, and 150 devices)						
sp6s	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 16.0			ns	
sp7s	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 3.5			ns	
sp8s	SPI_[0 1]_DI setup time <sup>2</sup>	3			ns	
sp9s	SPI_[0 1]_DI hold time <sup>2</sup>	2.5			ns	

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. For allowable pclk configurations, see the Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

**Figure 23 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**

