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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 60K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s060-fgg484">https://www.e-xfl.com/product-detail/microchip-technology/m2s060-fgg484</a>

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## 2.3.16 SRAM PUF

For more details on static random-access memory (SRAM) physical unclonable functions (PUF) services, see AC434: Using SRAM PUF System Services in SmartFusion2 Application Note

The following table lists the SRAM PUF in worst-case industrial conditions,  $T_{jw} = 100^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 274 SRAM PUF

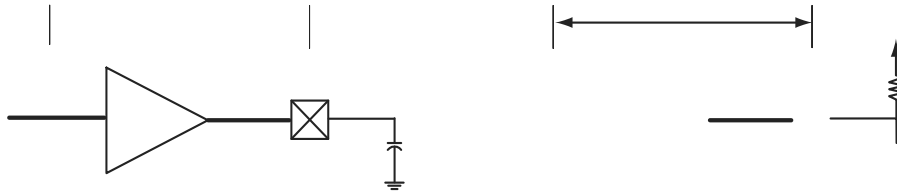
Service	PUF Off		PUF On		Unit
	Typ	Max	Typ	Max	
Create activation code	709.1	746.4	754.4	762.5	ms
Delete activation code	1329.3	1399.3	1414.1	1429.3	ms
Create intrinsic keycode	656.6	691.1	698.5	706.0	ms
Create extrinsic keycode	656.6	691.1	698.5	706.0	ms
Get number of keys	1.3	1.4	1.4	1.4	ms
Export (Kc0, Kc1)	998.0	1050.5	1061.7	1073.1	ms
Export 2 keycodes	2020.2	2126.5	2149.2	2172.3	ms
Export 4 keycodes	3065.7	3227.0	3261.3	3296.4	ms
Export 8 keycodes	5101.0	5369.5	5426.6	5485.0	ms
Export 16 keycodes	9212.1	9697.0	9800.1	9905.5	ms
Import (Kc0, Kc1)	39.7	41.8	42.2	42.7	ms
Import 2 keycodes	50.1	52.7	53.3	53.9	ms
Import 4 keycodes	60.1	63.8	64.5	65.2	ms
Import 8 keycodes	80.1	85.1	86.1	87.0	ms
Import 16 keycodes	123.8	130.4	131.7	133.2	ms
Delete keycode	552.5	581.6	587.8	594.1	ms
Fetch key	31.4	33.0	33.4	33.7	ms
Fetch ecc key	20.0	21.1	21.3	21.5	ms
Get seed	2.0	2.1	2.2	2.2	ms



### 2.3.5.2 Output Buffer and AC Loading

The following figure shows the output buffer and AC loading.

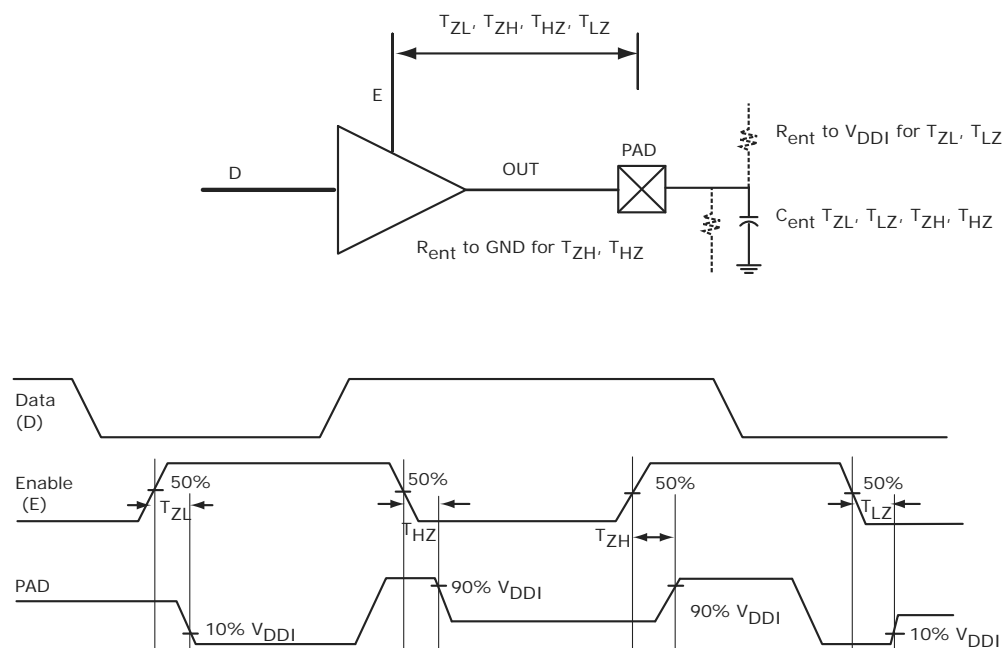
Figure 4 • Output Buffer AC Loading



### 2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

**Figure 5 • Tristate Buffer for Enable Path Test Point**



### 2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

**Table 18 • Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	630			Mbps
LVTTL 3.3 V	600			Mbps
LVC MOS 3.3 V	600			Mbps
LVC MOS 2.5 V	410	420	400	Mbps
LVC MOS 1.8 V	295	400	400	Mbps
LVC MOS 1.5 V	160	220	235	Mbps
LVC MOS 1.2 V	120	160	200	Mbps
LPDDR-LVC MOS 1.8 V mode			400	Mbps







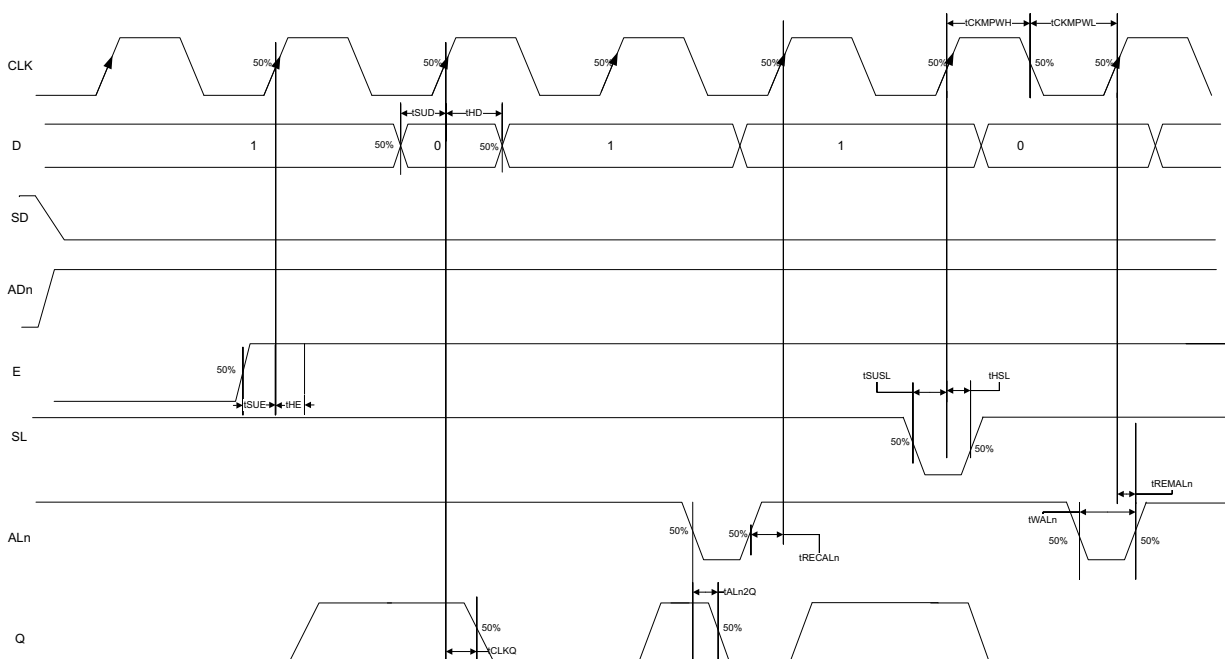






The following figure shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

**Figure 16 • Sequential Module Timing Diagram**



### 2.3.10.3.1 Timing Characteristics

The following table lists the register delays in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 224 • Register Delays**

Parameter	Symbol	-1	-Std	Unit
Clock-to-Q of the core register	$T_{CLKQ}$	0.108	0.127	ns
Data setup time for the core register	$T_{SUD}$	0.254	0.298	ns
Data hold time for the core register	$T_{HD}$	0	0	ns
Enable setup time for the core register	$T_{SUE}$	0.335	0.394	ns
Enable hold time for the core register	$T_{HE}$	0	0	ns
Synchronous load setup time for the core register	$T_{SUSL}$	0.335	0.394	ns
Synchronous load hold time for the core register	$T_{HSL}$	0	0	ns
Asynchronous Clear-to-Q of the core register (ADn = 1)	$T_{ALN2Q}$	0.473	0.556	ns
Asynchronous preset-to-Q of the core register (ADn = 0)		0.451	0.531	ns
Asynchronous load removal time for the core register	$T_{REMALN}$	0	0	ns
Asynchronous load recovery time for the core register	$T_{RECALN}$	0.353	0.415	ns
Asynchronous load minimum pulse width for the core register	$T_{WALN}$	0.266	0.313	ns
Clock minimum pulse width high for the core register	$T_{CKMPWH}$	0.065	0.077	ns
Clock minimum pulse width low for the core register	$T_{CKMPWL}$	0.139	0.164	ns

## 2.3.11 Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for the positions of various global routing resources.

The following table lists the 150 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 225 • 150 Device Global Resource**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	$T_{RCKL}$	0.83	0.911	0.831	0.913	ns
Input high delay for global clock	$T_{RCKH}$	1.457	1.588	1.715	1.869	ns
Maximum skew for global clock	$T_{RCKSW}$		0.131		0.154	ns

The following table lists the 090 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 226 • 090 Device Global Resource**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	$T_{RCKL}$	0.835	0.888	0.833	0.886	ns
Input high delay for global clock	$T_{RCKH}$	1.405	1.489	1.654	1.752	ns
Maximum skew for global clock	$T_{RCKSW}$		0.084		0.098	ns

The following table lists the 050 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 227 • 050 Device Global Resource**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	$T_{RCKL}$	0.827	0.897	0.826	0.896	ns
Input high delay for global clock	$T_{RCKH}$	1.419	1.53	1.671	1.8	ns
Maximum skew for global clock	$T_{RCKSW}$		0.111		0.129	ns

The following table lists the 025 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 228 • 025 Device Global Resource**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	$T_{RCKL}$	0.747	0.799	0.745	0.797	ns
Input high delay for global clock	$T_{RCKH}$	1.294	1.378	1.522	1.621	ns
Maximum skew for global clock	$T_{RCKSW}$		0.084		0.099	ns

**Table 232 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 (continued)**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Address setup time	$T_{ADDRSU}$	0.475		0.559		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.336		0.395		ns
Data hold time	$T_{DHD}$	0.082		0.096		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns
Block select hold time	$T_{BLKHD}$	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		1.529		1.799	ns
Block select minimum pulse width	$T_{BLKMPW}$	0.186		0.219		ns
Read enable setup time	$T_{RDESU}$	0.485		0.57		ns
Read enable hold time	$T_{RDEHD}$	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	$T_{R2Q}$		1.514		1.781	ns
Asynchronous reset removal time	$T_{RSTREM}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTREC}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	$T_{RSTMPW}$	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTSU}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTHD}$	0.036		0.043		ns
Write enable setup time	$T_{WESU}$	0.415		0.488		ns
Write enable hold time	$T_{WEHD}$	0.048		0.057		ns
Maximum frequency	$F_{MAX}$		400		340	MHz

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 233 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	$T_{CY}$	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	$T_{PLCY}$	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns

**Table 233 • RAM1K18 – Dual-Port Mode for Depth x Width Configuration 4K x 4 (continued)**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register			0.323		0.38	ns
Read access time without pipeline register	$T_{CLK2Q}$		2.273		2.673	ns
Access time with feed-through write timing			1.511		1.778	ns
Address setup time	$T_{ADDRSU}$	0.543		0.638		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.334		0.393		ns
Data hold time	$T_{DHD}$	0.082		0.096		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns
Block select hold time	$T_{BLKHD}$	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		1.511		1.778	ns
Block select minimum pulse width	$T_{BLKMPW}$	0.186		0.219		ns
Read enable setup time	$T_{RDESU}$	0.516		0.607		ns
Read enable hold time	$T_{RDEHD}$	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	$T_{R2Q}$		1.507		1.773	ns
Asynchronous reset removal time	$T_{RSTREM}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTREC}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	$T_{RSTMPW}$	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTSU}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTHD}$	0.036		0.043		ns
Write enable setup time	$T_{WESU}$	0.458		0.539		ns
Write enable hold time	$T_{WEHD}$	0.048		0.057		ns
Maximum frequency	$F_{MAX}$		400		340	MHz

**Table 240 •  $\mu$ SRAM (RAM128x8) in 128 x 8 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.091		0.107		ns
Read address hold time in asynchronous mode		-0.778		-0.915		ns
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHD}$	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	$T_{RSTREM}$	-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	$T_{RSTREC}$	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	$T_{R2Q}$		0.835		0.982	ns
Read synchronous reset setup time	$T_{SRSTSU}$	0.271		0.319		ns
Read synchronous reset hold time	$T_{SRSTHD}$	0.061		0.071		ns
Write clock period	$T_{CCY}$	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	$T_{BLKCSU}$	0.404		0.476		ns
Write block hold time	$T_{BLKCHD}$	0.007		0.008		ns
Write input data setup time	$T_{DINCSU}$	0.115		0.135		ns
Write input data hold time	$T_{DINCHD}$	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.026		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz



**Table 262 • SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

<b>M2S/M2GL Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	302672	6	41	8	Sec
010	568784	10	48	14	Sec
025	1223504	21	61	29	Sec
050	2424832	39	82	50	Sec
060	2418896	44	87	54	Sec
090	3645968	66	112	79	Sec
150	6139184	108	162	128	Sec

**Table 263 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

<b>M2S/M2GL Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	137536	3	64	4	Sec
010	274816	4	104	7	Sec
025	274816	4	104	8	Sec
050	2,78,528	4	102	8	Sec
060	268480	6	102	8	Sec
090	544496	10	179	15	Sec
150	544496	10	180	15	Sec

**Table 264 • SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

<b>M2S/M2GL Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	439296	9	83	11	Sec
010	842688	15	129	21	Sec
025	1497408	26	143	35	Sec
050	2695168	43	163	55	Sec
060	2686464	48	165	60	Sec
090	4190208	75	266	91	Sec
150	6682768	117	318	141	Sec

## 2.3.14 Math Block Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC math block supports 18×18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently. The following table lists the math blocks with all registers used in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 268 • Math Blocks with all Registers Used**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input, control register setup time	$T_{MISU}$	0.149		0.176		ns
Input, control register hold time	$T_{MIHD}$	1.68		1.976		ns
CDIN input setup time	$T_{MOCDINSU}$	0.185		0.218		ns
CDIN input hold time	$T_{MOCDINHHD}$	0.08		0.094		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	-0.419		-0.493		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	0.011		0.013		ns
Asynchronous reset removal time	$T_{MARSTREM}$	0		0		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.088		0.104		ns
Output register clock to out delay	$T_{MOCQ}$		0.232		0.273	ns
CLK minimum period	$T_{MCLKMP}$	2.245		2.641		ns

The following table lists the math blocks with input bypassed and output registers used in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 269 • Math Block with Input Bypassed and Output Registers Used**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Output register setup time	$T_{MOSU}$	2.294		2.699		ns
Output register hold time	$T_{MOHD}$	1.68		1.976		ns
CDIN input setup time	$T_{MOCDINSU}$	0.115		0.136		ns
CDIN input hold time	$T_{MOCDINHHD}$	-0.444		-0.522		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	-0.419		-0.493		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	0.011		0.013		ns
Asynchronous reset removal time	$T_{MARSTREM}$	0		0		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.014		0.017		ns
Output register clock to out delay	$T_{MOCQ}$		0.232		0.273	ns
CLK minimum period	$T_{MCLKMP}$	2.179		2.563		ns

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 270 • Math Block with Input Register Used and Output in Bypass Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input register setup time	$T_{MISU}$	0.149		0.176		ns
Input register hold time	$T_{MIHD}$	0.185		0.218		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	0.08		0.094		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	-0.012		-0.014		ns
Asynchronous reset removal time	$T_{MARSTREM}$	-0.005		-0.005		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.088		0.104		ns
Input register clock to output delay	$T_{MICQ}$		2.52		2.964	ns
CDIN to output delay	$T_{MCDIN2Q}$		1.951		2.295	ns

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 271 • Math Block with Input and Output in Bypass Mode**

Parameter	Symbol	-1	-Std	Unit
		Max	Max	
Input to output delay	$T_{MIQ}$	2.568	3.022	ns
CDIN to output delay	$T_{MCDIN2Q}$	1.951	2.295	ns

### 2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when  $V_{DD} = 1.14\text{ V}$ ,  $V_{PPNVM} = V_{PP} = 2.375\text{ V}$ .

**Table 272 • eNVM Read Performance**

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
$T_J$	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$F_{MAXREAD}$	eNVM maximum read frequency	25	25	25	25	25	25	MHz

The following table lists the eNVM page programming in worst-case conditions when  $V_{DD} = 1.14\text{ V}$ ,  $V_{PPNVM} = V_{PP} = 2.375\text{ V}$ .

**Table 273 • eNVM Page Programming**

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
$T_J$	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$T_{PAGEPGM}$	eNVM page programming time	40	40	40	40	40	40	ms



### 2.3.31.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI\_x\_CLK. For timing parameter definitions, see Figure 22, page 128.

The following table lists the SPI characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$

**Table 305 • SPI Characteristics for All Devices**

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPIFMAX	Maximum operating frequency of SPI interface			20	MHz	
sp1	SPI_[0 1]_CLK minimum period					
	SPI_[0 1]_CLK = PCLK/2	12			ns	
	SPI_[0 1]_CLK = PCLK/4	24.1			ns	
	SPI_[0 1]_CLK = PCLK/8	48.2			ns	
	SPI_[0 1]_CLK = PCLK/16	0.1			$\mu\text{s}$	
	SPI_[0 1]_CLK = PCLK/32	0.19			$\mu\text{s}$	
	SPI_[0 1]_CLK = PCLK/64	0.39			$\mu\text{s}$	
sp2	SPI_[0 1]_CLK minimum pulse width high					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			$\mu\text{s}$	
	SPI_[0 1]_CLK = PCLK/32	0.095			$\mu\text{s}$	
	SPI_[0 1]_CLK = PCLK/64	0.195			$\mu\text{s}$	
sp3	SPI_[0 1]_CLK minimum pulse width low					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			$\mu\text{s}$	
	SPI_[0 1]_CLK = PCLK/32	0.095			$\mu\text{s}$	
	SPI_[0 1]_CLK = PCLK/64	0.195			$\mu\text{s}$	
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) <sup>1</sup>		2.77		ns	I/O Configuration: LVCMOS 2.5 V– 8 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C