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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

|                         |   |
|-------------------------|---|
| Product Status          | Active  |
| Architecture            | MCU, FPGA   |
| Core Processor          | ARM® Cortex®-M3   |
| Flash Size              | 256KB   |
| RAM Size                | 64KB  |
| Peripherals             | DDR, PCIe, SERDES   |
| Connectivity            | CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB  |
| Speed                   | 166MHz  |
| Primary Attributes      | FPGA - 60K Logic Modules  |
| Operating Temperature   | 0°C ~ 85°C (TJ)   |
| Package / Case          | 676-BGA   |
| Supplier Device Package | 676-FBGA (27x27)  |
| Purchase URL            | <a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s060-fgg676">https://www.e-xfl.com/product-detail/microchip-technology/m2s060-fgg676</a> |



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where

- $\theta_{JA}$  = Junction-to-air thermal resistance
- $\theta_{JB}$  = Junction-to-board thermal resistance
- $\theta_{JC}$  = Junction-to-case thermal resistance
- $T_J$  = Junction temperature
- $T_A$  = Ambient temperature
- $T_B$  = Board temperature (measured 1.0 mm away from the package edge)
- $T_C$  = Case temperature
- $P$  = Total power dissipated by the device

**Table 9 • Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices**

| Device     | Still Air     | 1.0 m/s | 2.5 m/s | $\theta_{JB}$ | $\theta_{JC}$ | Unit |
|------------|---------------|---------|---------|---------------|---------------|------|
|            | $\theta_{JA}$ |         |         |               |               |      |
| <b>005</b> |               |         |         |               |               |      |
| FG484      | 19.36         | 15.81   | 14.63   | 9.74          | 5.27          | °C/W |
| VF256      | 41.30         | 38.16   | 35.30   | 28.41         | 3.94          | °C/W |
| VF400      | 20.19         | 16.94   | 15.41   | 8.86          | 4.95          | °C/W |
| TQ144      | 42.80         | 36.80   | 34.50   | 37.20         | 10.80         | °C/W |
| <b>010</b> |               |         |         |               |               |      |
| FG484      | 18.22         | 14.83   | 13.62   | 8.83          | 4.92          | °C/W |
| VF256      | 37.36         | 34.26   | 31.45   | 24.84         | 7.89          | °C/W |
| VF400      | 19.40         | 15.75   | 14.22   | 8.11          | 4.22          | °C/W |
| TQ144      | 38.60         | 32.60   | 30.30   | 31.80         | 8.60          | °C/W |
| <b>025</b> |               |         |         |               |               |      |
| FG484      | 17.03         | 13.66   | 12.45   | 7.66          | 4.18          | °C/W |
| VF256      | 33.85         | 30.59   | 27.85   | 21.63         | 6.13          | °C/W |
| VF400      | 18.36         | 14.89   | 13.36   | 7.12          | 3.41          | °C/W |
| FCS325     | 29.17         | 24.87   | 23.12   | 14.44         | 2.31          | °C/W |
| <b>050</b> |               |         |         |               |               |      |
| FG484      | 15.29         | 12.19   | 10.99   | 6.27          | 3.24          | °C/W |
| FG896      | 14.70         | 12.50   | 10.90   | 7.20          | 4.90          | °C/W |
| VF400      | 17.53         | 14.17   | 12.63   | 6.32          | 2.81          | °C/W |
| FCS325     | 27.38         | 23.18   | 21.41   | 12.47         | 1.59          | °C/W |
| <b>060</b> |               |         |         |               |               |      |
| FG484      | 15.40         | 12.06   | 10.85   | 6.14          | 3.15          | °C/W |
| FG676      | 15.49         | 12.21   | 11.06   | 7.07          | 3.87          | °C/W |
| VF400      | 17.45         | 14.01   | 12.47   | 6.22          | 2.69          | °C/W |
| FCS325     | 27.03         | 22.91   | 21.25   | 12.33         | 1.54          | °C/W |
| <b>090</b> |               |         |         |               |               |      |
| FG484      | 14.64         | 11.37   | 10.16   | 5.43          | 2.77          | °C/W |
| FG676      | 14.52         | 11.19   | 10.37   | 6.17          | 3.24          | °C/W |
| FCS325     | 26.63         | 22.26   | 20.13   | 14.24         | 2.50          | °C/W |

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIO I/O bank at  $V_{OH}/V_{OL}$  Level.

**Table 26 • I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank**

| $V_{DDI}$ Domain      | R(WEAK PULL-UP) at $V_{OH}$ ( $\Omega$ ) |       | R(WEAK PULL-DOWN) at $V_{OL}$ ( $\Omega$ ) |       |
|-----------------------|--|-------|--|-------|
|                       | Min                                      | Max   | Min  | Max   |
| 3.3 V                 | 9.9K                                     | 17.1K | 9.98K                                      | 17.5K |
| 2.5 V <sup>1, 2</sup> | 10K                                      | 17.6K | 10.1K                                      | 18.4K |
| 1.8 V <sup>1, 2</sup> | 10.4K                                    | 19.1K | 10.4K                                      | 20.4K |
| 1.5 V <sup>1, 2</sup> | 10.7K                                    | 20.4K | 10.8K                                      | 22.2K |
| 1.2 V <sup>1, 2</sup> | 11.3K                                    | 23.2K | 11.5K                                      | 26.7K |

1.  $R(\text{WEAK PULL-DOWN}) = (V_{OL\text{spec}})/I(\text{WEAK PULL-DOWN MAX})$ .
2.  $R(\text{WEAK PULL-UP}) = (V_{DDI\text{max}} - V_{OH\text{spec}})/I(\text{WEAK PULL-UP MIN})$ .

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIOD I/O bank at  $V_{OH}/V_{OL}$  Level.

**Table 27 • I/O Weak Pull-up/Pull-down Resistances for MSIOD I/O Bank**

| $V_{DDI}$ Domain      | R(WEAK PULL-UP) at $V_{OH}$ ( $\Omega$ ) |       | R(WEAK PULL-DOWN) at $V_{OL}$ ( $\Omega$ ) |       |
|-----------------------|--|-------|--|-------|
|                       | Min                                      | Max   | Min  | Max   |
| 2.5 V <sup>1, 2</sup> | 9.6K                                     | 16.6K | 9.5K                                       | 16.4K |
| 1.8 V <sup>1, 2</sup> | 9.7K                                     | 17.3K | 9.7K                                       | 17.1K |
| 1.5 V <sup>1, 2</sup> | 9.9K                                     | 18K   | 9.8K                                       | 17.6K |
| 1.2 V <sup>1, 2</sup> | 10.3K                                    | 19.6K | 10K  | 19.1K |

1.  $R(\text{WEAK PULL-DOWN}) = (V_{OL\text{spec}})/I(\text{WEAK PULL-DOWN MAX})$ .
2.  $R(\text{WEAK PULL-UP}) = (V_{DDI\text{max}} - V_{OH\text{spec}})/I(\text{WEAK PULL-UP MIN})$ .

The following table lists the hysteresis voltage value for schmitt trigger mode input buffers.

**Table 28 • Schmitt Trigger Input Hysteresis**

| Input Buffer Configuration        | Hysteresis Value (Typical, unless otherwise noted) |
|-----------------------------------|--|
| 3.3 V LVTTTL/LVCMOS/<br>PCI/PCI-X | $0.05 \times V_{DDI}$ (worst-case)                 |
| 2.5 V LVCMOS                      | $0.05 \times V_{DDI}$ (worst-case)                 |
| 1.8 V LVCMOS                      | $0.1 \times V_{DDI}$ (worst-case)                  |
| 1.5 V LVCMOS                      | 60 mV  |
| 1.2 V LVCMOS                      | 20 mV  |

**Table 72 • LVCMOS 1.5 V Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ |       | $T_{ZL}$ |       | $T_{ZH}$ |       | $T_{HZ}^1$ |       | $T_{LZ}^1$ |       | Unit |
|------------------------|--------------|----------|-------|----------|-------|----------|-------|------------|-------|------------|-------|------|
|                        |              | -1       | -Std  | -1       | -Std  | -1       | -Std  | -1         | -Std  | -1         | -Std  |      |
| 2 mA                   | Slow         | 2.735    | 3.218 | 3.371    | 3.966 | 3.618    | 4.257 | 6.03       | 7.095 | 5.705      | 6.712 | ns   |
| 4 mA                   | Slow         | 2.426    | 2.854 | 2.992    | 3.521 | 3.221    | 3.79  | 6.738      | 7.927 | 6.298      | 7.41  | ns   |
| 6 mA                   | Slow         | 2.433    | 2.862 | 2.81     | 3.306 | 3.031    | 3.566 | 7.123      | 8.38  | 6.596      | 7.76  | ns   |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.10 1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-12A.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 73 • LVCMOS 1.2 V DC Recommended DC Operating Conditions**

| Parameter      | Symbol    | Min   | Typ | Max  | Unit |
|----------------|-----------|-------|-----|------|------|
| Supply voltage | $V_{DDI}$ | 1.140 | 1.2 | 1.26 | V    |

**Table 74 • LVCMOS 1.2 V DC Input Voltage Specification**

| Parameter   | Symbol        | Min                   | Max                   | Unit |
|---|---------------|-----------------------|-----------------------|------|
| DC input logic high (for MSIOD and DDRIO I/O banks) | $V_{IH} (DC)$ | $0.65 \times V_{DDI}$ | 1.26                  | V    |
| DC input logic high (for MSIO I/O bank)             | $V_{IH} (DC)$ | $0.65 \times V_{DDI}$ | 3.45                  | V    |
| DC input logic low                                  | $V_{IL} (DC)$ | -0.3                  | $0.35 \times V_{DDI}$ | V    |
| Input current high <sup>1</sup>                     | $I_{IH} (DC)$ |                       |                       |      |
| Input current low <sup>1</sup>                      | $I_{IL} (DC)$ |                       |                       |      |

1. See [Table 24](#), page 22.

**Table 75 • LVCMOS 1.2 V DC Output Voltage Specification**

| Parameter            | Symbol   | Min                   | Max                   | Unit |
|----------------------|----------|-----------------------|-----------------------|------|
| DC output logic high | $V_{OH}$ | $V_{DDI} \times 0.75$ |                       | V    |
| DC output logic low  | $V_{OL}$ |                       | $V_{DDI} \times 0.25$ | V    |

**Table 76 • LVCMOS 1.2 V Minimum and Maximum AC Switching Speed**

| Parameter                              | Symbol    | Max | Unit | Conditions                                 |
|--|-----------|-----|------|--|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 200 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank)  | $D_{MAX}$ | 120 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 160 | Mbps | AC loading: 17 pF load, maximum drive/slew |

### 2.3.6.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 103 • DDR1/SSTL2 DC Recommended Operating Conditions**

| Parameter               | Symbol    | Min   | Typ   | Max   | Unit |
|-------------------------|-----------|-------|-------|-------|------|
| Supply voltage          | $V_{DDI}$ | 2.375 | 2.5   | 2.625 | V    |
| Termination voltage     | $V_{TT}$  | 1.164 | 1.250 | 1.339 | V    |
| Input reference voltage | $V_{REF}$ | 1.164 | 1.250 | 1.339 | V    |

**Table 104 • DDR1/SSTL2 DC Input Voltage Specification**

| Parameter                       | Symbol        | Min              | Max              | Unit |
|---------------------------------|---------------|------------------|------------------|------|
| DC input logic high             | $V_{IH}$ (DC) | $V_{REF} + 0.15$ | 2.625            | V    |
| DC input logic low              | $V_{IL}$ (DC) | -0.3             | $V_{REF} - 0.15$ | V    |
| Input current high <sup>1</sup> | $I_{IH}$ (DC) |                  |                  |      |
| Input current low <sup>1</sup>  | $I_{IL}$ (DC) |                  |                  |      |

1. See Table 24, page 22.

**Table 105 • DDR1/SSTL2 DC Output Voltage Specification**

| Parameter   | Symbol               | Min              | Max              | Unit |
|---|----------------------|------------------|------------------|------|
| <b>SSTL2 Class I (DDR Reduced Drive)</b>  |                      |                  |                  |      |
| DC output logic high  | $V_{OH}$             | $V_{TT} + 0.608$ |                  | V    |
| DC output logic low   | $V_{OL}$             |                  | $V_{TT} - 0.608$ | V    |
| Output minimum source DC current  | $I_{OH}$ at $V_{OH}$ | 8.1              |                  | mA   |
| Output minimum sink current   | $I_{OL}$ at $V_{OL}$ | -8.1             |                  | mA   |
| <b>SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Bank Only</b> |                      |                  |                  |      |
| DC output logic high  | $V_{OH}$             | $V_{TT} + 0.81$  |                  | V    |
| DC output logic low   | $V_{OL}$             |                  | $V_{TT} - 0.81$  | V    |
| Output minimum source DC current  | $I_{OH}$ at $V_{OH}$ | 16.2             |                  | mA   |
| Output minimum sink current   | $I_{OL}$ at $V_{OL}$ | -16.2            |                  | mA   |

**Table 106 • DDR1/SSTL2 DC Differential Voltage Specification**

| Parameter                     | Symbol        | Min | Unit |
|-------------------------------|---------------|-----|------|
| DC input differential voltage | $V_{ID}$ (DC) | 0.3 | V    |



**Table 122 • SSTL18 DC Differential Voltage Specification**

| Parameter                     | Symbol        | Min | Unit |
|-------------------------------|---------------|-----|------|
| DC input differential voltage | $V_{ID}$ (DC) | 0.3 | V    |

**Table 123 • SSTL18 AC Differential Voltage Specifications (Applicable to DDRIO Bank Only)**

| Parameter                           | Symbol          | Min                          | Max                          | Unit |
|-------------------------------------|-----------------|------------------------------|------------------------------|------|
| AC input differential voltage       | $V_{DIFF}$ (AC) | 0.5                          |                              | V    |
| AC differential cross point voltage | $V_x$ (AC)      | $0.5 \times V_{DDI} - 0.175$ | $0.5 \times V_{DDI} + 0.175$ | V    |

**Table 124 • SSTL18 Minimum and Maximum AC Switching Speed (Applicable to DDRIO Bank Only)**

| Parameter                              | Symbol    | Max | Unit | Conditions                          |
|--|-----------|-----|------|-------------------------------------|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 667 | Mbps | AC loading: per JEDEC specification |

**Table 125 • SSTL18 AC Impedance Specifications (Applicable to DDRIO Bank Only)**

| Parameter   | Symbol    | Typ         | Unit     | Conditions                        |
|---|-----------|-------------|----------|-----------------------------------|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | $R_{REF}$ | 20, 42      | $\Omega$ | Reference resistor = 150 $\Omega$ |
| Effective impedance value (ODT)                                   | $R_{TT}$  | 50, 75, 150 | $\Omega$ | Reference resistor = 150 $\Omega$ |

**Table 126 • SSTL18 AC Test Parameter Specifications (Applicable to DDRIO Bank Only)**

| Parameter  | Symbol         | Typ | Unit     |
|--|----------------|-----|----------|
| Measuring/trip point for data path   | $V_{TRIP}$     | 0.9 | V        |
| Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )         | $R_{ENT}$      | 2K  | $\Omega$ |
| Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ ) | $C_{ENT}$      | 5   | pF       |
| Reference resistance for data test path for SSTL18 Class I ( $T_{DTP}$ )         | $R_{TT\_TEST}$ | 50  | $\Omega$ |
| Reference resistance for data test path for SSTL18 Class II ( $T_{DTP}$ )        | $R_{TT\_TEST}$ | 25  | $\Omega$ |
| Capacitive loading for data path ( $T_{DTP}$ )                                   | $C_{LOAD}$     | 5   | pF       |

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 1.71\text{ V}$

**Table 127 • DDR2/SSTL18 Receiver Characteristics for DDRIO I/O Bank with Fixed Code**

|                     | On-Die Termination (ODT) | $T_{PY}$ |       | Unit |
|---------------------|--------------------------|----------|-------|------|
|                     |                          | -1       | -Std  |      |
| Pseudo differential | None                     | 1.567    | 1.844 | ns   |
| True differential   | None                     | 1.588    | 1.869 | ns   |

**Table 144 • LPDDR AC Differential Voltage Specifications (for DDRIO I/O Bank Only)**

| Parameter                           | Symbol     | Min                  | Max                  | Unit |
|-------------------------------------|------------|----------------------|----------------------|------|
| AC input differential voltage       | $V_{DIFF}$ | $0.6 \times V_{DDI}$ |                      | V    |
| AC differential cross point voltage | $V_x$      | $0.4 \times V_{DDI}$ | $0.6 \times V_{DDI}$ | V    |

**Table 145 • LPDDR AC Specifications (for DDRIO I/O Bank Only)**

| Parameter         | Symbol    | Max | Unit | Conditions                           |
|-------------------|-----------|-----|------|--------------------------------------|
| Maximum data rate | $D_{MAX}$ | 400 | Mbps | AC loading: per JEDEC specifications |

**Table 146 • LPDDR AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

| Parameter                                    | Symbol    | Typ         | Unit     | Conditions                        |
|--|-----------|-------------|----------|-----------------------------------|
| Supported output driver calibrated impedance | $R_{REF}$ | 20, 42      | $\Omega$ | Reference resistor = 150 $\Omega$ |
| Effective impedance value (ODT)              | $R_{TT}$  | 50, 70, 150 | $\Omega$ | Reference resistor = 150 $\Omega$ |

**Table 147 • LPDDR AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

| Parameter  | Symbol         | Typ | Unit     |
|--|----------------|-----|----------|
| Measuring/trip point for data path   | $V_{TRIP}$     | 0.9 | V        |
| Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )         | $R_{ENT}$      | 2K  | $\Omega$ |
| Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ ) | $C_{ENT}$      | 5   | pF       |
| Reference resistance for data test path for LPDDR ( $T_{DP}$ )                   | $R_{TT\_TEST}$ | 50  | $\Omega$ |
| Capacitive loading for data path ( $T_{DP}$ )                                    | $C_{LOAD}$     | 5   | $\Omega$ |

**AC Switching Characteristics**

Worst-case commercial conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ , worst-case  $V_{DDI}$ .

**Table 148 • LPDDR Receiver Characteristics for DDRIO I/O Bank with Fixed Codes**

|                     | On-Die Termination (ODT) | $T_{PY}$ |       | Unit |
|---------------------|--------------------------|----------|-------|------|
|                     |                          | -1       | -Std  |      |
| Pseudo differential | None                     | 1.568    | 1.845 | ns   |
| True differential   | None                     | 1.588    | 1.869 | ns   |

**Table 149 • LPDDR Reduced Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

|              | $T_{DP}$ |       | $T_{ENZL}$ |       | $T_{ENZH}$ |       | $T_{ENHZ}$ |       | $T_{ENLZ}$ |       | Unit |
|--------------|----------|-------|------------|-------|------------|-------|------------|-------|------------|-------|------|
|              | -1       | -Std  | -1         | -Std  | -1         | -Std  | -1         | -Std  | -1         | -Std  |      |
| Single-ended | 2.383    | 2.804 | 2.23       | 2.623 | 2.229      | 2.622 | 2.202      | 2.591 | 2.201      | 2.59  | ns   |
| Differential | 2.396    | 2.819 | 2.764      | 3.252 | 2.764      | 3.252 | 2.255      | 2.653 | 2.255      | 2.653 | ns   |

**Table 162 • LVDS DC Output Voltage Specification**

| Parameter            | Symbol   | Min  | Typ   | Max  | Unit |
|----------------------|----------|------|-------|------|------|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6  | V    |
| DC output logic low  | $V_{OL}$ | 0.9  | 1.075 | 1.25 | V    |

**Table 163 • LVDS DC Differential Voltage Specification**

| Parameter                         | Symbol    | Min   | Typ  | Max   | Unit |
|-----------------------------------|-----------|-------|------|-------|------|
| Differential output voltage swing | $V_{OD}$  | 250   | 350  | 450   | mV   |
| Output common mode voltage        | $V_{OCM}$ | 1.125 | 1.25 | 1.375 | V    |
| Input common mode voltage         | $V_{ICM}$ | 0.05  | 1.25 | 2.35  | V    |
| Input differential voltage        | $V_{ID}$  | 100   | 350  | 600   | mV   |

**Table 164 • LVDS Minimum and Maximum AC Switching Speed**

| Parameter  | Symbol    | Max | Unit | Conditions   |
|--|-----------|-----|------|--|
| Maximum data rate (for MSIO I/O bank)                  | $D_{MAX}$ | 535 | Mbps | AC loading: 12 pF / 100 $\Omega$ differential load |
| Maximum data rate (for MSIOD I/O bank) no pre-emphasis | $D_{MAX}$ | 620 | Mbps | AC loading: 10 pF / 100 $\Omega$ differential load |
|  |           | 700 | Mbps | AC loading: 2 pF / 100 $\Omega$ differential load  |

**Table 165 • LVDS AC Impedance Specifications**

| Parameter              | Symbol | Typ | Max | Unit     |
|------------------------|--------|-----|-----|----------|
| Termination resistance | $R_T$  | 100 |     | $\Omega$ |

**Table 166 • LVDS AC Test Parameter Specifications**

| Parameter  | Symbol     | Typ         | Unit     |
|--|------------|-------------|----------|
| Measuring/trip point for data path   | $V_{TRIP}$ | Cross point | V        |
| Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )         | $R_{ENT}$  | 2K          | $\Omega$ |
| Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ ) | $C_{ENT}$  | 5           | pF       |

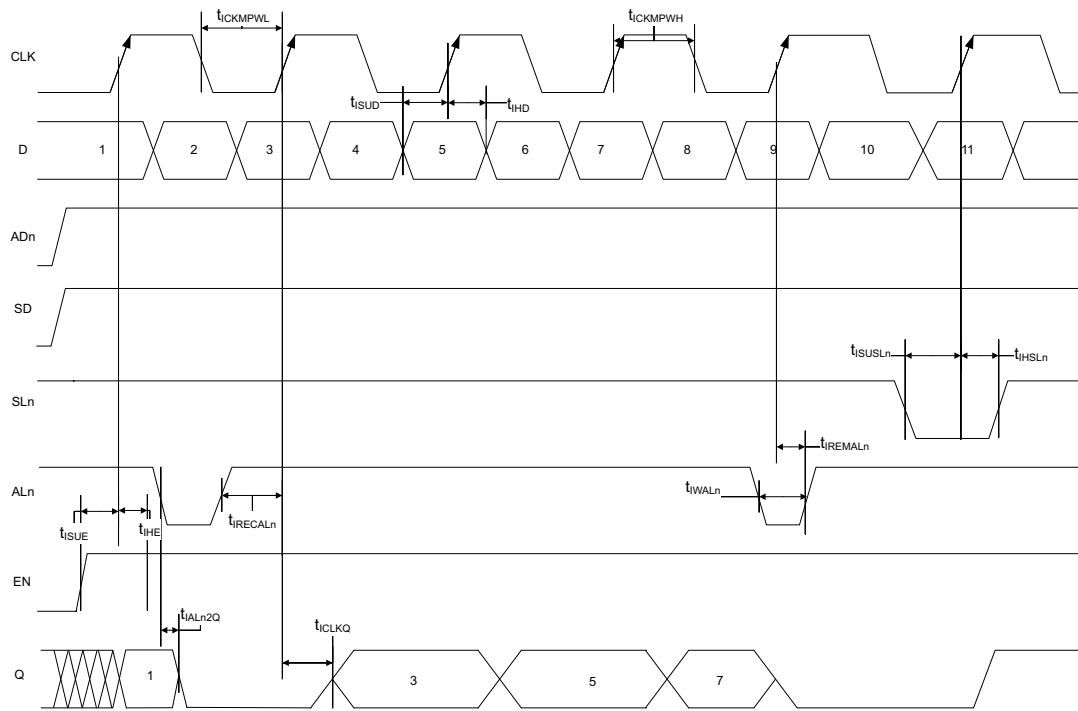
**LVDS25 AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

**Table 167 • LVDS25 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

| On-Die Termination (ODT) | $T_{PY}$ |       | Unit |
|--------------------------|----------|-------|------|
|                          | -1       | -Std  |      |
| None                     | 2.774    | 3.263 | ns   |
| 100                      | 2.775    | 3.264 | ns   |

**Figure 7 • I/O Register Input Timing Diagram**



## 2.3.11 Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. See [UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide](#) for the positions of various global routing resources.

The following table lists the 150 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 225 • 150 Device Global Resource**

| Parameter                         | Symbol      | -1    |       | -Std  |       | Unit |
|-----------------------------------|-------------|-------|-------|-------|-------|------|
|                                   |             | Min   | Max   | Min   | Max   |      |
| Input low delay for global clock  | $T_{RCKL}$  | 0.83  | 0.911 | 0.831 | 0.913 | ns   |
| Input high delay for global clock | $T_{RCKH}$  | 1.457 | 1.588 | 1.715 | 1.869 | ns   |
| Maximum skew for global clock     | $T_{RCKSW}$ |       | 0.131 |       | 0.154 | ns   |

The following table lists the 090 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 226 • 090 Device Global Resource**

| Parameter                         | Symbol      | -1    |       | -Std  |       | Unit |
|-----------------------------------|-------------|-------|-------|-------|-------|------|
|                                   |             | Min   | Max   | Min   | Max   |      |
| Input low delay for global clock  | $T_{RCKL}$  | 0.835 | 0.888 | 0.833 | 0.886 | ns   |
| Input high delay for global clock | $T_{RCKH}$  | 1.405 | 1.489 | 1.654 | 1.752 | ns   |
| Maximum skew for global clock     | $T_{RCKSW}$ |       | 0.084 |       | 0.098 | ns   |

The following table lists the 050 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 227 • 050 Device Global Resource**

| Parameter                         | Symbol      | -1    |       | -Std  |       | Unit |
|-----------------------------------|-------------|-------|-------|-------|-------|------|
|                                   |             | Min   | Max   | Min   | Max   |      |
| Input low delay for global clock  | $T_{RCKL}$  | 0.827 | 0.897 | 0.826 | 0.896 | ns   |
| Input high delay for global clock | $T_{RCKH}$  | 1.419 | 1.53  | 1.671 | 1.8   | ns   |
| Maximum skew for global clock     | $T_{RCKSW}$ |       | 0.111 |       | 0.129 | ns   |

The following table lists the 025 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 228 • 025 Device Global Resource**

| Parameter                         | Symbol      | -1    |       | -Std  |       | Unit |
|-----------------------------------|-------------|-------|-------|-------|-------|------|
|                                   |             | Min   | Max   | Min   | Max   |      |
| Input low delay for global clock  | $T_{RCKL}$  | 0.747 | 0.799 | 0.745 | 0.797 | ns   |
| Input high delay for global clock | $T_{RCKH}$  | 1.294 | 1.378 | 1.522 | 1.621 | ns   |
| Maximum skew for global clock     | $T_{RCKSW}$ |       | 0.084 |       | 0.099 | ns   |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 16K × 1 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 235 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1**

| Parameter  | Symbol          | –1     |       | –Std   |       | Unit |
|--|-----------------|--------|-------|--------|-------|------|
|  |                 | Min    | Max   | Min    | Max   |      |
| Clock period   | $T_{CY}$        | 2.5    |       | 2.941  |       | ns   |
| Clock minimum pulse width high   | $T_{CLKMPWH}$   | 1.125  |       | 1.323  |       | ns   |
| Clock minimum pulse width low  | $T_{CLKMPWL}$   | 1.125  |       | 1.323  |       | ns   |
| Pipelined clock period   | $T_{PLCY}$      | 2.5    |       | 2.941  |       | ns   |
| Pipelined clock minimum pulse width high                               | $T_{PLCLKMPWH}$ | 1.125  |       | 1.323  |       | ns   |
| Pipelined clock minimum pulse width low                                | $T_{PLCLKMPWL}$ | 1.125  |       | 1.323  |       | ns   |
| Read access time with pipeline register                                |                 |        | 0.32  |        | 0.377 | ns   |
| Read access time without pipeline register                             | $T_{CLK2Q}$     |        | 2.269 |        | 2.669 | ns   |
| Access time with feed-through write timing                             |                 |        | 1.51  |        | 1.777 | ns   |
| Address setup time   | $T_{ADDRSU}$    | 0.626  |       | 0.737  |       | ns   |
| Address hold time  | $T_{ADDRHD}$    | 0.274  |       | 0.322  |       | ns   |
| Data setup time  | $T_{DSU}$       | 0.322  |       | 0.378  |       | ns   |
| Data hold time   | $T_{DHD}$       | 0.082  |       | 0.096  |       | ns   |
| Block select setup time  | $T_{BLKSU}$     | 0.207  |       | 0.244  |       | ns   |
| Block select hold time   | $T_{BLKHD}$     | 0.216  |       | 0.254  |       | ns   |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$     |        | 1.51  |        | 1.777 | ns   |
| Block select minimum pulse width                                       | $T_{BLKMPW}$    | 0.186  |       | 0.219  |       | ns   |
| Read enable setup time   | $T_{RDESU}$     | 0.53   |       | 0.624  |       | ns   |
| Read enable hold time  | $T_{RDEHD}$     | 0.071  |       | 0.083  |       | ns   |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)                | $T_{RDPLESU}$   | 0.248  |       | 0.291  |       | ns   |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)                 | $T_{RDPLEHD}$   | 0.102  |       | 0.12   |       | ns   |
| Asynchronous reset to output propagation delay                         | $T_{R2Q}$       |        | 1.547 |        | 1.82  | ns   |
| Asynchronous reset removal time  | $T_{RSTREM}$    | 0.506  |       | 0.595  |       | ns   |
| Asynchronous reset recovery time                                       | $T_{RSTREC}$    | 0.004  |       | 0.005  |       | ns   |
| Asynchronous reset minimum pulse width                                 | $T_{RSTMPW}$    | 0.301  |       | 0.354  |       | ns   |
| Pipelined register asynchronous reset removal time                     | $T_{PLRSTREM}$  | –0.279 |       | –0.328 |       | ns   |
| Pipelined register asynchronous reset recovery time                    | $T_{PLRSTREC}$  | 0.327  |       | 0.385  |       | ns   |
| Pipelined register asynchronous reset minimum pulse width              | $T_{PLRSTMPW}$  | 0.282  |       | 0.332  |       | ns   |
| Synchronous reset setup time   | $T_{SRSTSU}$    | 0.226  |       | 0.265  |       | ns   |
| Synchronous reset hold time  | $T_{SRSTHD}$    | 0.036  |       | 0.043  |       | ns   |
| Write enable setup time  | $T_{WESU}$      | 0.454  |       | 0.534  |       | ns   |
| Write enable hold time   | $T_{WEHD}$      | 0.048  |       | 0.057  |       | ns   |
| Maximum frequency  | $F_{MAX}$       |        | 400   |        | 340   | MHz  |

The following table lists the RAM1K18 – two-port mode for depth × width configuration 512 × 36 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 236 • RAM1K18 – Two-Port Mode for Depth × Width Configuration 512 × 36**

| Parameter  | Symbol          | –1     |       | –Std   |       | Unit |
|--|-----------------|--------|-------|--------|-------|------|
|  |                 | Min    | Max   | Min    | Max   |      |
| Clock period   | $T_{CY}$        | 2.5    |       | 2.941  |       | ns   |
| Clock minimum pulse width high   | $T_{CLKMPWH}$   | 1.125  |       | 1.323  |       | ns   |
| Clock minimum pulse width low  | $T_{CLKMPWL}$   | 1.125  |       | 1.323  |       | ns   |
| Pipelined clock period   | $T_{PLCY}$      | 2.5    |       | 2.941  |       | ns   |
| Pipelined clock minimum pulse width high                               | $T_{PLCLKMPWH}$ | 1.125  |       | 1.323  |       | ns   |
| Pipelined clock minimum pulse width low                                | $T_{PLCLKMPWL}$ | 1.125  |       | 1.323  |       | ns   |
| Read access time with pipeline register                                | $T_{CLK2Q}$     |        | 0.334 |        | 0.393 | ns   |
| Read access time without pipeline register                             |                 |        | 2.25  |        | 2.647 | ns   |
| Address setup time   | $T_{ADDRSU}$    | 0.313  |       | 0.368  |       | ns   |
| Address hold time  | $T_{ADDRHD}$    | 0.274  |       | 0.322  |       | ns   |
| Data setup time  | $T_{DSU}$       | 0.337  |       | 0.396  |       | ns   |
| Data hold time   | $T_{DHD}$       | 0.111  |       | 0.13   |       | ns   |
| Block select setup time  | $T_{BLKSU}$     | 0.207  |       | 0.244  |       | ns   |
| Block select hold time   | $T_{BLKHD}$     | 0.201  |       | 0.237  |       | ns   |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$     |        | 2.25  |        | 2.647 | ns   |
| Block select minimum pulse width                                       | $T_{BLKMPW}$    | 0.186  |       | 0.219  |       | ns   |
| Read enable setup time   | $T_{RDESU}$     | 0.449  |       | 0.528  |       | ns   |
| Read enable hold time  | $T_{RDEHD}$     | 0.167  |       | 0.197  |       | ns   |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)                | $T_{RDPLESU}$   | 0.248  |       | 0.291  |       | ns   |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)                 | $T_{RDPLEHD}$   | 0.102  |       | 0.12   |       | ns   |
| Asynchronous reset to output propagation delay                         | $T_{R2Q}$       |        | 1.506 |        | 1.772 | ns   |
| Asynchronous reset removal time  | $T_{RSTREM}$    | 0.506  |       | 0.595  |       | ns   |
| Asynchronous reset recovery time                                       | $T_{RSTREC}$    | 0.004  |       | 0.005  |       | ns   |
| Asynchronous reset minimum pulse width                                 | $T_{RSTMPW}$    | 0.301  |       | 0.354  |       | ns   |
| Pipelined register asynchronous reset removal time                     | $T_{PLRSTREM}$  | –0.279 |       | –0.328 |       | ns   |
| Pipelined register asynchronous reset recovery time                    | $T_{PLRSTREC}$  | 0.327  |       | 0.385  |       | ns   |
| Pipelined register asynchronous reset minimum pulse width              | $T_{PLRSTMPW}$  | 0.282  |       | 0.332  |       | ns   |
| Synchronous reset setup time   | $T_{SRSTSU}$    | 0.226  |       | 0.265  |       | ns   |
| Synchronous reset hold time  | $T_{SRSTHD}$    | 0.036  |       | 0.043  |       | ns   |
| Write enable setup time  | $T_{WESU}$      | 0.39   |       | 0.458  |       | ns   |
| Write enable hold time   | $T_{WEHD}$      | 0.242  |       | 0.285  |       | ns   |
| Maximum frequency  | $F_{MAX}$       |        | 400   |        | 340   | MHz  |

## 2.3.22 JTAG

**Table 284 • JTAG 1532 for 005, 010, 025, and 050 Devices**

| Parameter                   | Symbol        | 005   |       | 010   |       | 025   |       | 050   |       | Unit |
|-----------------------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|------|
|                             |               | -1    | -Std  | -1    | -Std  | -1    | -Std  | -1    | -Std  |      |
| Clock to Q (data out)       | $T_{TCK2Q}$   | 7.47  | 8.79  | 7.73  | 9.09  | 7.75  | 9.12  | 7.89  | 9.28  | ns   |
| Reset to Q (data out)       | $T_{RSTB2Q}$  | 7.65  | 9     | 6.43  | 7.56  | 6.13  | 7.21  | 7.40  | 8.70  | ns   |
| Test data input setup time  | $T_{DISU}$    | -1.05 | -0.89 | -0.69 | -0.59 | -0.67 | -0.57 | -0.30 | -0.25 | ns   |
| Test data input hold time   | $T_{DIHD}$    | 2.38  | 2.8   | 2.38  | 2.8   | 2.42  | 2.85  | 2.09  | 2.45  | ns   |
| Test mode select setup time | $T_{TMSSU}$   | -0.73 | -0.62 | -1.03 | -1.21 | -1.1  | -0.94 | 0.28  | 0.33  | ns   |
| Test mode select hold time  | $T_{TMDHD}$   | 1.36  | 1.6   | 1.43  | 1.68  | 1.93  | 2.27  | 0.16  | 0.19  | ns   |
| ResetB removal time         | $T_{TRSTREM}$ | -0.77 | -0.65 | -1.08 | -0.92 | -1.33 | -1.13 | -0.45 | -0.38 | ns   |
| ResetB recovery time        | $T_{TRSTREC}$ | -0.76 | -0.65 | -1.07 | -0.91 | -1.34 | -1.14 | -0.45 | -0.38 | ns   |
| TCK maximum frequency       | $F_{TCKMAX}$  | 25    | 21.25 | 25    | 21.25 | 25    | 21.25 | 25.00 | 21.25 | MHz  |

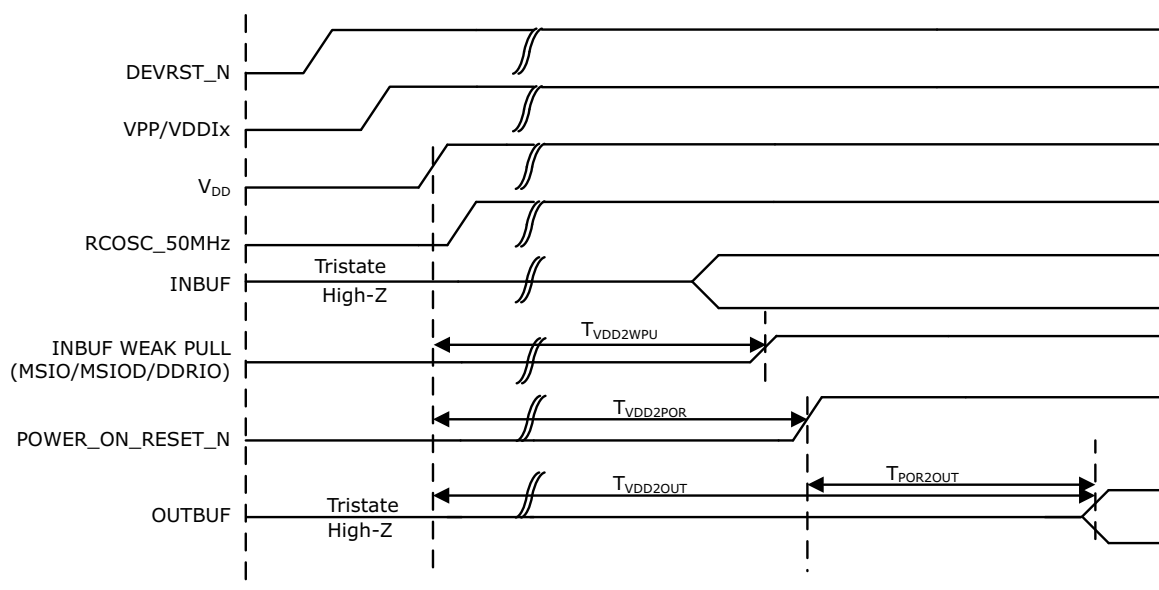
**Table 285 • JTAG 1532 for 060, 090, and 150 Devices**

| Parameter                   | Symbol        | 060   |       | 090   |       | 150   |       | Unit |
|-----------------------------|---------------|-------|-------|-------|-------|-------|-------|------|
|                             |               | -1    | -Std  | -1    | -Std  | -1    | -Std  |      |
| Clock to Q (data out)       | $T_{TCK2Q}$   | 8.38  | 9.86  | 8.96  | 10.54 | 8.66  | 10.19 | ns   |
| Reset to Q (data out)       | $T_{RSTB2Q}$  | 8.54  | 10.04 | 7.75  | 9.12  | 8.79  | 10.34 | ns   |
| Test data input setup time  | $T_{DISU}$    | -1.18 | -1    | -1.31 | -1.11 | -0.96 | -0.82 | ns   |
| Test data input hold time   | $T_{DIHD}$    | 2.52  | 2.97  | 2.68  | 3.15  | 2.57  | 3.02  | ns   |
| Test mode select setup time | $T_{TMSSU}$   | -0.97 | -0.83 | -1.02 | -0.87 | -0.53 | -0.45 | ns   |
| Test mode select hold time  | $T_{TMDHD}$   | 1.7   | 2     | 1.67  | 1.96  | 1.02  | 1.2   | ns   |
| ResetB removal time         | $T_{TRSTREM}$ | -1.21 | -1.03 | -0.76 | -0.65 | -1.03 | -0.88 | ns   |
| ResetB recovery time        | $T_{TRSTREC}$ | -1.21 | -1.03 | -0.77 | -0.65 | -1.03 | -0.88 | ns   |
| TCK maximum frequency       | $F_{TCKMAX}$  | 25    | 21.25 | 25    | 21.25 | 25    | 21.25 | MHz  |

## 2.3.23 System Controller SPI Characteristics



Figure 18 • Power-up to Functional Timing Diagram for IGLOO2



### 2.3.25 DEVRST\_N Characteristics

Table 290 • DEVRST\_N Characteristics for All Devices

| Parameter             | Symbol            | Max | Unit |
|-----------------------|-------------------|-----|------|
| DEVRST_N ramp rate    | $T_{RAMPDEVRSTN}$ | 1   | us   |
| DEVRST_N cycling rate | $F_{MAXPDEVRSTN}$ | 100 | kHz  |

### 2.3.26 DEVRST\_N to Functional Times

The following table lists the SmartFusion2 DEVRST\_N to functional times in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 291 • DEVRST\_N to Functional Times for SmartFusion2

| Symbol           | From             | To                      | Description                                       | Maximum Power-up to Functional Time for SmartFusion2 (uS) |     |     |     |     |     |     |
|------------------|------------------|-------------------------|---|---|-----|-----|-----|-----|-----|-----|
|                  |                  |                         |   | 005   | 010 | 025 | 050 | 060 | 090 | 150 |
| $T_{POR2OUT}$    | POWER_ON_RESET_N | Output available at I/O | Fabric to output                                  | 518   | 501 | 527 | 521 | 422 | 419 | 694 |
| $T_{POR2MSSRST}$ | POWER_ON_RESET_N | MSS_RESET_N_M2F         | Fabric to MSS                                     | 515   | 497 | 524 | 518 | 417 | 414 | 689 |
| $T_{MSSRST2OUT}$ | MSS_RESET_N_M2F  | Output available at I/O | MSS to output                                     | 3.5   | 3.5 | 3.5 | 3.3 | 4.8 | 4.8 | 4.8 |
| $T_{DEVRST2OUT}$ | DEVRST_N         | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 706   | 768 | 715 | 691 | 641 | 635 | 871 |

### 2.3.30 SerDes Electrical and Timing AC and DC Characteristics

PCIe is a high-speed, packet-based, point-to-point, low-pin-count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block.

The following table lists the transmitter parameters in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 296 • Transmitter Parameters**

| Symbol        | Description  | Min   | Max           | Unit          |
|---------------|--|-------|---------------|---------------|
| VTX-DIFF-PP   | Differential swing (2.5 Gbps, 5.0 Gbps)                          | 0.8   | 1.2           | V             |
| VTX-CM-AC-P   | Output common mode voltage (2.5 Gbps)                            |       | 20            | mV            |
| VTX-CM-AC-PP  | Output common mode voltage (5.0 Gbps)                            |       | 100           | mV            |
| VTX-RISE-FALL | Rise and fall time (20% to 80%, 2.5 Gbps)                        | 0.125 |               | UI            |
|               | Rise and fall time (20% to 80%, 5.0 Gbps)                        | 0.15  |               | UI            |
| ZTX-DIFF-DC   | Output impedance–differential                                    | 80    | 120           | $\Omega$      |
| LTX-SKEW      | Lane-to-lane TX skew within a SerDes block (2.5 Gbps)            |       | 500 ps + 2 UI | ps            |
|               | Lane-to-lane TX skew within a SerDes block (5.0 Gbps)            |       | 500 ps + 4 UI | ps            |
| RLTX-DIFF     | Return loss differential mode (2.5 Gbps)                         | –10   |               | dB            |
|               | Return loss differential mode (5.0 Gbps)<br>0.05 GHz to 1.25 GHz | –10   |               | dB            |
|               | 1.25 GHz to 2.5 GHz  | –8    |               | dB            |
| RLTX-CM       | Return loss common mode (2.5 Gbps, 5.0 Gbps)                     | –6    |               | dB            |
| TX-LOCK-RST   | Transmit PLL lock time from reset                                |       | 10            | $\mu\text{s}$ |
| VTX-AMP       | 100 mV setting   | 90    | 150           | mV            |
|               | 400 mV setting   | 320   | 480           | mV            |
|               | 800 mV setting   | 660   | 940           | mV            |
|               | 1200 mV setting  | 950   | 1400          | mV            |

### 2.3.31.2 SmartFusion2 Inter-Integrated Circuit (I<sup>2</sup>C) Characteristics

This section describes the DC and switching of the I<sup>2</sup>C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, see [Figure 21](#), page 125.

The following table lists the I<sup>2</sup>C characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$

**Table 303 • I<sup>2</sup>C Characteristics**

| Parameter   | Symbol                | Min                   | Typ    | Max    | Unit          | Conditions   |
|---|-----------------------|-----------------------|--------|--------|---------------|--|
| Input low voltage   | $V_{IL}$              | -0.3                  |        | 0.8    | V             | See <a href="#">Single-Ended I/O Standards</a> , page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive. |
| Input high voltage  | $V_{IH}$              | 2                     |        | 3.45   | V             | See <a href="#">Single-Ended I/O Standards</a> , page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive. |
| Hysteresis of schmitt triggered inputs for $V_{DDI} > 2\text{ V}$                       | $V_{HYS}$             | $0.05 \times V_{DDI}$ |        |        | V             | See <a href="#">Table 28</a> , page 23 for more information.   |
| Input current high  | $I_{IL}$              |                       |        | 10     | $\mu\text{A}$ | See <a href="#">Single-Ended I/O Standards</a> , page 24 for more information.   |
| Input current low   | $I_{IH}$              |                       |        | 10     | $\mu\text{A}$ | See <a href="#">Single-Ended I/O Standards</a> , page 24 for more information.   |
| Input rise time   | $T_{ir}$              |                       |        | 1000   | ns            | Standard mode  |
|   |                       |                       |        | 300    | ns            | Fast mode  |
| Input fall time   | $T_{if}$              |                       |        | 300    | ns            | Standard mode  |
|   |                       |                       |        | 300    | ns            | Fast mode  |
| Maximum output voltage low (open drain) at 3 mA sink current for $V_{DDI} > 2\text{ V}$ | $V_{OL}$              |                       |        | 0.4    | V             | See <a href="#">Single-Ended I/O Standards</a> , page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive. |
| Pin capacitance   | $C_{in}$              |                       |        | 10     | pF            | $V_{IN} = 0$ , $f = 1.0\text{ MHz}$  |
| Output fall time from $V_{IHMin}$ to $V_{ILMax}^1$                                      | $t_{OF}^1$            |                       | 21.04  |        | ns            | $V_{IHmin}$ to $V_{ILMax}$ , $C_{LOAD} = 400\text{ pF}$  |
|   |                       |                       | 5.556  |        | ns            | $V_{IHmin}$ to $V_{ILMax}$ , $C_{LOAD} = 100\text{ pF}$  |
| Output rise time from $V_{ILMax}$ to $V_{IHMin}^1$                                      | $t_{OR}^1$            |                       | 19.887 |        | ns            | $V_{ILMax}$ to $V_{IHmin}$ , $C_{LOAD} = 400\text{ pF}$  |
|   |                       |                       | 5.218  |        | ns            | $V_{ILMax}$ to $V_{IHmin}$ , $C_{LOAD} = 100\text{ pF}$  |
| Output buffer maximum pull-down resistance <sup>2,3</sup>                               | $R_{pull-up}^{2,3}$   |                       |        | 50     | $\Omega$      |  |
| Output buffer maximum pull-up resistance <sup>2,4</sup>                                 | $R_{pull-down}^{2,4}$ |                       |        | 131.25 | $\Omega$      |  |

### 2.3.31.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI\_x\_CLK. For timing parameter definitions, see [Figure 22](#), page 128.

The following table lists the SPI characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$

**Table 305 • SPI Characteristics for All Devices**

| Symbol  | Description  | Min   | Typ  | Max | Unit          | Conditions  |
|---------|--|-------|------|-----|---------------|---|
| SPIFMAX | Maximum operating frequency of SPI interface                               |       |      | 20  | MHz           |   |
| sp1     | SPI_[0 1]_CLK minimum period   |       |      |     |               |   |
|         | SPI_[0 1]_CLK = PCLK/2   | 12    |      |     | ns            |   |
|         | SPI_[0 1]_CLK = PCLK/4   | 24.1  |      |     | ns            |   |
|         | SPI_[0 1]_CLK = PCLK/8   | 48.2  |      |     | ns            |   |
|         | SPI_[0 1]_CLK = PCLK/16  | 0.1   |      |     | $\mu\text{s}$ |   |
|         | SPI_[0 1]_CLK = PCLK/32  | 0.19  |      |     | $\mu\text{s}$ |   |
|         | SPI_[0 1]_CLK = PCLK/64  | 0.39  |      |     | $\mu\text{s}$ |   |
|         | SPI_[0 1]_CLK = PCLK/128   | 0.77  |      |     | $\mu\text{s}$ |   |
| sp2     | SPI_[0 1]_CLK minimum pulse width high                                     |       |      |     |               |   |
|         | SPI_[0 1]_CLK = PCLK/2   | 6     |      |     | ns            |   |
|         | SPI_[0 1]_CLK = PCLK/4   | 12.05 |      |     | ns            |   |
|         | SPI_[0 1]_CLK = PCLK/8   | 24.1  |      |     | ns            |   |
|         | SPI_[0 1]_CLK = PCLK/16  | 0.05  |      |     | $\mu\text{s}$ |   |
|         | SPI_[0 1]_CLK = PCLK/32  | 0.095 |      |     | $\mu\text{s}$ |   |
|         | SPI_[0 1]_CLK = PCLK/64  | 0.195 |      |     | $\mu\text{s}$ |   |
|         | SPI_[0 1]_CLK = PCLK/128   | 0.385 |      |     | $\mu\text{s}$ |   |
| sp3     | SPI_[0 1]_CLK minimum pulse width low                                      |       |      |     |               |   |
|         | SPI_[0 1]_CLK = PCLK/2   | 6     |      |     | ns            |   |
|         | SPI_[0 1]_CLK = PCLK/4   | 12.05 |      |     | ns            |   |
|         | SPI_[0 1]_CLK = PCLK/8   | 24.1  |      |     | ns            |   |
|         | SPI_[0 1]_CLK = PCLK/16  | 0.05  |      |     | $\mu\text{s}$ |   |
|         | SPI_[0 1]_CLK = PCLK/32  | 0.095 |      |     | $\mu\text{s}$ |   |
|         | SPI_[0 1]_CLK = PCLK/64  | 0.195 |      |     | $\mu\text{s}$ |   |
|         | SPI_[0 1]_CLK = PCLK/128   | 0.385 |      |     | $\mu\text{s}$ |   |
| sp4     | SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) <sup>1</sup> |       | 2.77 |     | ns            | I/O Configuration:<br>LVCMOS 2.5 V–<br>8 mA<br>AC loading: 35 pF<br>Test conditions:<br>Typical voltage,<br>25 °C |

## 2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 308 • MMUART Characteristics**

| Parameter       | Description  | -1     | -Std  | Unit |
|-----------------|--|--------|-------|------|
| FMMUART_REF_CLK | Internally sourced MMUART reference clock frequency. | 166    | 142   | MHz  |
| BAUDMMUARTTx    | Maximum transmit baud rate                           | 10.375 | 8.875 | Mbps |
| BAUDMMUARTRx    | Maximum receive baud rate                            | 10.375 | 8.875 | Mbps |

## 2.3.35 IGLOO2 Specifications

### 2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 309 • Maximum Frequency for HPMS Main Clock**

| Symbol   | Description                               | -1  | -Std | Unit |
|----------|---|-----|------|------|
| HPMS_CLK | Maximum frequency for the HPMS main clock | 166 | 142  | MHz  |

### 2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI\_0\_CLK. For timing parameter definitions, see [Figure 23](#), page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 310 • SPI Characteristics for All Devices**

| Symbol                   | Description                                  | Min  | Typ | Max           | Unit          | Conditions |
|--------------------------|--|------|-----|---------------|---------------|------------|
| SPIFMAX                  | Maximum operating frequency of SPI interface |      |     | 20            | MHz           |            |
| sp1                      | SPI_[0 1]_CLK minimum period                 |      |     |               |               |            |
|                          | SPI_[0 1]_CLK = PCLK/2                       | 12   |     |               | ns            |            |
|                          | SPI_[0 1]_CLK = PCLK/4                       | 24.1 |     |               | ns            |            |
|                          | SPI_[0 1]_CLK = PCLK/8                       | 48.2 |     |               | ns            |            |
|                          | SPI_[0 1]_CLK = PCLK/16                      | 0.1  |     |               | $\mu\text{s}$ |            |
|                          | SPI_[0 1]_CLK = PCLK/32                      | 0.19 |     |               | $\mu\text{s}$ |            |
|                          | SPI_[0 1]_CLK = PCLK/64                      | 0.39 |     |               | $\mu\text{s}$ |            |
| SPI_[0 1]_CLK = PCLK/128 | 0.77   |      |     | $\mu\text{s}$ |               |            |