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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

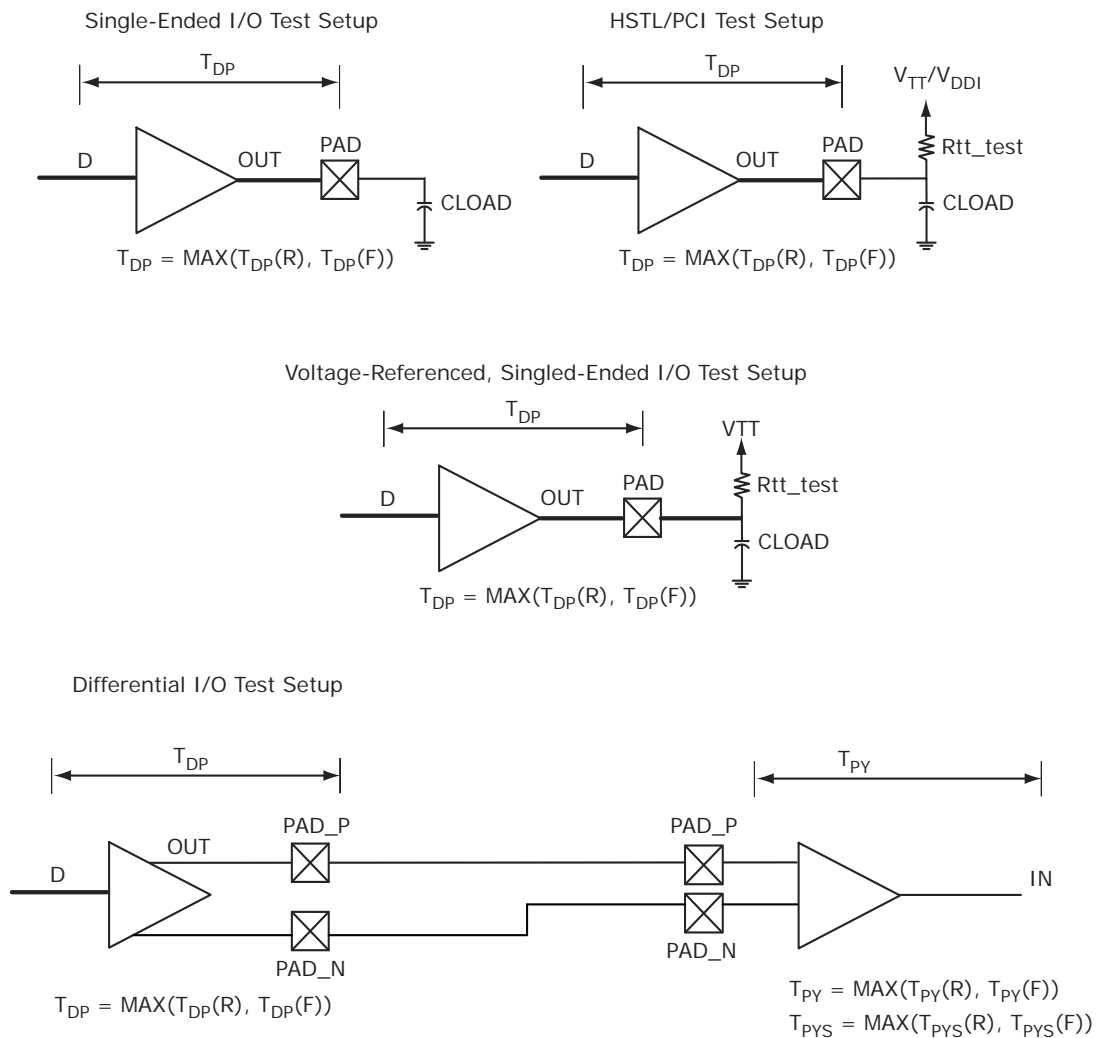
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 60K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-LFBGA
Supplier Device Package	400-VFBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s060-vfg400">https://www.e-xfl.com/product-detail/microchip-technology/m2s060-vfg400</a>

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### 2.3.5.2 Output Buffer and AC Loading

The following figure shows the output buffer and AC loading.

**Figure 4 • Output Buffer AC Loading**



**Table 43 • LVCMOS 2.5 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	1.2	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega\sigma$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**Table 44 • LVCMOS 2.5 V Transmitter Drive Strength Specifications**

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (With Software Default Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	4 mA	4 mA	$V_{DDI} - 0.4$	0.4	4	4
6 mA	6 mA	6 mA	$V_{DDI} - 0.4$	0.4	6	6
8 mA	8 mA	8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	12 mA	12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA		16 mA	$V_{DDI} - 0.4$	0.4	16	16

**Note:** For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at:  
[www.microsemi.com/soc/download/ibis/default.aspx](http://www.microsemi.com/soc/download/ibis/default.aspx).

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

**Table 45 • LVCMOS 2.5 V Receiver Characteristics (Input Buffers)**

	On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
		-1	-Std	-1	-Std	
LVCMOS 2.5 V (for DDRIO I/O bank)	None	1.823	2.145	1.932	2.274	ns
LVCMOS 2.5 V (for MSIO I/O bank)	None	2.486	2.925	2.495	2.935	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	None	2.29	2.694	2.305	2.712	ns

**Table 46 • LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.657	4.302	3.393	3.991	3.675	4.323	3.894	4.582	3.552	4.18	ns
	Medium	3.374	3.97	3.139	3.693	3.396	3.995	3.635	4.277	3.253	3.828	ns
	Medium fast	3.239	3.811	3.036	3.572	3.261	3.836	3.519	4.141	3.128	3.681	ns
	Fast	3.224	3.793	3.029	3.563	3.246	3.818	3.512	4.132	3.119	3.67	ns

**Table 100 • HSTL AC Test Parameter Specification**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	0.75	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Reference resistance for data test path for HSTL15 Class I ( $T_{DP}$ )	$RTT\_TEST$	50	$\Omega$
Reference resistance for data test path for HSTL15 Class II ( $T_{DP}$ )	$RTT\_TEST$	25	$\Omega$
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**AC Switching Characteristics**

Worst-case commercial conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ , worst-case  $V_{DDI}$ .

**Table 101 • HSTL Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)**

	On-Die Termination (ODT)	$T_{PY}$		
		-1	-Std	Unit
Pseudo differential	None	1.605	1.888	ns
	47.8	1.614	1.898	ns
True differential	None	1.622	1.909	ns
	47.8	1.628	1.916	ns

**Table 102 • HSTL Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
<b>HSTL Class I</b>											
Single-ended	2.6	3.059	2.514	2.958	2.514	2.958	2.431	2.86	2.431	2.86	ns
Differential	2.621	3.083	2.648	3.115	2.647	3.113	2.925	3.442	2.923	3.44	ns
<b>HSTL Class II</b>											
Single-ended	2.511	2.954	2.488	2.927	2.49	2.93	2.409	2.833	2.411	2.836	ns
Differential	2.528	2.974	2.552	3.003	2.551	3.001	2.897	3.409	2.896	3.408	ns

**2.3.6.2 Stub-Series Terminated Logic**

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

**Table 136 • SSTL15 AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	0.75	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Reference resistance for data test path for SSTL15 Class I ( $T_{DP}$ )	$RTT\_TEST$	50	$\Omega$
Reference resistance for data test path for SSTL15 Class II ( $T_{DP}$ )	$RTT\_TEST$	25	$\Omega$
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 1.425\text{ V}$

**Table 137 • DDR3/SSTL15 Receiver Characteristics for DDRIO I/O Bank – with Calibration Only**

		$T_{PY}$		
On-Die Termination (ODT)		-1	-Std	Unit
Pseudo differential	None	1.605	1.888	ns
	20	1.616	1.901	ns
	30	1.613	1.897	ns
	40	1.611	1.895	ns
	60	1.609	1.893	ns
	120	1.607	1.89	ns
True differential	None	1.623	1.91	ns
	20	1.637	1.926	ns
	30	1.63	1.918	ns
	40	1.626	1.914	ns
	60	1.622	1.91	ns
	120	1.619	1.905	ns

**Table 138 • DDR3/SSTL15 Transmitter Characteristics (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
<b>DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)</b>											
Single-ended	2.533	2.98	2.522	2.967	2.523	2.968	2.427	2.855	2.428	2.856	ns
Differential	2.555	3.005	3.073	3.615	3.073	3.615	2.416	2.843	2.416	2.843	ns
<b>DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)</b>											
Single-ended	2.53	2.977	2.514	2.958	2.516	2.96	2.422	2.849	2.425	2.852	ns
Differential	2.552	3.002	2.591	3.048	2.59	3.047	2.882	3.391	2.881	3.39	ns

### 2.3.7.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 173 • B-LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V

**Table 174 • B-LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	$V_I$	0	2.925	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 175 • B-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	$V_{OH}$	1.25	1.425	1.6	V
DC output logic low	$V_{OL}$	0.9	1.075	1.25	V

**Table 176 • B-LVDS DC Differential Voltage Specification**

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	$V_{OD}$	65	460	mV
Output common mode voltage (for MSIO I/O bank only)	$V_{OCM}$	1.1	1.5	V
Input common mode voltage	$V_{ICM}$	0.05	2.4	V
Input differential voltage	$V_{ID}$	0.1	$V_{DDI}$	V

**Table 177 • B-LVDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	500	Mbps	AC loading: 2 pF / 100 $\Omega$ differential load

**Table 178 • B-LVDS AC Impedance Specifications**

Parameter	Symbol	Typ	Unit
Termination resistance	$R_T$	27	$\Omega$

**Table 179 • B-LVDS AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	Cross point	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF

**Table 191 • M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

On-Die Termination (ODT)	T <sub>PY</sub>		Unit
	-1	-Std	
None	2.495	2.934	ns
100	2.495	2.935	ns

**Table 192 • M-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub>		T <sub>LZ</sub>		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.258	2.656	2.348	2.762	2.334	2.746	2.123	2.497	2.125	2.5	ns

### 2.3.7.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

#### Mini-LVDS Minimum and Maximum Input and Output Levels

**Table 193 • Mini-LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>DDI</sub>	2.375	2.5	2.625	V

**Table 194 • Mini-LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC Input voltage	V <sub>I</sub>	0	2.925	V

**Table 195 • Mini-LVDS DC Output Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V <sub>OH</sub>	1.25	1.425	1.6	V
DC output logic low	V <sub>OL</sub>	0.9	1.075	1.25	V

**Table 196 • Mini-LVDS DC Differential Voltage Specification**

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing	V <sub>OD</sub>	300	600	mV
Output common mode voltage	V <sub>OCM</sub>	1	1.4	V
Input common mode voltage	V <sub>ICM</sub>	0.3	1.2	V
Input differential voltage	V <sub>ID</sub>	100	600	mV

**Table 197 • Mini-LVDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D <sub>MAX</sub>	520	Mbps	AC loading: 2 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank)	D <sub>MAX</sub>	700	Mbps	AC loading: 2 pF / 100 Ω differential load



### AC Switching Characteristics

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$ .

**Table 210 • RSDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.855	3.359	ns
100	2.85	3.353	ns

**Table 211 • RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.602	3.061	ns
100	2.597	3.055	ns

**Table 212 • RSDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.097	2.467	2.303	2.709	2.291	2.695	1.961	2.307	1.947	2.29	ns

**Table 213 • RSDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
No pre-emphasis	1.614	1.899	1.559	1.834	1.55	1.823	1.59	1.87	1.575	1.852	ns
Min pre-emphasis	1.604	1.887	1.742	2.05	1.728	2.032	1.889	2.222	1.858	2.185	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

#### 2.3.7.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

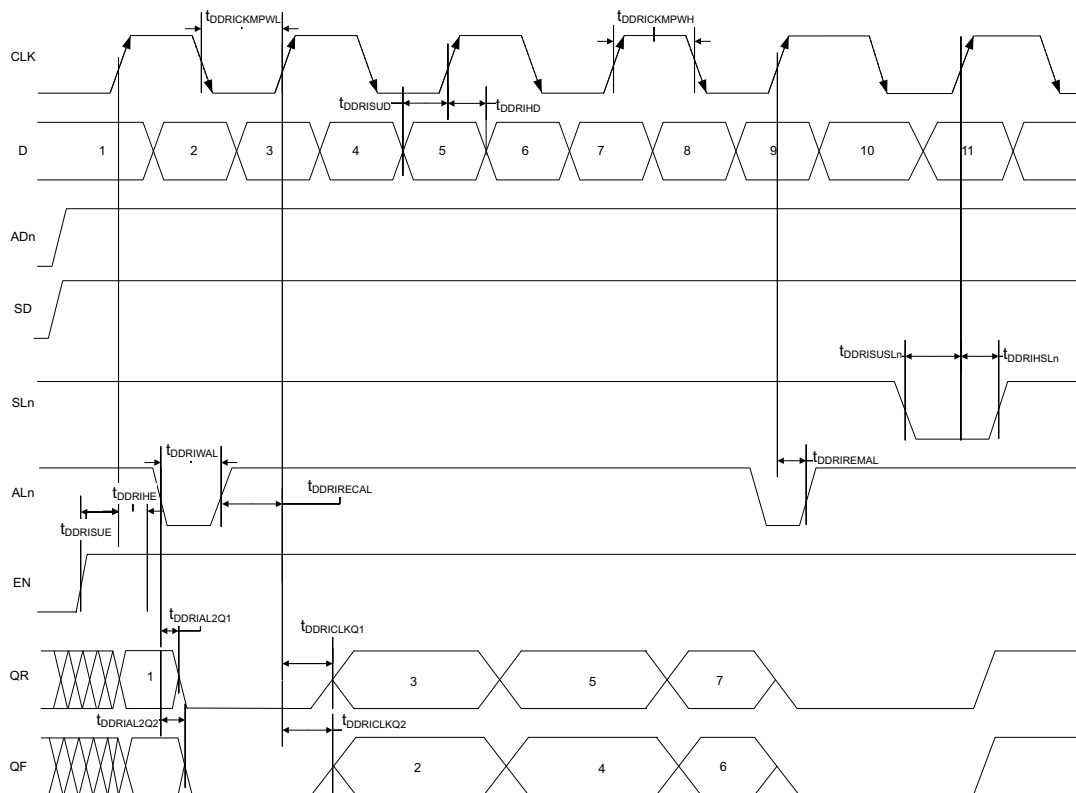
#### Minimum and Maximum Input and Output Levels (Applicable to MSIO I/O Bank Only)

**Table 214 • LVPECL Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	3.15	3.3	3.45	V

### 2.3.9.2 Input DDR Timing Diagram

Figure 11 • Input DDR Timing Diagram



### 2.3.9.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

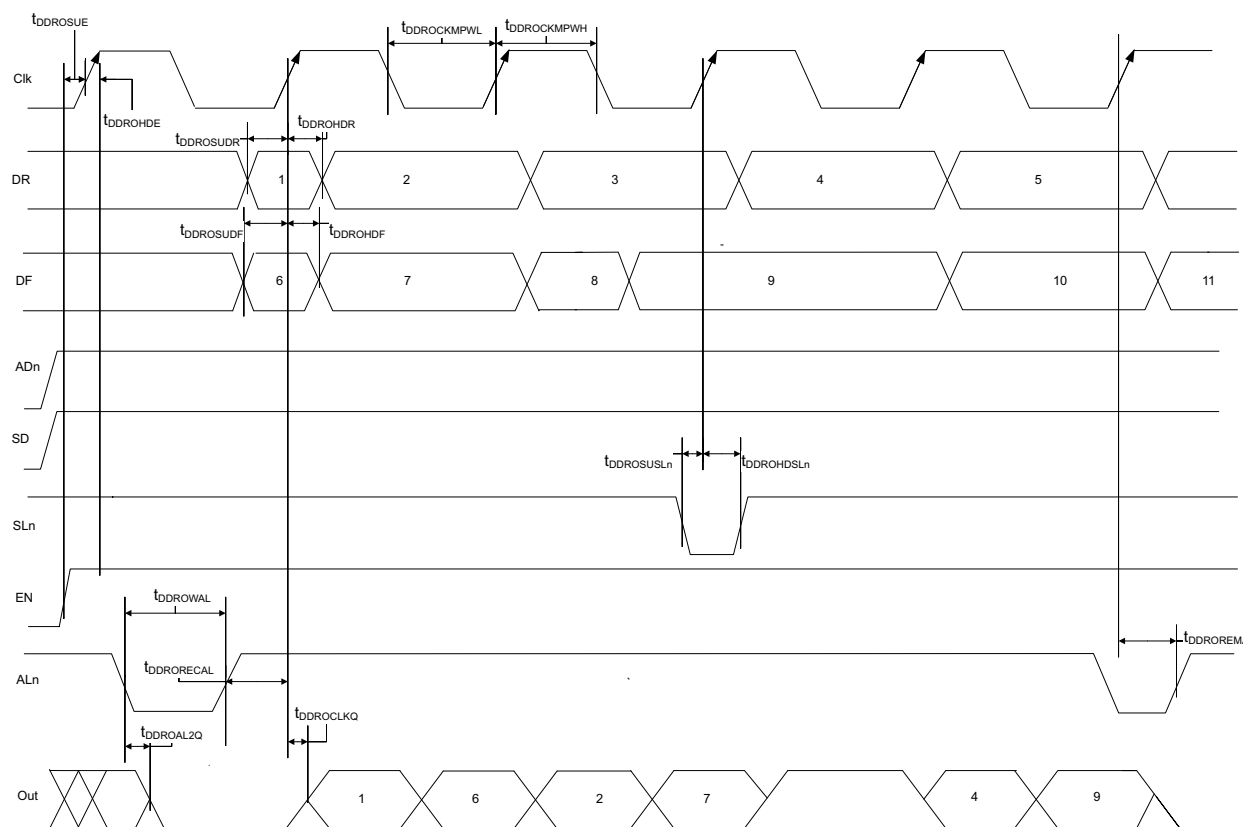
Table 221 • Input DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDRICKLKQ1}$	Clock-to-Out Out_QR for input DDR	B, C	0.16	0.188	ns
$T_{DDRICKLKQ2}$	Clock-to-Out Out_QF for input DDR	B, D	0.166	0.195	ns
$T_{DDRISUD}$	Data setup for input DDR	A, B	0.357	0.421	ns
$T_{DDRIHD}$	Data hold for input DDR	A, B	0	0	ns
$T_{DDRISUE}$	Enable setup for input DDR	E, B	0.46	0.542	ns
$T_{DDRIHE}$	Enable hold for input DDR	E, B	0	0	ns
$T_{DDRISUSL}$	Synchronous load setup for input DDR	G, B	0.46	0.542	ns
$T_{DDRIHSL}$	Synchronous load hold for input DDR	G, B	0	0	ns
$T_{DDRIR2Q1}$	Asynchronous load-to-out QR for input DDR	F, C	0.587	0.69	ns
$T_{DDRIR2Q2}$	Asynchronous load-to-out QF for input DDR	F, D	0.541	0.636	ns
$T_{DDRIREMAL}$	Asynchronous load removal time for input DDR	F, B	0	0	ns
$T_{DDRIRECAL}$	Asynchronous load recovery time for input DDR	F, B	0.074	0.087	ns

**Table 221 • Input DDR Propagation Delays (continued)**

Symbol	Description	Measuring Nodes (from, to)	-1		Unit
			-Std		
$T_{DDRIWAL}$	Asynchronous load minimum pulse width for input DDR	F, F	0.304	0.357	ns
$T_{DDRICKMPWH}$	Clock minimum pulse width high for input DDR	B, B	0.075	0.088	ns
$T_{DDRICKMPWL}$	Clock minimum pulse width low for input DDR	B, B	0.159	0.187	ns

**Figure 13 • Output DDR Timing Diagram**



**2.3.9.5 Timing Characteristics**

The following table lists the output DDR propagation delays in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 222 • Output DDR Propagation Delays**

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDROCLKQ}$	Clock-to-out of DDR for output DDR	E, G	0.263	0.309	ns
$T_{DDROSUDF}$	Data_F data setup for output DDR	F, E	0.143	0.168	ns
$T_{DDROSUDR}$	Data_R data setup for output DDR	A, E	0.19	0.223	ns
$T_{DDROHDF}$	Data_F data hold for output DDR	F, E	0	0	ns
$T_{DDROHDR}$	Data_R data hold for output DDR	A, E	0	0	ns
$T_{DDROSUE}$	Enable setup for input DDR	B, E	0.419	0.493	ns
$T_{DDROHE}$	Enable hold for input DDR	B, E	0	0	ns
$T_{DDROSUSLn}$	Synchronous load setup for input DDR	D, E	0.196	0.231	ns
$T_{DDROHSLn}$	Synchronous load hold for input DDR	D, E	0	0	ns
$T_{DDROAL2Q}$	Asynchronous load-to-out for output DDR	C, G	0.528	0.621	ns
$T_{DDROREMA}$	Asynchronous load removal time for output DDR	C, E	0	0	ns
$T_{DDRORECAL}$	Asynchronous load recovery time for output DDR	C, E	0.034	0.04	ns

**Table 222 • Output DDR Propagation Delays (continued)**

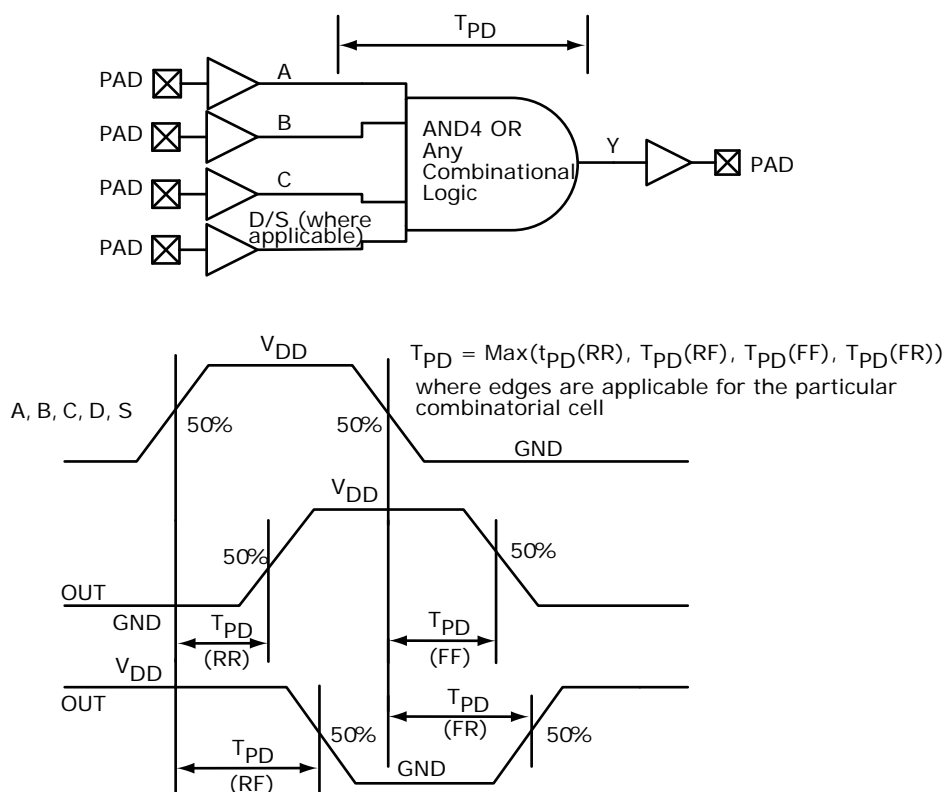
Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDROWAL}$	Asynchronous load minimum pulse width for output DDR	C, C	0.304	0.357	ns
$T_{DDROCKMPWH}$	Clock minimum pulse width high for the output DDR	E, E	0.075	0.088	ns
$T_{DDROCKMPWL}$	Clock minimum pulse width low for the output DDR	E, E	0.159	0.187	ns

## 2.3.10 Logic Element Specifications

### 2.3.10.1 4-input LUT (LUT-4)

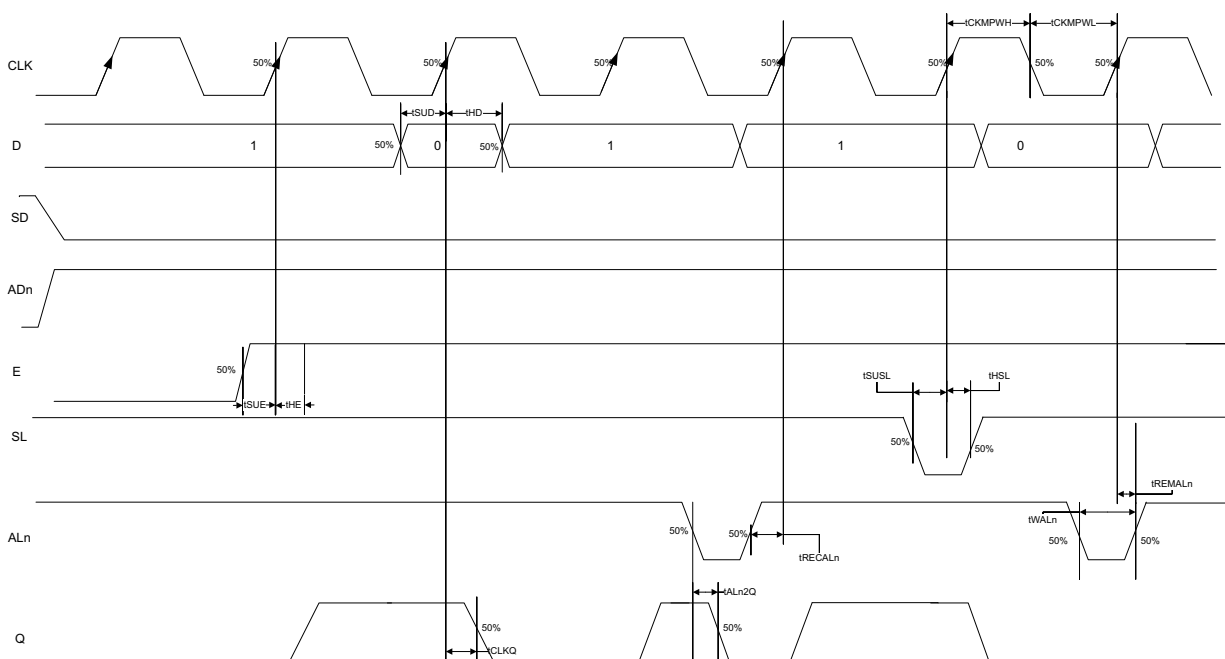
The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, see *SmartFusion2 and IGLOO2 Macro Library Guide*.

**Figure 14 • LUT-4**



The following figure shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

**Figure 16 • Sequential Module Timing Diagram**



### 2.3.10.3.1 Timing Characteristics

The following table lists the register delays in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 224 • Register Delays**

Parameter	Symbol	-1	-Std	Unit
Clock-to-Q of the core register	$T_{CLKQ}$	0.108	0.127	ns
Data setup time for the core register	$T_{SUD}$	0.254	0.298	ns
Data hold time for the core register	$T_{HD}$	0	0	ns
Enable setup time for the core register	$T_{SUE}$	0.335	0.394	ns
Enable hold time for the core register	$T_{HE}$	0	0	ns
Synchronous load setup time for the core register	$T_{SUSL}$	0.335	0.394	ns
Synchronous load hold time for the core register	$T_{HSL}$	0	0	ns
Asynchronous Clear-to-Q of the core register (ADn = 1)	$T_{ALN2Q}$	0.473	0.556	ns
Asynchronous preset-to-Q of the core register (ADn = 0)		0.451	0.531	ns
Asynchronous load removal time for the core register	$T_{RECALN}$	0	0	ns
Asynchronous load recovery time for the core register	$T_{RECALN}$	0.353	0.415	ns
Asynchronous load minimum pulse width for the core register	$T_{WALN}$	0.266	0.313	ns
Clock minimum pulse width high for the core register	$T_{CKMPWH}$	0.065	0.077	ns
Clock minimum pulse width low for the core register	$T_{CKMPWL}$	0.139	0.164	ns

**Table 232 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 (continued)**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Address setup time	$T_{ADDRSU}$	0.475		0.559		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.336		0.395		ns
Data hold time	$T_{DHD}$	0.082		0.096		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns
Block select hold time	$T_{BLKHD}$	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		1.529		1.799	ns
Block select minimum pulse width	$T_{BLKMPW}$	0.186		0.219		ns
Read enable setup time	$T_{RDESU}$	0.485		0.57		ns
Read enable hold time	$T_{RDEHD}$	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	$T_{R2Q}$		1.514		1.781	ns
Asynchronous reset removal time	$T_{RSTREM}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTREC}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	$T_{RSTMPW}$	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTSU}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTHD}$	0.036		0.043		ns
Write enable setup time	$T_{WESU}$	0.415		0.488		ns
Write enable hold time	$T_{WEHD}$	0.048		0.057		ns
Maximum frequency	$F_{MAX}$		400		340	MHz

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 233 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	$T_{CY}$	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	$T_{PLCY}$	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 8K × 2 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 234 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	$T_{CY}$	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	$T_{PLCY}$	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register				0.32	0.377	ns
Read access time without pipeline register	$T_{CLK2Q}$			2.272	2.673	ns
Access time with feed-through write timing				1.511	1.778	ns
Address setup time	$T_{ADDRSU}$	0.612		0.72		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.33		0.388		ns
Data hold time	$T_{DHD}$	0.082		0.096		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns
Block select hold time	$T_{BLKHD}$	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$			1.511	1.778	ns
Block select minimum pulse width	$T_{BLKMPW}$	0.186		0.219		ns
Read enable setup time	$T_{RDESU}$	0.529		0.622		ns
Read enable hold time	$T_{RDEHD}$	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	$T_{R2Q}$			1.528	1.797	ns
Asynchronous reset removal time	$T_{RSTREM}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTREC}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	$T_{RSTMPW}$	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTSU}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTHD}$	0.036		0.043		ns
Write enable setup time	$T_{WESU}$	0.488		0.574		ns
Write enable hold time	$T_{WEHD}$	0.048		0.057		ns
Maximum frequency	$F_{MAX}$			400	340	MHz



**Table 237 •  $\mu$ SRAM (RAM64x18) in 64 × 18 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.026		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

The following table lists the  $\mu$ SRAM in 64 × 16 mode in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 238 •  $\mu$ SRAM (RAM64x16) in 64 × 16 Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	$T_{CY}$	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	$T_{PLCY}$	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	$T_{CLK2Q}$		0.266		0.313	ns
Read access time without pipeline register				1.677		1.973
Read address setup time in synchronous mode	$T_{ADDRSU}$	0.301		0.354		ns
Read address setup time in asynchronous mode			1.856		2.184	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.091		0.107		ns
Read address hold time in asynchronous mode			-0.778		-0.915	
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHD}$	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	$T_{RSTREM}$	-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)			0.046		0.054	
Read asynchronous reset recovery time (pipelined clock)	$T_{RSTREC}$	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)			0.236		0.278	
Read asynchronous reset to output propagation delay (with pipelined register enabled)	$T_{R2Q}$		0.835		0.983	ns
Read synchronous reset setup time	$T_{SRSTSU}$	0.271		0.319		ns

**Table 277 • Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz) (continued)**

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Startup time (with regard to stable oscillator output)	SUXTAL			0.8	ms	005, 010, 025, and 050 devices
				1.0	ms	090 and 150 devices

**Table 278 • Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)**

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		2		MHz	
Accuracy	ACCXTAL			0.00105	%	050 devices
				0.003	%	005, 010, 025, 090, and 150 devices
				0.004	%	060 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		1	5	ns	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		1	5	ns	
Operating current	IDYNXTAL		0.3		mA	
Input logic level high	VIHXTAL	0.9 V <sub>PP</sub>			V	
Input logic level low	VILXTAL			0.1 V <sub>PP</sub>	V	
Startup time (with regard to stable oscillator output)	SUXTAL			4.5	ms	010 and 050 devices
				5	ms	005 and 025 devices
				7	ms	090 and 150 devices

**Table 279 • Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)**

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		32		kHz	
Accuracy	ACCXTAL			0.004	%	005, 010, 025, 050, 060, and 090 devices
				0.005	%	150 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		150	300	ns	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		150	300	ns	
Operating current	IDYNXTAL			0.044	mA	010 and 050 devices
				0.060	mA	005, 025, 060, 090, and 150 devices
Input logic level high	VIHXTAL	0.9 V <sub>PP</sub>			V	
Input logic level low	VILXTAL			0.1 V <sub>PP</sub>	V	
Startup time (with regard to stable oscillator output)	SUXTAL			115	ms	005, 025, 050, 090, and 150 devices
				126	ms	010 devices

### 2.3.31.2 SmartFusion2 Inter-Integrated Circuit (I<sup>2</sup>C) Characteristics

This section describes the DC and switching of the I<sup>2</sup>C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, see Figure 21, page 125.

The following table lists the I<sup>2</sup>C characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$

**Table 303 • I<sup>2</sup>C Characteristics**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input low voltage	$V_{IL}$	-0.3		0.8	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive.
Input high voltage	$V_{IH}$	2		3.45	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive.
Hysteresis of schmitt triggered inputs for $V_{DDI} > 2\text{ V}$	$V_{HYS}$	$0.05 \times V_{DDI}$			V	See Table 28, page 23 for more information.
Input current high	$I_{IL}$			10	$\mu\text{A}$	See Single-Ended I/O Standards, page 24 for more information.
Input current low	$I_{IH}$			10	$\mu\text{A}$	See Single-Ended I/O Standards, page 24 for more information.
Input rise time	$T_{ir}$			1000	ns	Standard mode
				300	ns	Fast mode
Input fall time	$T_{if}$			300	ns	Standard mode
				300	ns	Fast mode
Maximum output voltage low (open drain) at 3 mA sink current for $V_{DDI} > 2\text{ V}$	$V_{OL}$			0.4	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive.
Pin capacitance	$C_{in}$			10	pF	$V_{IN} = 0$ , $f = 1.0\text{ MHz}$
Output fall time from $V_{IHMin}$ to $V_{ILMax}^1$	$t_{OF}^1$		21.04		ns	$V_{IHmin}$ to $V_{ILMax}$ , CLOAD = 400 pF
			5.556		ns	$V_{IHmin}$ to $V_{ILMax}$ , CLOAD = 100 pF
Output rise time from $V_{ILMax}$ to $V_{IHMin}^1$	$t_{OR}^1$		19.887		ns	$V_{ILMax}$ to $V_{IHmin}$ , CLOAD = 400 pF
			5.218		ns	$V_{ILMax}$ to $V_{IHmin}$ , CLOAD = 100 pF
Output buffer maximum pull-down resistance <sup>2,3</sup>	$R_{pull-up}^{2,3}$			50	$\Omega$	
Output buffer maximum pull-up resistance <sup>2,4</sup>	$R_{pull-down}^{2,4}$			131.25	$\Omega$	

**Table 303 • I2C Characteristics (continued)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Maximum data rate	$D_{MAX}$			400	Kbps	Fast mode
				100	Kbps	Standard mode
Pulse width of spikes which must be suppressed by the input filter	$T_{FILT}$		50		ns	Fast mode

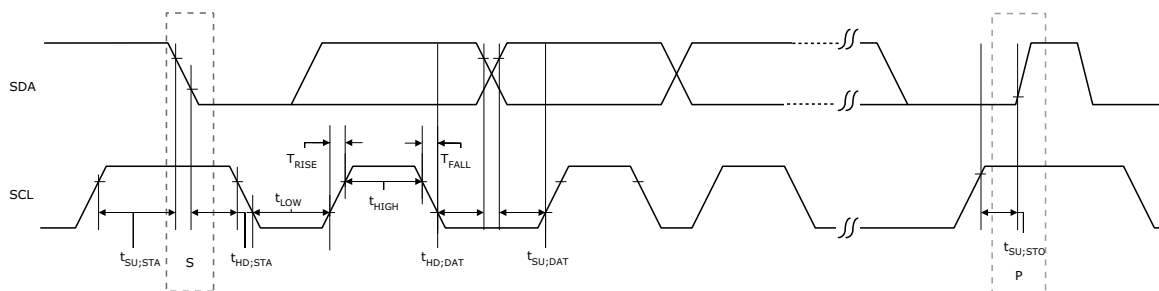
1. These values are provided for MSIO Bank–LVTTTL 8 mA Low Drive at 25 °C, typical conditions. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on  $V_{DDIX}$ , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
3.  $R(PULL-DOWN-MAX) = (VOLspec)/IOLspec$ .
4.  $R(PULL-UP-MAX) = (VDDImax-VOHspec)/IOHspec$ .

The following table lists the I<sup>2</sup>C switching characteristics in worst-case industrial conditions when  $T_J = 100\text{ °C}$ ,  $V_{DD} = 1.14\text{ V}$

**Table 304 • I2C Switching Characteristics**

Parameter	Symbol	-1		Unit
		Min	Min	
Low period of I2C_x_SCL	$T_{LOW}$	1	1	PCLK cycles
High period of I2C_x_SCL	$T_{HIGH}$	1	1	PCLK cycles
START hold time	$T_{HD;STA}$	1	1	PCLK cycles
START setup time	$T_{SU;STA}$	1	1	PCLK cycles
DATA hold time	$T_{HD;DAT}$	1	1	PCLK cycles
DATA setup time	$T_{SU;DAT}$	1	1	PCLK cycles
STOP setup time	$T_{SU;STO}$	1	1	PCLK cycles

**Figure 21 • I<sup>2</sup>C Timing Parameter Definition**



**Table 310 • SPI Characteristics for All Devices (continued)**

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp2	SPI_[0 1]_CLK minimum pulse width high					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			µs	
	SPI_[0 1]_CLK = PCLK/32	0.095			µs	
	SPI_[0 1]_CLK = PCLK/64	0.195			µs	
	SPI_[0 1]_CLK = PCLK/128	0.385			µs	
sp3	SPI_[0 1]_CLK minimum pulse width low					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			µs	
	SPI_[0 1]_CLK = PCLK/32	0.095			µs	
	SPI_[0 1]_CLK = PCLK/64	0.195			µs	
	SPI_[0 1]_CLK = PCLK/128	0.385			µs	
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) <sup>1</sup>		2.77		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%–90%) <sup>1</sup>		2.906		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0 1]_DI setup time <sup>2</sup>	12			ns	
sp9m	SPI_[0 1]_DI hold time <sup>2</sup>	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0 1]_DI setup time <sup>2</sup>	2			ns	
sp9s	SPI_[0 1]_DI hold time <sup>2</sup>	7			ns	