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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

| | |
|-------------------------|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | ARM® Cortex®-M3 |
| Flash Size | 256KB |
| RAM Size | 64KB |
| Peripherals | DDR, PCIe, SERDES |
| Connectivity | CANbus, Ethernet, I ² C, SPI, UART/USART, USB |
| Speed | 166MHz |
| Primary Attributes | FPGA - 60K Logic Modules |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2s060t-fgg484 |

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- Added Table 244, page 94 and Table 256, page 99 (SAR 73971).
- Updated the SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 71171).
- Added the DEVRST_N Characteristics, page 116 (SAR 64100, 72103).
- Added Table 298, page 122 (SAR 71897).
- Updated Table 25, page 22, Table 26, page 23, and Table 27, page 23 (SAR 74570).
- Added 060 devices in Table 277, page 107, Table 278, page 108, and Table 279, page 108 (SAR 57898).
- Updated duty cycle parameter of crystal in Table 280, page 109 and Table 281, page 109 (SAR 57898).
- Added 32 KHz mode PLL acquisition time in Table 282, page 110 (SAR 68281).
- Updated Table 293, page 119 for 060 devices (SAR 57828).
- Updated Table 297, page 122 for CID value (SAR 70878).

1.4 Revision 8.0

The following is a summary of the changes in revision 8.0 of this document.

- Updated Table 11, page 12 (SAR 69218).
- Updated Table 12, page 13 (SAR 69218).
- Updated Table 283, page 111 (SAR 69000).

1.5 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Updated Table 1, page 4(SAR 68620).

1.6 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- Updated Table 5, page 7 (SAR 65949).
- Updated Table 9, page 10 (SAR 62995).
- Updated Table 123, page 47 and Table 133, page 49 (SAR 67210).
- Added Embedded NVM (eNVM) Characteristics, page 104 (SAR 52509).
- Updated Table 277, page 107 (SAR 64855).
- Updated Table 282, page 110 (SAR 65958 and SAR 56666).
- Added DDR Memory Interface Characteristics, page 120 (SAR 66223).
- Added SFP Transceiver Characteristics, page 120 (SAR 63105).
- Updated Table 302, page 123 and Table 309, page 129 (SAR 66314).

1.7 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Updated Table 1, page 4.
- Updated Table 4, page 6 for T_J symbol information.
- Updated Table 5, page 7 (SAR 63109).
- Updated Table 9, page 10.
- Updated Table 282, page 110 (SAR 62012).
- Added Table 290, page 116 (SAR 64100).
- Added Table 306, page 128, Table 307, page 128 (SAR 50424).

1.8 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document.

- Updated Table 1, page 4. Changed the Status of 090 devices to "Production" (SAR 62750).
- Updated Figure 10, page 70. Removed inverter bubble from DDR_IN latch (SAR 61418).
- Updated SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 62836).

The following table lists the embedded operating flash limits.

Table 6 • Embedded Operating Flash Limits

| Product Grade | Element | Programming Temperature | Maximum Operating Temperature | Programming Cycles | Retention (Biased/Unbiased) |
|---------------|----------------|--|--|---|-----------------------------|
| Commercial | Embedded flash | Min T _J = 0 °C Max T _J = 85 °C | Min T _J = 0 °C Max T _J = 85 °C | < 1000 cycles per page, up to two million cycles per eNVM array | 20 years |
| | | | | < 10000 cycles per page, up to 20 million cycles per eNVM array | 10 years |
| Industrial | Embedded flash | Min T _J = -40 °C Max T _J = 100 °C | Min T _J = -40 °C Max T _J = 100 °C | < 1000 cycles per page, up to two million cycles per eNVM array | 20 years |
| | | | | < 10000 cycles per page, up to 20 million cycles per eNVM array | 10 years |

Note: If your product qualification requires accelerated programming cycles, see *Microsemi SoC Products Quality and Reliability Report* about recommended methodologies.

Table 7 • Device Storage Temperature and Retention

| Product Grade | Storage Temperature (T _{stg}) | Retention |
|---------------|--|-----------|
| Commercial | Min T _J = 0 °C Max T _J = 85 °C | 20 years |
| Industrial | Min T _J = -40 °C Max T _J = 100 °C | 20 years |

Table 8 • High Temperature Data Retention (HTR) Lifetime

| T _J (C) | HTR Lifetime ¹ (yrs) |
|--------------------|---------------------------------|
| 90 | 20.5 |
| 95 | 20.5 |
| 100 | 20.5 |
| 105 | 17.0 |
| 110 | 15.0 |
| 115 | 13.0 |
| 120 | 11.5 |
| 125 | 10.0 |
| 130 | 8.0 |
| 135 | 6.0 |
| 140 | 4.5 |
| 145 | 3.0 |
| 150 | 1.5 |

1. HTR Lifetime is the period during which a verify failure is not expected due to flash leakage.

Table 17 • Timing Model Parameters (continued)

| Index | Symbol | Description | -1 | Unit | For More Information |
|-------|-------------|---|-------|------|------------------------|
| F | T_{DP} | Propagation delay of an OR gate | 0.179 | ns | See Table 223, page 76 |
| G | T_{DP} | Propagation delay of an LVDS transmitter | 2.136 | ns | See Table 169, page 57 |
| H | T_{DP} | Propagation delay of a three-input XOR Gate | 0.241 | ns | See Table 223, page 76 |
| I | T_{DP} | Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 16 mA on the MSIO bank | 2.412 | ns | See Table 46, page 27 |
| J | T_{DP} | Propagation delay of a two-input NAND gate | 0.179 | ns | See Table 223, page 76 |
| K | T_{DP} | Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 8 mA on the MSIO bank | 2.309 | ns | See Table 46, page 27 |
| L | T_{CLKQ} | Clock-to-Q of the data register | 0.108 | ns | See Table 224, page 77 |
| | T_{SUD} | Setup time of the data register | 0.254 | ns | See Table 224, page 77 |
| M | T_{DP} | Propagation delay of a two-input AND gate | 0.179 | ns | See Table 223, page 76 |
| N | T_{OCLKQ} | Clock-to-Q of the output data register | 0.263 | ns | See Table 220, page 69 |
| | T_{OSUD} | Setup time of the output data register | 0.19 | ns | See Table 220, page 69 |
| O | T_{DP} | Propagation delay of SSTL2, Class I transmitter on the MSIO bank | 2.055 | ns | See Table 114, page 45 |
| P | T_{DP} | Propagation delay of LVCMOS 1.5 V transmitter, drive strength of 12 mA, fast slew on the DDRIO bank | 3.316 | ns | See Table 70, page 34 |

2.3.5 User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the I/Os section of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

2.3.5.1 Input Buffer and AC Loading

The following figure shows the input buffer and AC loading.

Figure 3 • Input Buffer AC Loading

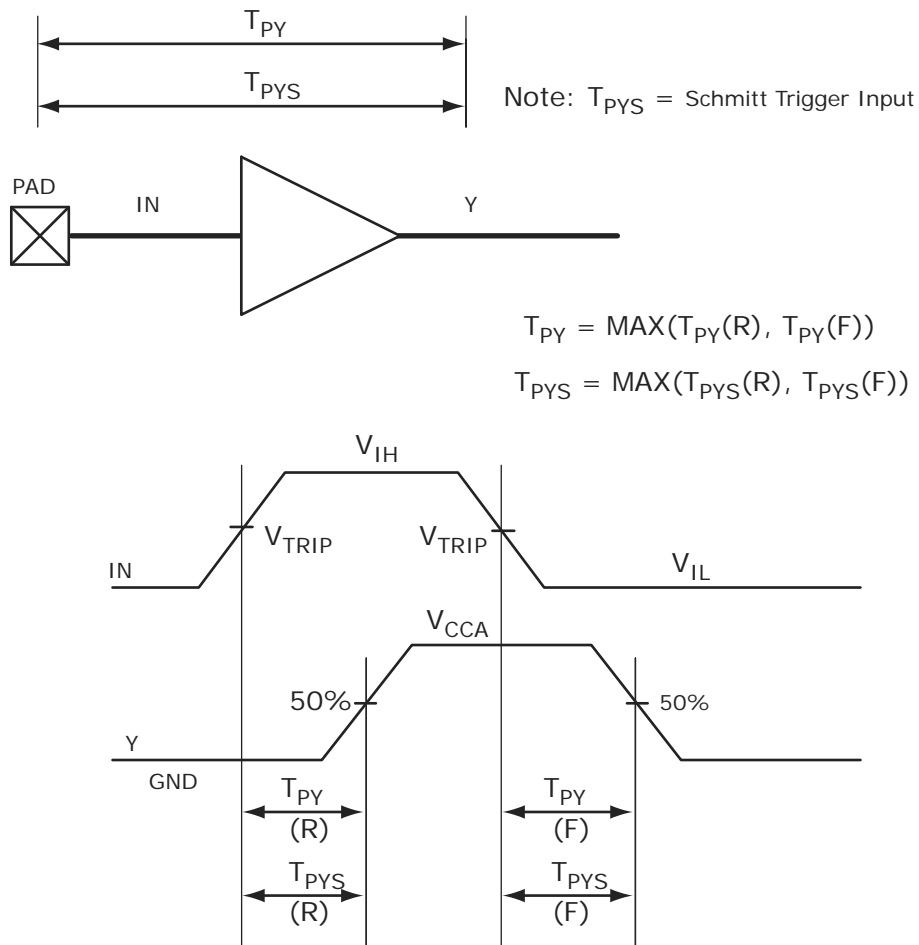


Table 46 • LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)
(continued)

| Output Drive Selection | Slew Control | T_{DP} | | T_{ZL} | | T_{ZH} | | T_{HZ}^1 | | T_{LZ}^1 | | Unit |
|------------------------|--------------|----------|-------|----------|-------|----------|-------|------------|-------|------------|-------|------|
| | | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | |
| 4 mA | Slow | 3.095 | 3.641 | 2.705 | 3.182 | 3.088 | 3.633 | 4.738 | 5.575 | 4.348 | 5.116 | ns |
| | Medium | 2.825 | 3.324 | 2.488 | 2.927 | 2.823 | 3.321 | 4.492 | 5.285 | 4.063 | 4.781 | ns |
| | Medium fast | 2.701 | 3.178 | 2.384 | 2.804 | 2.698 | 3.173 | 4.364 | 5.135 | 3.945 | 4.642 | ns |
| | Fast | 2.69 | 3.165 | 2.377 | 2.796 | 2.687 | 3.161 | 4.359 | 5.129 | 3.94 | 4.636 | ns |
| 6 mA | Slow | 2.919 | 3.434 | 2.491 | 2.93 | 2.902 | 3.414 | 5.085 | 5.983 | 4.674 | 5.5 | ns |
| | Medium | 2.65 | 3.118 | 2.279 | 2.681 | 2.642 | 3.108 | 4.845 | 5.701 | 4.375 | 5.148 | ns |
| | Medium fast | 2.529 | 2.975 | 2.176 | 2.56 | 2.521 | 2.965 | 4.724 | 5.558 | 4.259 | 5.011 | ns |
| | Fast | 2.516 | 2.96 | 2.168 | 2.551 | 2.508 | 2.95 | 4.717 | 5.55 | 4.251 | 5.002 | ns |
| 8 mA | Slow | 2.863 | 3.368 | 2.427 | 2.855 | 2.844 | 3.346 | 5.196 | 6.114 | 4.769 | 5.612 | ns |
| | Medium | 2.599 | 3.058 | 2.217 | 2.608 | 2.59 | 3.047 | 4.952 | 5.827 | 4.471 | 5.261 | ns |
| | Medium fast | 2.483 | 2.921 | 2.114 | 2.487 | 2.473 | 2.91 | 4.832 | 5.685 | 4.364 | 5.134 | ns |
| | Fast | 2.467 | 2.902 | 2.106 | 2.478 | 2.457 | 2.89 | 4.826 | 5.678 | 4.348 | 5.116 | ns |
| 12 mA | Slow | 2.747 | 3.232 | 2.296 | 2.701 | 2.724 | 3.204 | 5.39 | 6.342 | 4.938 | 5.81 | ns |
| | Medium | 2.493 | 2.934 | 2.102 | 2.473 | 2.483 | 2.921 | 5.166 | 6.078 | 4.65 | 5.471 | ns |
| | Medium fast | 2.382 | 2.803 | 2.006 | 2.36 | 2.371 | 2.789 | 5.067 | 5.962 | 4.546 | 5.349 | ns |
| | Fast | 2.369 | 2.787 | 1.999 | 2.352 | 2.357 | 2.773 | 5.063 | 5.958 | 4.538 | 5.339 | ns |
| 16 mA | Slow | 2.677 | 3.149 | 2.213 | 2.604 | 2.649 | 3.116 | 5.575 | 6.56 | 5.08 | 5.977 | ns |
| | Medium | 2.432 | 2.862 | 2.028 | 2.386 | 2.421 | 2.848 | 5.372 | 6.32 | 4.801 | 5.649 | ns |
| | Medium fast | 2.324 | 2.734 | 1.937 | 2.278 | 2.311 | 2.718 | 5.297 | 6.233 | 4.7 | 5.531 | ns |
| | Fast | 2.313 | 2.721 | 1.929 | 2.269 | 2.3 | 2.706 | 5.296 | 6.231 | 4.699 | 5.529 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 47 • LVCMOS 2.5 V Transmitter Characteristics for MSIO Bank (Output and Tristate Buffers)

| Output Drive Selection | Slew Control | T_{DP} | | T_{ZL} | | T_{ZH} | | T_{HZ}^1 | | T_{LZ}^1 | | Unit |
|------------------------|--------------|----------|-------|----------|-------|----------|-------|------------|-------|------------|-------|------|
| | | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | |
| 2 mA | Slow | 3.48 | 4.095 | 3.855 | 4.534 | 3.785 | 4.453 | 2.12 | 2.494 | 3.45 | 4.059 | ns |
| 4 mA | Slow | 2.583 | 3.039 | 3.042 | 3.579 | 3.138 | 3.691 | 4.143 | 4.874 | 4.687 | 5.513 | ns |
| 6 mA | Slow | 2.392 | 2.815 | 2.669 | 3.139 | 2.82 | 3.317 | 4.909 | 5.775 | 5.083 | 5.98 | ns |
| 8 mA | Slow | 2.309 | 2.717 | 2.565 | 3.017 | 2.74 | 3.223 | 5.812 | 6.837 | 5.523 | 6.497 | ns |
| 12 mA | Slow | 2.333 | 2.745 | 2.437 | 2.867 | 2.626 | 3.089 | 6.131 | 7.213 | 5.712 | 6.72 | ns |
| 16 mA | Slow | 2.412 | 2.838 | 2.335 | 2.747 | 2.533 | 2.979 | 6.54 | 7.694 | 6.007 | 7.067 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 95 • HSTL DC Output Voltage Specification Applicable to DDRIO I/O Bank Only

| Parameter | Symbol | Min | Max | Unit |
|---|----------------------|-----------------|-----|------|
| HSTL Class I | | | | |
| DC output logic high | V_{OH} | $V_{DDI} - 0.4$ | | V |
| DC output logic low | V_{OL} | | 0.4 | V |
| Output minimum source DC current (MSIO and DDRIO I/O banks) | I_{OH} at V_{OH} | -8.0 | | mA |
| Output minimum sink current (MSIO and DDRIO I/O banks) | I_{OL} at V_{OL} | 8.0 | | mA |
| HSTL Class II | | | | |
| DC output logic high | V_{OH} | $V_{DDI} - 0.4$ | | V |
| DC output logic low | V_{OL} | | 0.4 | V |
| Output minimum source DC current | I_{OH} at V_{OH} | -16.0 | | mA |
| Output minimum sink current | I_{OL} at V_{OL} | 16.0 | | mA |

Table 96 • HSTL DC Differential Voltage Specification

| Parameter | Symbol | Min | Unit |
|-------------------------------|---------------|-----|------|
| DC input differential voltage | V_{ID} (DC) | 0.2 | V |

Table 97 • HSTL AC Differential Voltage Specifications

| Parameter | Symbol | Min | Max | Unit |
|-------------------------------------|------------|------|-----|------|
| AC input differential voltage | V_{DIFF} | 0.4 | | V |
| AC differential cross point voltage | V_x | 0.68 | 0.9 | V |

Table 98 • HSTL Minimum and Maximum AC Switching Speed

| Parameter | Symbol | Max | Unit | Conditions |
|-------------------|-----------|-----|------|--------------------------------------|
| Maximum data rate | D_{MAX} | 400 | Mbps | AC loading: per JEDEC specifications |

Table 99 • HSTL Impedance Specification

| Parameter | Symbol | Typ | Unit | Conditions |
|---|-----------|------------|----------|-------------------------------------|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | R_{REF} | 25.5, 47.8 | Ω | Reference resistance = 191 Ω |
| Effective impedance value (ODT for DDRIO I/O bank only) | R_{TT} | 47.8 | Ω | Reference resistance = 191 Ω |

2.3.6.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 103 • DDR1/SSTL2 DC Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|-------------------------|-----------|-------|-------|-------|------|
| Supply voltage | V_{DDI} | 2.375 | 2.5 | 2.625 | V |
| Termination voltage | V_{TT} | 1.164 | 1.250 | 1.339 | V |
| Input reference voltage | V_{REF} | 1.164 | 1.250 | 1.339 | V |

Table 104 • DDR1/SSTL2 DC Input Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---------------------------------|---------------|------------------|------------------|------|
| DC input logic high | V_{IH} (DC) | $V_{REF} + 0.15$ | 2.625 | V |
| DC input logic low | V_{IL} (DC) | -0.3 | $V_{REF} - 0.15$ | V |
| Input current high ¹ | I_{IH} (DC) | | | |
| Input current low ¹ | I_{IL} (DC) | | | |

1. See Table 24, page 22.

Table 105 • DDR1/SSTL2 DC Output Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---|----------------------|------------------|------------------|------|
| SSTL2 Class I (DDR Reduced Drive) | | | | |
| DC output logic high | V_{OH} | $V_{TT} + 0.608$ | | V |
| DC output logic low | V_{OL} | | $V_{TT} - 0.608$ | V |
| Output minimum source DC current | I_{OH} at V_{OH} | 8.1 | | mA |
| Output minimum sink current | I_{OL} at V_{OL} | -8.1 | | mA |
| SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Bank Only | | | | |
| DC output logic high | V_{OH} | $V_{TT} + 0.81$ | | V |
| DC output logic low | V_{OL} | | $V_{TT} - 0.81$ | V |
| Output minimum source DC current | I_{OH} at V_{OH} | 16.2 | | mA |
| Output minimum sink current | I_{OL} at V_{OL} | -16.2 | | mA |

Table 106 • DDR1/SSTL2 DC Differential Voltage Specification

| Parameter | Symbol | Min | Unit |
|-------------------------------|---------------|-----|------|
| DC input differential voltage | V_{ID} (DC) | 0.3 | V |

Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers) (continued)

| | | | | | | | | | | | | |
|-------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|----|
| | medium | 3.246 | 3.819 | 2.686 | 3.16 | 3.236 | 3.807 | 5.542 | 6.52 | 4.936 | 5.807 | ns |
| | medium_fast | 3.066 | 3.607 | 2.525 | 2.971 | 3.054 | 3.593 | 5.405 | 6.359 | 4.811 | 5.66 | ns |
| | fast | 3.046 | 3.584 | 2.513 | 2.957 | 3.034 | 3.57 | 5.401 | 6.353 | 4.803 | 5.651 | ns |
| 10 mA | slow | 3.498 | 4.115 | 2.878 | 3.386 | 3.481 | 4.096 | 6.046 | 7.113 | 5.444 | 6.404 | ns |
| | medium | 3.138 | 3.692 | 2.569 | 3.023 | 3.126 | 3.678 | 5.782 | 6.803 | 5.129 | 6.034 | ns |
| | medium_fast | 2.966 | 3.489 | 2.414 | 2.841 | 2.951 | 3.472 | 5.666 | 6.665 | 5.013 | 5.897 | ns |
| | fast | 2.945 | 3.464 | 2.401 | 2.826 | 2.93 | 3.448 | 5.659 | 6.658 | 5.003 | 5.886 | ns |
| 12 mA | slow | 3.417 | 4.02 | 2.807 | 3.303 | 3.401 | 4.002 | 6.083 | 7.156 | 5.464 | 6.428 | ns |
| | medium | 3.076 | 3.618 | 2.519 | 2.964 | 3.063 | 3.604 | 5.828 | 6.856 | 5.176 | 6.089 | ns |
| | medium_fast | 2.913 | 3.427 | 2.376 | 2.795 | 2.898 | 3.41 | 5.725 | 6.736 | 5.072 | 5.966 | ns |
| | fast | 2.894 | 3.405 | 2.362 | 2.78 | 2.879 | 3.388 | 5.715 | 6.724 | 5.064 | 5.957 | ns |
| 16 mA | slow | 3.366 | 3.96 | 2.751 | 3.237 | 3.348 | 3.939 | 6.226 | 7.324 | 5.576 | 6.56 | ns |
| | medium | 3.03 | 3.565 | 2.47 | 2.906 | 3.017 | 3.55 | 5.981 | 7.036 | 5.282 | 6.214 | ns |
| | medium_fast | 2.87 | 3.377 | 2.328 | 2.739 | 2.854 | 3.358 | 5.895 | 6.935 | 5.18 | 6.094 | ns |
| | fast | 2.853 | 3.357 | 2.314 | 2.723 | 2.837 | 3.338 | 5.889 | 6.929 | 5.177 | 6.09 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO management).

2.3.7 Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

2.3.7.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

Minimum and Maximum Input and Output Levels

Table 160 • LVDS Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|----------------|-----------|-------|-----|-------|------|-------------|
| Supply voltage | V_{DDI} | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| Supply voltage | V_{DDI} | 3.15 | 3.3 | 3.45 | V | 3.3 V range |

Table 161 • LVDS DC Input Voltage Specification

| Parameter | Symbol | Min | Max | Unit | Conditions |
|---------------------------------|---------------|-----|-------|------|-------------|
| DC Input voltage | V_I | 0 | 2.925 | V | 2.5 V range |
| DC input voltage | V_I | 0 | 3.45 | V | 3.3 V range |
| Input current high ¹ | I_{IH} (DC) | | | | |
| Input current low ¹ | I_{IL} (DC) | | | | |

1. See Table 24, page 22.

Table 168 • LVDS25 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

| On-Die Termination (ODT) | T_{PY} | | Unit |
|--------------------------|----------|-------|------|
| | -1 | -Std | |
| None | 2.554 | 3.004 | ns |
| 100 | 2.549 | 2.999 | ns |

Table 169 • LVDS25 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

| T_{DP} | | T_{ZL} | | T_{ZH} | | T_{HZ} | | T_{LZ} | | Unit |
|----------|-------|----------|-------|----------|-------|----------|------|----------|-------|------|
| -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | |
| 2.136 | 2.513 | 2.416 | 2.842 | 2.402 | 2.825 | 2.423 | 2.85 | 2.409 | 2.833 | ns |

Table 170 • LVDS25 Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)

| | T_{DP} | | T_{ZL} | | T_{ZH} | | T_{HZ} | | T_{LZ} | | Unit |
|------------------|----------|-------|----------|-------|----------|-------|----------|-------|----------|-------|------|
| | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | |
| No pre-emphasis | 1.61 | 1.893 | 1.749 | 2.058 | 1.735 | 2.041 | 1.897 | 2.231 | 1.866 | 2.195 | ns |
| Min pre-emphasis | 1.527 | 1.796 | 1.757 | 2.067 | 1.744 | 2.052 | 1.905 | 2.241 | 1.876 | 2.207 | ns |
| Med pre-emphasis | 1.496 | 1.76 | 1.765 | 2.077 | 1.751 | 2.06 | 1.914 | 2.252 | 1.884 | 2.216 | ns |

LVDS33 AC Switching Characteristics
Table 171 • LVDS33 Receiver Characteristics for MSIO I/O Bank (Input Buffers)

| On Die Termination (ODT) | T_{PY} | | Unit |
|--------------------------|----------|-------|------|
| | -1 | -Std | |
| None | 2.572 | 3.025 | ns |
| 100 | 2.569 | 3.023 | ns |

Table 172 • LVDS33 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

| T_{DP} | | T_{ZL} | | T_{ZH} | | T_{HZ} | | T_{LZ} | | Unit |
|----------|-------|----------|------|----------|-------|----------|-------|----------|-------|------|
| -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | |
| 1.942 | 2.284 | 1.98 | 2.33 | 1.97 | 2.318 | 1.953 | 2.298 | 1.96 | 2.307 | ns |

Table 191 • M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)

| On-Die Termination (ODT) | T _{PY} | | Unit |
|--------------------------|-----------------|-------|------|
| | -1 | -Std | |
| None | 2.495 | 2.934 | ns |
| 100 | 2.495 | 2.935 | ns |

Table 192 • M-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)

| T _{DP} | | T _{ZL} | | T _{ZH} | | T _{HZ} | | T _{LZ} | | Unit |
|-----------------|-------|-----------------|-------|-----------------|-------|-----------------|-------|-----------------|------|------|
| -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | |
| 2.258 | 2.656 | 2.348 | 2.762 | 2.334 | 2.746 | 2.123 | 2.497 | 2.125 | 2.5 | ns |

2.3.7.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

Mini-LVDS Minimum and Maximum Input and Output Levels

Table 193 • Mini-LVDS Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------|------------------|-------|-----|-------|------|
| Supply voltage | V _{DDI} | 2.375 | 2.5 | 2.625 | V |

Table 194 • Mini-LVDS DC Input Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|------------------|----------------|-----|-------|------|
| DC Input voltage | V _I | 0 | 2.925 | V |

Table 195 • Mini-LVDS DC Output Voltage Specification

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------------|-----------------|------|-------|------|------|
| DC output logic high | V _{OH} | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | V _{OL} | 0.9 | 1.075 | 1.25 | V |

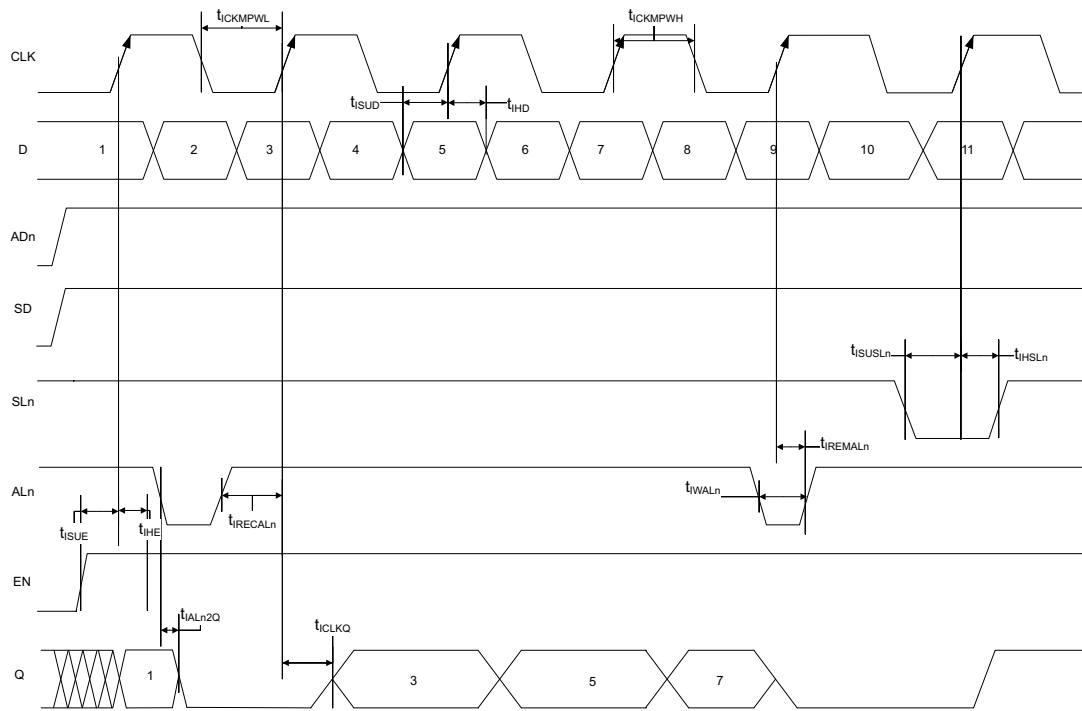
Table 196 • Mini-LVDS DC Differential Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|-----------------------------------|------------------|-----|-----|------|
| Differential output voltage swing | V _{OD} | 300 | 600 | mV |
| Output common mode voltage | V _{OCM} | 1 | 1.4 | V |
| Input common mode voltage | V _{ICM} | 0.3 | 1.2 | V |
| Input differential voltage | V _{ID} | 100 | 600 | mV |

Table 197 • Mini-LVDS Minimum and Maximum AC Switching Speed

| Parameter | Symbol | Max | Unit | Conditions |
|--|------------------|-----|------|--|
| Maximum data rate (for MSIO I/O bank) | D _{MAX} | 520 | Mbps | AC loading: 2 pF / 100 Ω differential load |
| Maximum data rate (for MSIOD I/O bank) | D _{MAX} | 700 | Mbps | AC loading: 2 pF / 100 Ω differential load |

Figure 7 • I/O Register Input Timing Diagram



The following table lists the RAM1K18 – two-port mode for depth × width configuration 512 × 36 in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 236 • RAM1K18 – Two-Port Mode for Depth × Width Configuration 512 × 36

| Parameter | Symbol | –1 | | –Std | | Unit |
|--|-----------------|--------|-------|--------|-------|------|
| | | Min | Max | Min | Max | |
| Clock period | T_{CY} | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | T_{PLCY} | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | T_{CLK2Q} | | 0.334 | | 0.393 | ns |
| Read access time without pipeline register | | | 2.25 | | 2.647 | ns |
| Address setup time | T_{ADDRSU} | 0.313 | | 0.368 | | ns |
| Address hold time | T_{ADDRHD} | 0.274 | | 0.322 | | ns |
| Data setup time | T_{DSU} | 0.337 | | 0.396 | | ns |
| Data hold time | T_{DHD} | 0.111 | | 0.13 | | ns |
| Block select setup time | T_{BLKSU} | 0.207 | | 0.244 | | ns |
| Block select hold time | T_{BLKHD} | 0.201 | | 0.237 | | ns |
| Block select to out disable time (when pipelined register is disabled) | T_{BLK2Q} | | 2.25 | | 2.647 | ns |
| Block select minimum pulse width | T_{BLKMPW} | 0.186 | | 0.219 | | ns |
| Read enable setup time | T_{RDESU} | 0.449 | | 0.528 | | ns |
| Read enable hold time | T_{RDEHD} | 0.167 | | 0.197 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | T_{R2Q} | | 1.506 | | 1.772 | ns |
| Asynchronous reset removal time | T_{RSTREM} | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | T_{RSTREC} | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | T_{RSTMPW} | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | T_{SRSTSU} | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | T_{SRSTHD} | 0.036 | | 0.043 | | ns |
| Write enable setup time | T_{WESU} | 0.39 | | 0.458 | | ns |
| Write enable hold time | T_{WEHD} | 0.242 | | 0.285 | | ns |
| Maximum frequency | F_{MAX} | | 400 | | 340 | MHz |

Table 237 • μ SRAM (RAM64x18) in 64 × 18 Mode (continued)

| Parameter | Symbol | -1 | | -Std | | Unit |
|--------------------------|---------------|--------|-----|-------|-----|------|
| | | Min | Max | Min | Max | |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.128 | | 0.15 | | ns |
| Write enable setup time | T_{WECSU} | 0.397 | | 0.467 | | ns |
| Write enable hold time | T_{WECHD} | -0.026 | | -0.03 | | ns |
| Maximum frequency | F_{MAX} | | 250 | | 250 | MHz |

The following table lists the μ SRAM in 64 × 16 mode in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 238 • μ SRAM (RAM64x16) in 64 × 16 Mode

| Parameter | Symbol | -1 | | -Std | | Unit |
|---|-----------------|--------|--------|--------|--------|-------|
| | | Min | Max | Min | Max | |
| Read clock period | T_{CY} | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | T_{PLCY} | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | T_{CLK2Q} | | 0.266 | | 0.313 | ns |
| Read access time without pipeline register | | | | 1.677 | | 1.973 |
| Read address setup time in synchronous mode | T_{ADDRSU} | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | | 1.856 | | 2.184 | |
| Read address hold time in synchronous mode | T_{ADDRHD} | 0.091 | | 0.107 | | ns |
| Read address hold time in asynchronous mode | | | -0.778 | | -0.915 | |
| Read enable setup time | T_{RDENSU} | 0.278 | | 0.327 | | ns |
| Read enable hold time | T_{RDENHD} | 0.057 | | 0.067 | | ns |
| Read block select setup time | T_{BLKSU} | 1.839 | | 2.163 | | ns |
| Read block select hold time | T_{BLKHD} | -0.65 | | -0.765 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | T_{BLK2Q} | | 2.036 | | 2.396 | ns |
| Read asynchronous reset removal time (pipelined clock) | T_{RSTREM} | -0.023 | | -0.027 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | | 0.046 | | 0.054 | |
| Read asynchronous reset recovery time (pipelined clock) | T_{RSTREC} | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | | 0.236 | | 0.278 | |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | T_{R2Q} | | 0.835 | | 0.983 | ns |
| Read synchronous reset setup time | T_{SRSTSU} | 0.271 | | 0.319 | | ns |

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 270 • Math Block with Input Register Used and Output in Bypass Mode

| Parameter | Symbol | -1 | | -Std | | Unit |
|--------------------------------------|-----------------|--------|-------|--------|-------|------|
| | | Min | Max | Min | Max | |
| Input register setup time | T_{MISU} | 0.149 | | 0.176 | | ns |
| Input register hold time | T_{MIHD} | 0.185 | | 0.218 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | 0.08 | | 0.094 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | -0.012 | | -0.014 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | -0.005 | | -0.005 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.088 | | 0.104 | | ns |
| Input register clock to output delay | T_{MICQ} | | 2.52 | | 2.964 | ns |
| CDIN to output delay | $T_{MCDIN2Q}$ | | 1.951 | | 2.295 | ns |

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 271 • Math Block with Input and Output in Bypass Mode

| Parameter | Symbol | -1 | -Std | Unit |
|-----------------------|---------------|-------|-------|------|
| | | Max | Max | |
| Input to output delay | T_{MIQ} | 2.568 | 3.022 | ns |
| CDIN to output delay | $T_{MCDIN2Q}$ | 1.951 | 2.295 | ns |

2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when $V_{DD} = 1.14\text{ V}$, $V_{PPNVM} = V_{PP} = 2.375\text{ V}$.

Table 272 • eNVM Read Performance

| Symbol | Description | Operating Temperature Range | | | | | | Unit |
|---------------|-----------------------------|-----------------------------|------|------------------|------|---------------|------|------|
| | | -1 | -Std | -1 | -Std | -1 | -Std | |
| T_J | Junction temperature range | -55 °C to 125 °C | | -40 °C to 100 °C | | 0 °C to 85 °C | | °C |
| $F_{MAXREAD}$ | eNVM maximum read frequency | 25 | 25 | 25 | 25 | 25 | 25 | MHz |

The following table lists the eNVM page programming in worst-case conditions when $V_{DD} = 1.14\text{ V}$, $V_{PPNVM} = V_{PP} = 2.375\text{ V}$.

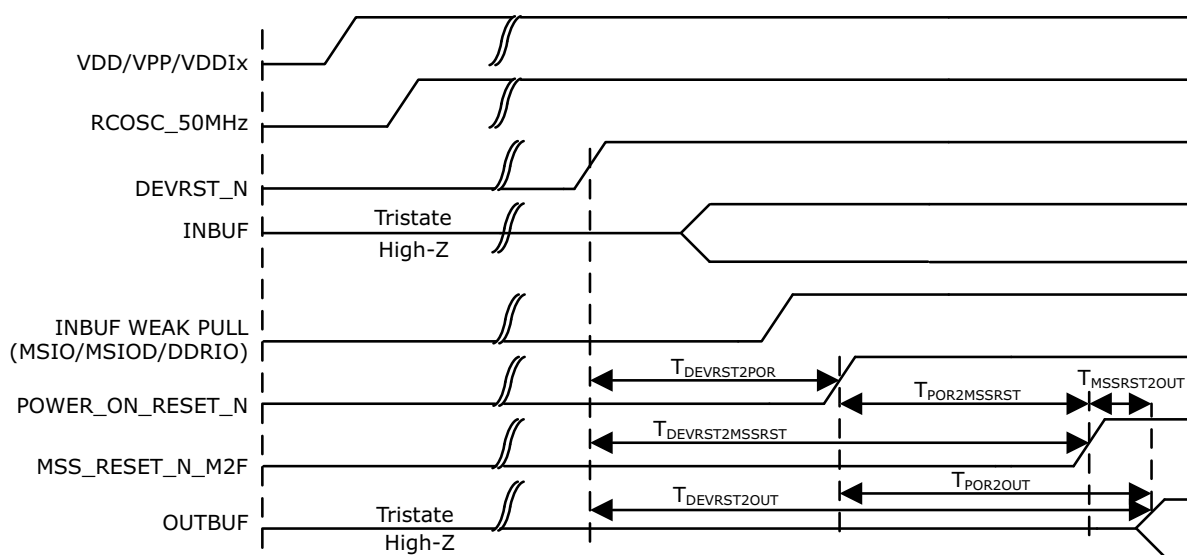
Table 273 • eNVM Page Programming

| Symbol | Description | Operating Temperature Range | | | | | | Unit |
|---------------|----------------------------|-----------------------------|------|------------------|------|---------------|------|------|
| | | -1 | -Std | -1 | -Std | -1 | -Std | |
| T_J | Junction temperature range | -55 °C to 125 °C | | -40 °C to 100 °C | | 0 °C to 85 °C | | °C |
| $T_{PAGEPGM}$ | eNVM page programming time | 40 | 40 | 40 | 40 | 40 | 40 | ms |

Table 291 • DEVRST_N to Functional Times for SmartFusion2 (continued)

| Symbol | From | To | Description | Maximum Power-up to Functional Time for SmartFusion2 (uS) | | | | | | |
|---------------------|----------|-----------------------|---|---|-----|-----|-----|-----|-----|-----|
| | | | | 005 | 010 | 025 | 050 | 060 | 090 | 150 |
| $T_{DEVRST2POR}$ | DEVRST_N | POWER_ON_RESET_N | V_{DD} at its minimum threshold level to fabric | 233 | 289 | 216 | 213 | 237 | 234 | 219 |
| $T_{DEVRST2MSSRST}$ | DEVRST_N | MSS_RESET_N_M2F | V_{DD} at its minimum threshold level to MSS | 702 | 765 | 712 | 688 | 636 | 630 | 866 |
| $T_{DEVRST2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |

Figure 19 • DEVRST_N to Functional Timing Diagram for SmartFusion2



The following table lists the IGLOO2 DEVRST_N to functional times in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 292 • DEVRST_N to Functional Times for IGLOO2

| Symbol | From | To | Description | Maximum Power-up to Functional Time for IGLOO2 (uS) | | | | | | |
|------------------|------------------|-------------------------|---|---|-----|-----|-----|-----|-----|-----|
| | | | | 005 | 010 | 025 | 050 | 060 | 090 | 150 |
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 114 | 116 | 113 | 113 | 115 | 115 | 114 |
| $T_{DEVRST2OUT}$ | DEVRST_N | Output available at I/O | V_{DD} at its minimum threshold level to output | 314 | 353 | 314 | 307 | 343 | 341 | 341 |
| $T_{DEVRST2POR}$ | DEVRST_N | POWER_ON_RESET_N | V_{DD} at its minimum threshold level to fabric | 200 | 238 | 201 | 195 | 230 | 229 | 227 |
| $T_{DEVRST2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |

2.3.31.3 Serial Peripheral Interface (SPI) Characteristics

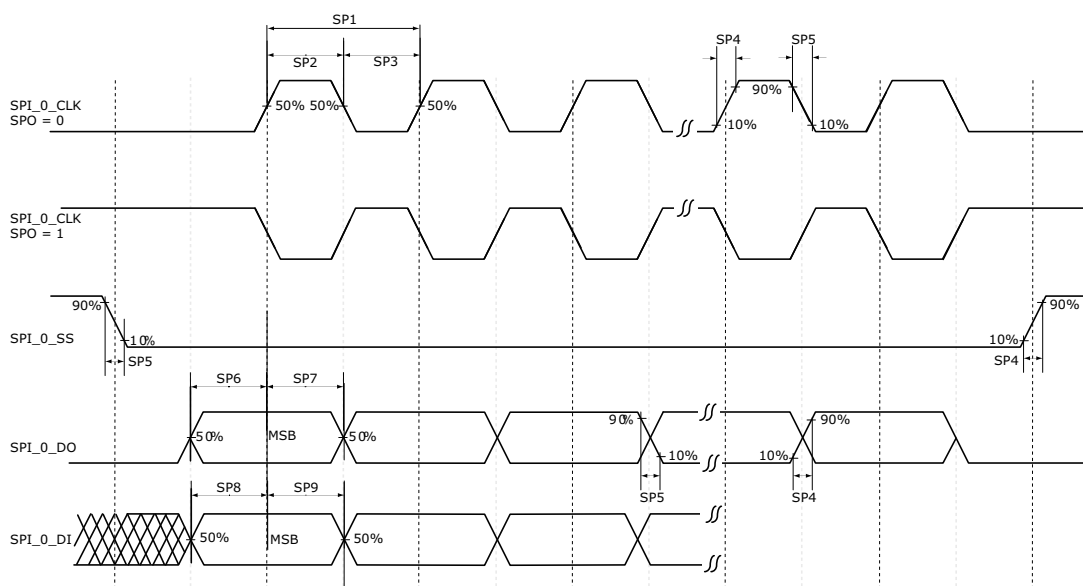
This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, see Figure 22, page 128.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Table 305 • SPI Characteristics for All Devices

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---------|--|-------|------|-----|---------------|---|
| SPIFMAX | Maximum operating frequency of SPI interface | | | 20 | MHz | |
| sp1 | SPI_[0 1]_CLK minimum period | | | | | |
| | SPI_[0 1]_CLK = PCLK/2 | 12 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/4 | 24.1 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/8 | 48.2 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/16 | 0.1 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/32 | 0.19 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/64 | 0.39 | | | μs | |
| sp2 | SPI_[0 1]_CLK minimum pulse width high | | | | | |
| | SPI_[0 1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/16 | 0.05 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/32 | 0.095 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/64 | 0.195 | | | μs | |
| sp3 | SPI_[0 1]_CLK minimum pulse width low | | | | | |
| | SPI_[0 1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/16 | 0.05 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/32 | 0.095 | | | μs | |
| | SPI_[0 1]_CLK = PCLK/64 | 0.195 | | | μs | |
| sp4 | SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) ¹ | | 2.77 | | ns | I/O Configuration: LVCMOS 2.5 V– 8 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C |
| | | | | | | |

Figure 22 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)



2.3.32 CAN Controller Characteristics

The following table lists the CAN controller characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 306 • CAN Controller Characteristics

| Parameter | Description | -1 | -Std | Unit |
|-------------------------|--|------|------|------|
| FCANREFCLK ¹ | Internally sourced CAN reference clock frequency | 160 | 136 | MHz |
| BAUDCANMAX | Maximum CAN performance baud rate | 1 | 1 | Mbps |
| BAUDCANMIN | Minimum CAN performance baud rate | 0.05 | 0.05 | Mbps |

1. PCLK to CAN controller must be a multiple of 8 MHz.

2.3.33 USB Characteristics

The following table lists the USB characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 307 • USB Characteristics

| Parameter | Description | -1 | -Std | Unit |
|------------|--|-------|-------|------|
| FUSBREFCLK | Internally sourced USB reference clock frequency | 166 | 142 | MHz |
| TUSBCLK | USB clock period | 16.66 | 16.66 | ns |
| TUSBPD | Clock to USB data propagation delay | 9.0 | 9.0 | ns |
| TUSBSU | Setup time for USB data | 6.0 | 6.0 | ns |
| TUSBHD | Hold time for USB data | 0 | 0 | ns |

Table 310 • SPI Characteristics for All Devices (continued)

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|--------------------------------------|-----------------------------|-----|-----|------|------------|
| SPI master configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6m | SPI_[0 1]_DO setup time ² | (SPI_x_CLK_period/2) – 7.0 | | | ns | |
| sp7m | SPI_[0 1]_DO hold time ² | (SPI_x_CLK_period/2) – 9.5 | | | ns | |
| sp8m | SPI_[0 1]_DI setup time ² | 15 | | | ns | |
| sp9m | SPI_[0 1]_DI hold time ² | –2.5 | | | ns | |
| SPI slave configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6s | SPI_[0 1]_DO setup time ² | (SPI_x_CLK_period/2) – 16.0 | | | ns | |
| sp7s | SPI_[0 1]_DO hold time ² | (SPI_x_CLK_period/2) – 3.5 | | | ns | |
| sp8s | SPI_[0 1]_DI setup time ² | 3 | | | ns | |
| sp9s | SPI_[0 1]_DI hold time ² | 2.5 | | | ns | |

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. For allowable pclk configurations, see the Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

Figure 23 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)

