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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 90K Logic Modules
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	325-TFBGA, FCBGA
Supplier Device Package	325-FCBGA (11x13.5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s090ts-fcsg325i">https://www.e-xfl.com/product-detail/microchip-technology/m2s090ts-fcsg325i</a>

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**Table 34 • LVTTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	1.4	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**Table 35 • LVTTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank**

Output Drive Selection	$V_{OH}$ (V)	$V_{OL}$ (V)	IOH (at $V_{OH}$ ) mA	IOL (at $V_{OL}$ ) mA
2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	$V_{DDI} - 0.4$	0.4	4	4
8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA	$V_{DDI} - 0.4$	0.4	16	16
20 mA	$V_{DDI} - 0.4$	0.4	20	20

**Note:** For a detailed I/V curve, use the corresponding IBIS models:  
[www.microsemi.com/soc/download/ibis/default.aspx](http://www.microsemi.com/soc/download/ibis/default.aspx).

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 3.0\text{ V}$

**Table 36 • LVTTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
	-1	-Std	-1	-Std	
None	2.262	2.663	2.289	2.695	ns

**Table 37 • LVTTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.192	3.755	3.47	4.083	2.969	3.494	1.856	2.183	3.337	3.926	ns
4 mA	Slow	2.331	2.742	2.673	3.145	2.526	2.973	3.034	3.569	4.451	5.236	ns
8 mA	Slow	2.135	2.511	2.33	2.741	2.297	2.703	4.532	5.331	4.825	5.676	ns
12 mA	Slow	2.052	2.414	2.107	2.479	2.162	2.544	5.75	6.764	5.445	6.406	ns
16 mA	Slow	2.062	2.425	2.072	2.438	2.145	2.525	5.993	7.05	5.625	6.618	ns
20 mA	Slow	2.148	2.527	1.999	2.353	2.088	2.458	6.262	7.367	5.876	6.913	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 58 • LVCMOS 1.8 V Transmitter Characteristics for MSIO I/O Bank**

Output Drive Selection	Slew Control	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub> <sup>1</sup>		T <sub>LZ</sub> <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.441	4.047	4.165	4.9	4.413	5.192	4.891	5.755	5.138	6.044	ns
4 mA	Slow	3.218	3.786	3.642	4.284	3.941	4.636	5.665	6.665	5.568	6.551	ns
6 mA	Slow	3.141	3.694	3.501	4.118	3.823	4.498	6.587	7.75	6.032	7.096	ns
8 mA	Slow	3.165	3.723	3.319	3.904	3.654	4.298	6.898	8.115	6.216	7.313	ns
10 mA	Slow	3.202	3.767	3.278	3.857	3.616	4.254	7.25	8.529	6.435	7.571	ns
12 mA	Slow	3.277	3.855	3.175	3.736	3.519	4.139	7.392	8.697	6.538	7.692	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 59 • LVCMOS 1.8 V Transmitter Characteristics for MSIOD I/O Bank**

Output Drive Selection	Slew Control	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub> <sup>1</sup>		T <sub>LZ</sub> <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	2.725	3.206	3.316	3.901	3.484	4.099	5.204	6.123	4.997	5.88	ns
4 mA	Slow	2.242	2.638	2.777	3.267	2.947	3.466	5.729	6.74	5.448	6.41	ns
6 mA	Slow	1.995	2.347	2.466	2.901	2.63	3.094	6.372	7.496	5.987	7.043	ns
8 mA	Slow	2.001	2.354	2.44	2.87	2.6	3.058	6.633	7.804	6.193	7.286	ns
10 mA	Slow	2.025	2.382	2.312	2.719	2.47	2.906	6.94	8.165	6.412	7.544	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.9 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 60 • LVCMOS 1.5 V DC Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>DDI</sub>	1.425	1.5	1.575	V

**Table 61 • LVCMOS 1.5 V DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high for (MSIOD and DDRIO I/O banks)	V <sub>IH</sub> (DC)	0.65 × V <sub>DDI</sub>	1.575	V
DC input logic high (for MSIO I/O bank)	V <sub>IH</sub> (DC)	0.65 × V <sub>DDI</sub>	3.45	V
DC input logic low	V <sub>IL</sub> (DC)	-0.3	0.35 × V <sub>DDI</sub>	V
Input current high <sup>1</sup>	I <sub>IH</sub> (DC)			-
Input current low <sup>1</sup>	I <sub>IL</sub> (DC)			-

1. See Table 24, page 22.

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 1.425\text{ V}$

**Table 67 • LVCMOS 1.5 V Receiver Characteristics for DDRIO I/O Bank with Fixed Codes (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
	-1	-Std	-1	-Std	
None	2.051	2.413	2.086	2.455	ns

**Table 68 • LVCMOS 1.5 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
	-1	-Std	-1	-Std	
None	3.311	3.896	3.285	3.865	ns
50	3.654	4.299	3.623	4.263	ns
75	3.533	4.156	3.501	4.119	ns
150	3.415	4.018	3.388	3.986	ns

**Table 69 • LVCMOS 1.5 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
	-1	-Std	-1	-Std	
None	2.959	3.481	2.93	3.447	ns
50	3.298	3.88	3.268	3.845	ns
75	3.162	3.719	3.128	3.68	ns
150	3.053	3.592	3.021	3.554	ns

**Table 70 • LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	5.122	6.026	4.31	5.07	5.145	6.052	5.258	6.186	4.672	5.496	ns
	Medium	4.58	5.389	3.86	4.54	4.6	5.411	4.977	5.855	4.357	5.126	ns
	Medium fast	4.323	5.086	3.629	4.269	4.341	5.107	4.804	5.652	4.228	4.974	ns
	Fast	4.296	5.054	3.609	4.245	4.314	5.075	4.791	5.636	4.219	4.963	ns
4 mA	Slow	4.449	5.235	3.707	4.361	4.443	5.227	6.058	7.127	5.458	6.421	ns
	Medium	3.961	4.66	3.264	3.839	3.954	4.651	5.778	6.797	5.116	6.018	ns
	Medium fast	3.729	4.387	3.043	3.579	3.72	4.376	5.63	6.624	4.981	5.86	ns
	Fast	3.704	4.358	3.027	3.56	3.695	4.347	5.624	6.617	4.973	5.851	ns

**Table 107 • SSTL2 AC Differential Voltage Specifications**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	$V_{DIFF} (AC)$	0.7		V
AC differential cross point voltage	$V_x (AC)$	$0.5 \times V_{DDI} - 0.2$	$0.5 \times V_{DDI} + 0.2$	V

**Table 108 • SSTL2 Minimum and Maximum AC Switching Speeds**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	$D_{MAX}$	400	Mbps	AC loading: per JEDEC specifications
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	575	Mbps	AC loading: 17pF load
Maximum data rate (for MSIOD I/O bank)	$D_{MAX}$	700	Mbps	AC loading: 3 pF / 50 $\Omega$ load
		510	Mbps	AC loading: 17pF load

**Table 109 • SSTL2 AC Impedance Specifications**

Parameter	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	20, 42	$\Omega$	Reference resistor = 150 $\Omega$

**Table 110 • DDR1/SSTL2 AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	1.25	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Reference resistance for data test path for SSTL2 Class I ( $T_{DP}$ )	$R_{TT\_TEST}$	50	$\Omega$
Reference resistance for data test path for SSTL2 Class II ( $T_{DP}$ )	$R_{TT\_TEST}$	25	$\Omega$
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

**Table 111 • SSTL2 Receiver Characteristics for DDRIO I/O Bank (Input Buffers)**

	On-Die Termination (ODT)	$T_{PY}$		Unit
		-1	-Std	
Pseudo differential	None	1.549	1.821	ns
True differential	None	1.589	1.87	ns



**Table 118 • DDR1/SSTL2 Class II Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.29	2.693	1.988	2.338	1.978	2.326	1.989	2.34	1.979	2.328	ns
Differential	2.418	2.846	2.304	2.711	2.297	2.702	2.131	2.506	2.124	2.499	ns

**2.3.6.4 Stub-Series Terminated Logic 1.8 V (SSTL18)**

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification****Table 119 • SSTL18 DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	1.71	1.8	1.89	V
Termination voltage	$V_{TT}$	0.838	0.900	0.964	V
Input reference voltage	$V_{REF}$	0.838	0.900	0.964	V

**Table 120 • SSTL18 DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}$ (DC)	$V_{REF} + 0.125$	1.89	V
DC input logic low	$V_{IL}$ (DC)	-0.3	$V_{REF} - 0.125$	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 121 • SSTL18 DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
<b>SSTL18 Class I (DDR2 Reduced Drive)</b>				
DC output logic high	$V_{OH}$	$V_{TT} + 0.603$		V
DC output logic low	$V_{OL}$		$V_{TT} - 0.603$	V
Output minimum source DC current (DDRIO I/O bank only)	$I_{OH}$ at $V_{OH}$	6.5		mA
Output minimum sink current (DDRIO I/O bank only)	$I_{OL}$ at $V_{OL}$	-6.5		mA
<b>SSTL18 Class II (DDR2 Full Drive)<sup>1</sup></b>				
DC output logic high	$V_{OH}$	$V_{TT} + 0.603$		V
DC output logic low	$V_{OL}$		$V_{TT} - 0.603$	V
Output minimum source DC current (DDRIO I/O bank only)	$I_{OH}$ at $V_{OH}$	13.4		mA
Output minimum sink current (DDRIO I/O bank only)	$I_{OL}$ at $V_{OL}$	-13.4		mA

1. To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.

**Table 131 • SSTL15 DC Output Voltage Specification (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
<b>DDR3/SSTL15 Class I (DDR3 Reduced Drive)</b>				
DC output logic high	$V_{OH}$	$0.8 \times V_{DDI}$		V
DC output logic low	$V_{OL}$		$0.2 \times V_{DDI}$	V
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	6.5		mA
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-6.5		mA
<b>DDR3/SSTL15 Class II (DDR3 Full Drive)</b>				
DC output logic high	$V_{OH}$	$0.8 \times V_{DDI}$		V
DC output logic low	$V_{OL}$		$0.2 \times V_{DDI}$	V
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	7.6		mA
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-7.6		mA

**Table 132 • SSTL15 DC Differential Voltage Specification (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Unit
DC input differential voltage	$V_{ID}$	0.2	V

**Note:** To meet JEDEC electrical compliance, use DDR3 full drive transmitter.

**Table 133 • SSTL15 AC SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	$V_{DIFF}$ (AC)	0.3		V
AC differential cross point voltage	$V_x$ (AC)	$0.5 \times V_{DDI} - 0.150$	$0.5 \times V_{DDI} + 0.150$	V

**Table 134 • SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	$D_{MAX}$	667	Mbps	AC loading: per JEDEC specifications

**Table 135 • SSTL15 AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	$R_{REF}$	34, 40	$\Omega$	Reference resistor = 240 $\Omega$
Effective impedance value (ODT)	$R_{TT}$	20, 30, 40, 60, 120	$\Omega$	Reference resistor = 240 $\Omega$

**Table 136 • SSTL15 AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	0.75	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Reference resistance for data test path for SSTL15 Class I ( $T_{DP}$ )	$RTT\_TEST$	50	$\Omega$
Reference resistance for data test path for SSTL15 Class II ( $T_{DP}$ )	$RTT\_TEST$	25	$\Omega$
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 1.425\text{ V}$

**Table 137 • DDR3/SSTL15 Receiver Characteristics for DDRIO I/O Bank – with Calibration Only**

	On-Die Termination (ODT)	$T_{PY}$		Unit
		-1	-Std	
Pseudo differential	None	1.605	1.888	ns
	20	1.616	1.901	ns
	30	1.613	1.897	ns
	40	1.611	1.895	ns
	60	1.609	1.893	ns
	120	1.607	1.89	ns
True differential	None	1.623	1.91	ns
	20	1.637	1.926	ns
	30	1.63	1.918	ns
	40	1.626	1.914	ns
	60	1.622	1.91	ns
	120	1.619	1.905	ns

**Table 138 • DDR3/SSTL15 Transmitter Characteristics (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
<b>DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)</b>											
Single-ended	2.533	2.98	2.522	2.967	2.523	2.968	2.427	2.855	2.428	2.856	ns
Differential	2.555	3.005	3.073	3.615	3.073	3.615	2.416	2.843	2.416	2.843	ns
<b>DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)</b>											
Single-ended	2.53	2.977	2.514	2.958	2.516	2.96	2.422	2.849	2.425	2.852	ns
Differential	2.552	3.002	2.591	3.048	2.59	3.047	2.882	3.391	2.881	3.39	ns

**Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers) (continued)**

	medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	medium_fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10 mA	slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	medium_fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12 mA	slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	medium_fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16 mA	slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	medium_fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO management).

### 2.3.7 Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

#### 2.3.7.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

##### Minimum and Maximum Input and Output Levels

**Table 160 • LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V	2.5 V range
Supply voltage	$V_{DDI}$	3.15	3.3	3.45	V	3.3 V range

**Table 161 • LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit	Conditions
DC Input voltage	$V_I$	0	2.925	V	2.5 V range
DC input voltage	$V_I$	0	3.45	V	3.3 V range
Input current high <sup>1</sup>	$I_{IH}$ (DC)				
Input current low <sup>1</sup>	$I_{IL}$ (DC)				

1. See Table 24, page 22.

**Table 198 • Mini-LVDS AC Impedance Specifications**

Parameter	Symbol	Typ	Unit
Termination resistance	$R_T$	100	$\Omega$

**Table 199 • Mini-LVDS AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	Cross point	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$ .

**Table 200 • Mini-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.855	3.359	ns
100	2.85	3.353	ns
None	2.602	3.061	ns
100	2.597	3.055	ns

**Table 201 • Mini-LVDS AC Switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)**

$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.097	2.467	2.308	2.715	2.296	2.701	1.964	2.31	1.949	2.293	ns

**Table 202 • Mini-LVDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
No pre-emphasis	1.614	1.899	1.562	1.837	1.553	1.826	1.593	1.874	1.578	1.856	ns
Min pre-emphasis	1.604	1.887	1.745	2.053	1.731	2.036	1.892	2.225	1.861	2.189	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

### 2.3.10.2 Timing Characteristics

The following table lists the combinatorial cell propagation delays in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

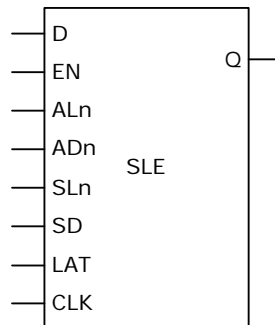
**Table 223 • Combinatorial Cell Propagation Delays**

Combinatorial Cell	Equation	Symbol	-1	-Std	Unit
INV	$Y = !A$	$T_{PD}$	0.1	0.118	ns
AND2	$Y = A \cdot B$	$T_{PD}$	0.164	0.193	ns
NAND2	$Y = !(A \cdot B)$	$T_{PD}$	0.147	0.173	ns
OR2	$Y = A + B$	$T_{PD}$	0.164	0.193	ns
NOR2	$Y = !(A + B)$	$T_{PD}$	0.147	0.173	ns
XOR2	$Y = A \oplus B$	$T_{PD}$	0.164	0.193	ns
XOR3	$Y = A \oplus B \oplus C$	$T_{PD}$	0.225	0.265	ns
AND3	$Y = A \cdot B \cdot C$	$T_{PD}$	0.209	0.246	ns
AND4	$Y = A \cdot B \cdot C \cdot D$	$T_{PD}$	0.287	0.338	ns

### 2.3.10.3 Sequential Module

IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

**Figure 15 • Sequential Module**



The following table lists the RAM1K18 – two-port mode for depth × width configuration 512 × 36 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 236 • RAM1K18 – Two-Port Mode for Depth × Width Configuration 512 × 36**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	$T_{CY}$	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	$T_{PLCY}$	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register	$T_{CLK2Q}$		0.334		0.393	ns
Read access time without pipeline register			2.25		2.647	ns
Address setup time	$T_{ADDRSU}$	0.313		0.368		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.337		0.396		ns
Data hold time	$T_{DHD}$	0.111		0.13		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns
Block select hold time	$T_{BLKHD}$	0.201		0.237		ns
Block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.25		2.647	ns
Block select minimum pulse width	$T_{BLKMPW}$	0.186		0.219		ns
Read enable setup time	$T_{RDESU}$	0.449		0.528		ns
Read enable hold time	$T_{RDEHD}$	0.167		0.197		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	$T_{R2Q}$		1.506		1.772	ns
Asynchronous reset removal time	$T_{RSTREM}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTREC}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	$T_{RSTMPW}$	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTSU}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTHD}$	0.036		0.043		ns
Write enable setup time	$T_{WESU}$	0.39		0.458		ns
Write enable hold time	$T_{WEHD}$	0.242		0.285		ns
Maximum frequency	$F_{MAX}$		400		340	MHz

**Table 239 •  $\mu$ SRAM (RAM128x9) in 128 × 9 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read asynchronous reset removal time (pipelined clock)		-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)	$T_{RSTREM}$	0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)		0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)	$T_{RSTREC}$	0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	$T_{R2Q}$		0.835		0.982	ns
Read synchronous reset setup time	$T_{SRSTSU}$	0.271		0.319		ns
Read synchronous reset hold time	$T_{SRSTHD}$	0.061		0.071		ns
Write clock period	$T_{CCY}$	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	$T_{BLKCSU}$	0.404		0.476		ns
Write block hold time	$T_{BLKCHD}$	0.007		0.008		ns
Write input data setup time	$T_{DINCSU}$	0.115		0.135		ns
Write input data hold time	$T_{DINCHD}$	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.026		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

The following table lists the  $\mu$ SRAM in 128 × 8 mode in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 240 •  $\mu$ SRAM (RAM128x8) in 128 × 8 Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	$T_{CY}$	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	$T_{PLCY}$	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register			0.266		0.313	ns
Read access time without pipeline register	$T_{CLK2Q}$		1.677		1.973	ns
Read address setup time in synchronous mode		0.301		0.354		ns
Read address setup time in asynchronous mode	$T_{ADDRSU}$	1.856		2.184		ns



**Table 240 •  $\mu$ SRAM (RAM128x8) in 128 x 8 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.091		0.107		ns
Read address hold time in asynchronous mode		-0.778		-0.915		ns
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHD}$	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	$T_{RSTREM}$	-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	$T_{RSTREC}$	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	$T_{R2Q}$		0.835		0.982	ns
Read synchronous reset setup time	$T_{SRSTSU}$	0.271		0.319		ns
Read synchronous reset hold time	$T_{SRSTHD}$	0.061		0.071		ns
Write clock period	$T_{CCY}$	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	$T_{BLKCSU}$	0.404		0.476		ns
Write block hold time	$T_{BLKCHD}$	0.007		0.008		ns
Write input data setup time	$T_{DINCSU}$	0.115		0.135		ns
Write input data hold time	$T_{DINCHD}$	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.026		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

## 2.3.20 On-Chip Oscillator

The following tables describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

**Table 280 • Electrical Characteristics of the 50 MHz RC Oscillator**

Parameter	Symbol	Typ	Max	Unit	Condition
Operating frequency	F50RC	50		MHz	
Accuracy	ACC50RC	1	4	%	050 devices
		1	5	%	005, 025, and 060 devices
		1	6.3	%	090 devices
		1	7.1	%	010 and 150 devices
Output duty cycle	CYC50RC	49–51	46.5–53.5	%	
Output jitter (peak to peak)	JIT50RC	Period Jitter			
		200	300	ps	005, 010, 050, and 060 devices
		200	400	ps	150 devices
		300	500	ps	025 and 090 devices
		Cycle-to-Cycle Jitter			
		200	300	ps	005 and 050 devices
		320	420	ps	010, 060, and 150 devices
		320	850	ps	025 and 090 devices
Operating current	IDYN50RC	6.5		mA	

**Table 281 • Electrical Characteristics of the 1 MHz RC Oscillator**

Parameter	Symbol	Typ	Max	Unit	Condition
Operating frequency	F1RC	1		MHz	
Accuracy	ACC1RC	1	3	%	005, 010, 025, and 050 devices
		1	4.5	%	060, and 150 devices
		1	5.6	%	090 devices
Output duty cycle	CYC1RC	49–51	46.5–53.5	%	005, 010, 025, 050, 090 and 150 devices
		49–51	46.0–54.0	%	060 devices
Output jitter (peak to peak)	JIT1RC	Period Jitter			
		10	20	ns	005, 010, 025, and 050 devices
		10	28	ns	060, 090 and 150 devices
		Cycle-to-Cycle Jitter			
		10	20	ns	005, 010, and 050 devices
		10	35	ns	025, 060, and 150 devices
		10	45	ns	090 devices
Operating current	IDYN1RC	0.1		mA	
Startup time	SU1RC	17		μs	050, 090, and 150 devices
		18		μs	005, 010, and 025 devices

## 2.3.24 Power-up to Functional Times

The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 288 • Power-up to Functional Times for SmartFusion2**

Symbol	From	To	Description	Maximum Power-up to Functional Time for SmartFusion2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	647	500	531	483	474	524	647
$T_{POR2MSSRST}$	POWER_ON_RESET_N	MSS_RESE T_N_M2F	Fabric to MSS	644	497	528	480	468	518	641
$T_{MSSRST2OUT}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.6	3.6	3.6	3.4	4.9	4.8	4.8
$T_{VDD2OUT}$	$V_{DD}$	Output available at I/O	$V_{DD}$ at its minimum threshold level to output	3096	2975	3012	2959	2869	2992	3225
$T_{VDD2POR}$	$V_{DD}$	POWER_ON_RESET_N	$V_{DD}$ at its minimum threshold level to fabric	2476	2487	2496	2486	2406	2563	2602
$T_{VDD2MSSRST}$	$V_{DD}$	MSS_RESE T_N_M2F	$V_{DD}$ at its minimum threshold level to MSS	3093	2972	3008	2956	2864	2987	3220
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

**Note:** For more information about power-up times, see [UG0331: SmartFusion2 Microcontroller Subsystem User Guide](#).

### 2.3.31.2 SmartFusion2 Inter-Integrated Circuit (I<sup>2</sup>C) Characteristics

This section describes the DC and switching of the I<sup>2</sup>C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, see [Figure 21](#), page 125.

The following table lists the I<sup>2</sup>C characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$

**Table 303 • I<sup>2</sup>C Characteristics**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input low voltage	$V_{IL}$	-0.3		0.8	V	See <a href="#">Single-Ended I/O Standards</a> , page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTTL 8 mA low drive.
Input high voltage	$V_{IH}$	2		3.45	V	See <a href="#">Single-Ended I/O Standards</a> , page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTTL 8 mA low drive.
Hysteresis of schmitt triggered inputs for $V_{DDI} > 2\text{ V}$	$V_{HYS}$	$0.05 \times V_{DDI}$			V	See <a href="#">Table 28</a> , page 23 for more information.
Input current high	$I_{IL}$			10	$\mu\text{A}$	See <a href="#">Single-Ended I/O Standards</a> , page 24 for more information.
Input current low	$I_{IH}$			10	$\mu\text{A}$	See <a href="#">Single-Ended I/O Standards</a> , page 24 for more information.
Input rise time	$T_{ir}$			1000	ns	Standard mode
				300	ns	Fast mode
Input fall time	$T_{if}$			300	ns	Standard mode
				300	ns	Fast mode
Maximum output voltage low (open drain) at 3 mA sink current for $V_{DDI} > 2\text{ V}$	$V_{OL}$			0.4	V	See <a href="#">Single-Ended I/O Standards</a> , page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTTL 8 mA low drive.
Pin capacitance	$C_{in}$			10	pF	$V_{IN} = 0$ , $f = 1.0\text{ MHz}$
Output fall time from $V_{IHMin}$ to $V_{ILMax}^1$	$t_{OF}^1$		21.04		ns	$V_{IHmin}$ to $V_{ILMax}$ , $C_{LOAD} = 400\text{ pF}$
			5.556		ns	$V_{IHmin}$ to $V_{ILMax}$ , $C_{LOAD} = 100\text{ pF}$
Output rise time from $V_{ILMax}$ to $V_{IHMin}^1$	$t_{OR}^1$		19.887		ns	$V_{ILMax}$ to $V_{IHmin}$ , $C_{LOAD} = 400\text{ pF}$
			5.218		ns	$V_{ILMax}$ to $V_{IHmin}$ , $C_{LOAD} = 100\text{ pF}$
Output buffer maximum pull-down resistance <sup>2,3</sup>	$R_{pull-up}^{2,3}$			50	$\Omega$	
Output buffer maximum pull-up resistance <sup>2,4</sup>	$R_{pull-down}^{2,4}$			131.25	$\Omega$	

**Table 303 • I2C Characteristics (continued)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Maximum data rate	$D_{MAX}$			400	Kbps	Fast mode
				100	Kbps	Standard mode
Pulse width of spikes which must be suppressed by the input filter	$T_{FILT}$		50		ns	Fast mode

1. These values are provided for MSIO Bank–LVTTTL 8 mA Low Drive at 25 °C, typical conditions. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on  $V_{DDIX}$ , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
3.  $R(PULL-DOWN-MAX) = (VOLspec)/IOLspec$ .
4.  $R(PULL-UP-MAX) = (VDDImax-VOHspec)/IOHspec$ .

The following table lists the I<sup>2</sup>C switching characteristics in worst-case industrial conditions when  $T_J = 100\text{ °C}$ ,  $V_{DD} = 1.14\text{ V}$

**Table 304 • I2C Switching Characteristics**

Parameter	Symbol	-1		Unit
		Min	Min	
Low period of I2C_x_SCL	$T_{LOW}$	1	1	PCLK cycles
High period of I2C_x_SCL	$T_{HIGH}$	1	1	PCLK cycles
START hold time	$T_{HD;STA}$	1	1	PCLK cycles
START setup time	$T_{SU;STA}$	1	1	PCLK cycles
DATA hold time	$T_{HD;DAT}$	1	1	PCLK cycles
DATA setup time	$T_{SU;DAT}$	1	1	PCLK cycles
STOP setup time	$T_{SU;STO}$	1	1	PCLK cycles

**Figure 21 • I<sup>2</sup>C Timing Parameter Definition**

