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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 90K Logic Modules
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s090ts-fgg676i">https://www.e-xfl.com/product-detail/microchip-technology/m2s090ts-fgg676i</a>

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The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIO I/O bank at  $V_{OH}/V_{OL}$  Level.

**Table 26 • I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank**

$V_{DDI}$ Domain	R(WEAK PULL-UP) at $V_{OH}$ ( $\Omega$ )		R(WEAK PULL-DOWN) at $V_{OL}$ ( $\Omega$ )	
	Min	Max	Min	Max
3.3 V	9.9K	17.1K	9.98K	17.5K
2.5 V <sup>1,2</sup>	10K	17.6K	10.1K	18.4K
1.8 V <sup>1,2</sup>	10.4K	19.1K	10.4K	20.4K
1.5 V <sup>1,2</sup>	10.7K	20.4K	10.8K	22.2K
1.2 V <sup>1,2</sup>	11.3K	23.2K	11.5K	26.7K

1.  $R(\text{WEAK PULL-DOWN}) = (V_{OLspec})/I(\text{WEAK PULL-DOWN MAX})$ .
2.  $R(\text{WEAK PULL-UP}) = (V_{DDImax} - V_{OHspec})/I(\text{WEAK PULL-UP MIN})$ .

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIOD I/O bank at  $V_{OH}/V_{OL}$  Level.

**Table 27 • I/O Weak Pull-up/Pull-down Resistances for MSIOD I/O Bank**

$V_{DDI}$ Domain	R(WEAK PULL-UP) at $V_{OH}$ ( $\Omega$ )		R(WEAK PULL-DOWN) at $V_{OL}$ ( $\Omega$ )	
	Min	Max	Min	Max
2.5 V <sup>1,2</sup>	9.6K	16.6K	9.5K	16.4K
1.8 V <sup>1,2</sup>	9.7K	17.3K	9.7K	17.1K
1.5 V <sup>1,2</sup>	9.9K	18K	9.8K	17.6K
1.2 V <sup>1,2</sup>	10.3K	19.6K	10K	19.1K

1.  $R(\text{WEAK PULL-DOWN}) = (V_{OLspec})/I(\text{WEAK PULL-DOWN MAX})$ .
2.  $R(\text{WEAK PULL-UP}) = (V_{DDImax} - V_{OHspec})/I(\text{WEAK PULL-UP MIN})$ .

The following table lists the hysteresis voltage value for schmitt trigger mode input buffers.

**Table 28 • Schmitt Trigger Input Hysteresis**

Input Buffer Configuration	Hysteresis Value (Typical, unless otherwise noted)
3.3 V LVTTTL/LVCMOS/ PCI/PCI-X	$0.05 \times V_{DDI}$ (worst-case)
2.5 V LVCMOS	$0.05 \times V_{DDI}$ (worst-case)
1.8 V LVCMOS	$0.1 \times V_{DDI}$ (worst-case)
1.5 V LVCMOS	60 mV
1.2 V LVCMOS	20 mV

### 2.3.5.7 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs that are in compliance with the JEDEC specification JESD8-5A.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 38 • LVCMOS 2.5 V DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V

**Table 39 • LVCMOS 2.5 V DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	$V_{IH}$ (DC)	1.7	2.625	V
DC input logic high (for MSIO I/O bank)	$V_{IH}$ (DC)	1.7	3.45	V
DC input logic low	$V_{IL}$ (DC)	-0.3	0.7	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 40 • LVCMOS 2.5 V DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	$V_{OH}$ <sup>1</sup>	$V_{DDI} - 0.4$	-	V
DC output logic low	$V_{OL}$ <sup>2</sup>		0.4	V

1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

**Table 41 • LVCMOS 2.5 V AC Minimum and Maximum Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	$D_{MAX}$	400	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	410	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	$D_{MAX}$	420	Mbps	AC loading: 17 pF load, maximum drive/slew

**Table 42 • LVCMOS 2.5 V AC Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	Rodt_cal	75, 60, 50, 33, 25, 20	$\Omega$

**Table 72 • LVCMOS 1.5 V Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	2.735	3.218	3.371	3.966	3.618	4.257	6.03	7.095	5.705	6.712	ns
4 mA	Slow	2.426	2.854	2.992	3.521	3.221	3.79	6.738	7.927	6.298	7.41	ns
6 mA	Slow	2.433	2.862	2.81	3.306	3.031	3.566	7.123	8.38	6.596	7.76	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.10 1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-12A.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 73 • LVCMOS 1.2 V DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	1.140	1.2	1.26	V

**Table 74 • LVCMOS 1.2 V DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	$V_{IH} (DC)$	$0.65 \times V_{DDI}$	1.26	V
DC input logic high (for MSIO I/O bank)	$V_{IH} (DC)$	$0.65 \times V_{DDI}$	3.45	V
DC input logic low	$V_{IL} (DC)$	-0.3	$0.35 \times V_{DDI}$	V
Input current high <sup>1</sup>	$I_{IH} (DC)$			
Input current low <sup>1</sup>	$I_{IL} (DC)$			

1. See Table 24, page 22.

**Table 75 • LVCMOS 1.2 V DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	$V_{OH}$	$V_{DDI} \times 0.75$		V
DC output logic low	$V_{OL}$		$V_{DDI} \times 0.25$	V

**Table 76 • LVCMOS 1.2 V Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	$D_{MAX}$	200	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	120	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	$D_{MAX}$	160	Mbps	AC loading: 17 pF load, maximum drive/slew

**Table 82 • LVCMOS 1.2 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

On-Die Termination (ODT)	T <sub>PY</sub>		T <sub>PYS</sub>		Unit
	-1	-Std	-1	-Std	
None	4.154	4.887	4.114	4.84	ns
50	6.918	8.139	6.806	8.008	ns
75	5.613	6.603	5.533	6.509	ns
150	4.716	5.549	4.657	5.479	ns

**Table 83 • LVCMOS 1.2 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub> <sup>1</sup>		T <sub>LZ</sub> <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	6.713	7.897	5.362	6.308	6.723	7.909	7.233	8.51	6.375	7.499	ns
	Medium	5.912	6.955	4.616	5.43	5.915	6.959	6.887	8.102	6.009	7.069	ns
	Medium fast	5.5	6.469	4.231	4.978	5.5	6.471	6.672	7.849	5.835	6.865	ns
	Fast	5.462	6.426	4.194	4.935	5.463	6.427	6.646	7.819	5.828	6.857	ns
4 mA	Slow	6.109	7.186	4.708	5.539	6.098	7.174	8.005	9.418	7.033	8.274	ns
	Medium	5.355	6.299	4.034	4.746	5.338	6.28	7.637	8.985	6.672	7.849	ns
	Medium fast	4.953	5.826	3.685	4.336	4.932	5.802	7.44	8.752	6.499	7.646	ns
	Fast	4.911	5.777	3.658	4.303	4.89	5.754	7.427	8.737	6.488	7.632	ns
6 mA	Slow	5.89	6.929	4.506	5.301	5.874	6.911	8.337	9.808	7.315	8.605	ns
	Medium	5.176	6.089	3.862	4.543	5.155	6.065	7.986	9.394	6.943	8.168	ns
	Medium fast	4.792	5.637	3.523	4.145	4.765	5.606	7.808	9.186	6.775	7.97	ns
	Fast	4.754	5.593	3.486	4.101	4.728	5.563	7.777	9.149	6.769	7.963	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 84 • LVCMOS 1.2 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub> <sup>1</sup>		T <sub>LZ</sub> <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	6.746	7.937	7.458	8.774	8.172	9.614	9.867	11.608	8.393	9.874	ns
4 mA	Slow	7.068	8.315	6.678	7.857	7.474	8.793	10.986	12.924	9.043	10.638	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.



### 2.3.6.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 103 • DDR1/SSTL2 DC Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V
Termination voltage	$V_{TT}$	1.164	1.250	1.339	V
Input reference voltage	$V_{REF}$	1.164	1.250	1.339	V

**Table 104 • DDR1/SSTL2 DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}$ (DC)	$V_{REF} + 0.15$	2.625	V
DC input logic low	$V_{IL}$ (DC)	-0.3	$V_{REF} - 0.15$	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 105 • DDR1/SSTL2 DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
<b>SSTL2 Class I (DDR Reduced Drive)</b>				
DC output logic high	$V_{OH}$	$V_{TT} + 0.608$		V
DC output logic low	$V_{OL}$		$V_{TT} - 0.608$	V
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	8.1		mA
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-8.1		mA
<b>SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Bank Only</b>				
DC output logic high	$V_{OH}$	$V_{TT} + 0.81$		V
DC output logic low	$V_{OL}$		$V_{TT} - 0.81$	V
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	16.2		mA
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-16.2		mA

**Table 106 • DDR1/SSTL2 DC Differential Voltage Specification**

Parameter	Symbol	Min	Unit
DC input differential voltage	$V_{ID}$ (DC)	0.3	V

**Table 131 • SSTL15 DC Output Voltage Specification (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
<b>DDR3/SSTL15 Class I (DDR3 Reduced Drive)</b>				
DC output logic high	$V_{OH}$	$0.8 \times V_{DDI}$		V
DC output logic low	$V_{OL}$		$0.2 \times V_{DDI}$	V
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	6.5		mA
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-6.5		mA
<b>DDR3/SSTL15 Class II (DDR3 Full Drive)</b>				
DC output logic high	$V_{OH}$	$0.8 \times V_{DDI}$		V
DC output logic low	$V_{OL}$		$0.2 \times V_{DDI}$	V
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	7.6		mA
Output minimum sink current	$I_{OL}$ at $V_{OL}$	-7.6		mA

**Table 132 • SSTL15 DC Differential Voltage Specification (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Unit
DC input differential voltage	$V_{ID}$	0.2	V

**Note:** To meet JEDEC electrical compliance, use DDR3 full drive transmitter.

**Table 133 • SSTL15 AC SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	$V_{DIFF}$ (AC)	0.3		V
AC differential cross point voltage	$V_x$ (AC)	$0.5 \times V_{DDI} - 0.150$	$0.5 \times V_{DDI} + 0.150$	V

**Table 134 • SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	$D_{MAX}$	667	Mbps	AC loading: per JEDEC specifications

**Table 135 • SSTL15 AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	$R_{REF}$	34, 40	$\Omega$	Reference resistor = 240 $\Omega$
Effective impedance value (ODT)	$R_{TT}$	20, 30, 40, 60, 120	$\Omega$	Reference resistor = 240 $\Omega$

### 2.3.7.5 RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

#### Minimum and Maximum Input and Output Levels

**Table 203 • RSDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V

**Table 204 • RSDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	$V_I$	0	2.925	V

**Table 205 • RSDS DC Output Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	$V_{OH}$	1.25	1.425	1.6	V
DC output logic low	$V_{OL}$	0.9	1.075	1.25	V

**Table 206 • RSDS Differential Voltage Specification**

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing	$V_{OD}$	100	600	mV
Output common mode voltage	$V_{OCM}$	0.5	1.5	V
Input common mode voltage	$V_{ICM}$	0.3	1.5	V
Input differential voltage	$V_{ID}$	100	600	mV

**Table 207 • RSDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	520	Mbps	AC loading: 2 pF / 100 $\Omega$ differential load
Maximum data rate (for MSIOD I/O bank)	$D_{MAX}$	700	Mbps	AC loading: 2 pF / 100 $\Omega$ differential load

**Table 208 • RSDS AC Impedance Specifications**

Parameter	Symbol	Typ	Unit
Termination resistance	$R_T$	100	$\Omega$

**Table 209 • RSDS AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	Cross point	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF

The following table lists the input data register propagation delays in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 219 • Input Data Register Propagation Delays**

Parameter	Symbol	Measuring Nodes (from, to) <sup>1</sup>	-1		Unit
			-1	-Std	
Bypass delay of the input register	$T_{IBYP}$	F, G	0.353	0.415	ns
Clock-to-Q of the input register	$T_{ICLKQ}$	E, G	0.16	0.188	ns
Data setup time for the input register	$T_{ISUD}$	A, E	0.357	0.421	ns
Data hold time for the input register	$T_{IHD}$	A, E	0	0	ns
Enable setup time for the input register	$T_{ISUE}$	B, E	0.46	0.542	ns
Enable hold time for the input register	$T_{IHE}$	B, E	0	0	ns
Synchronous load setup time for the input register	$T_{ISUSL}$	D, E	0.46	0.542	ns
Synchronous load hold time for the input register	$T_{IHSL}$	D, E	0	0	ns
Asynchronous clear-to-Q of the input register (ADn=1)	$T_{IALN2Q}$	C, G	0.625	0.735	ns
Asynchronous preset-to-Q of the input register (ADn=0)		C, G	0.587	0.69	ns
Asynchronous load removal time for the input register	$T_{IREMALN}$	C, E	0	0	ns
Asynchronous load recovery time for the input register	$T_{IRECALN}$	C, E	0.074	0.087	ns
Asynchronous load minimum pulse width for the input register	$T_{IWALN}$	C, C	0.304	0.357	ns
Clock minimum pulse width high for the input register	$T_{ICKMPWH}$	E, E	0.075	0.088	ns
Clock minimum pulse width low for the input register	$T_{ICKMPWL}$	E, E	0.159	0.187	ns

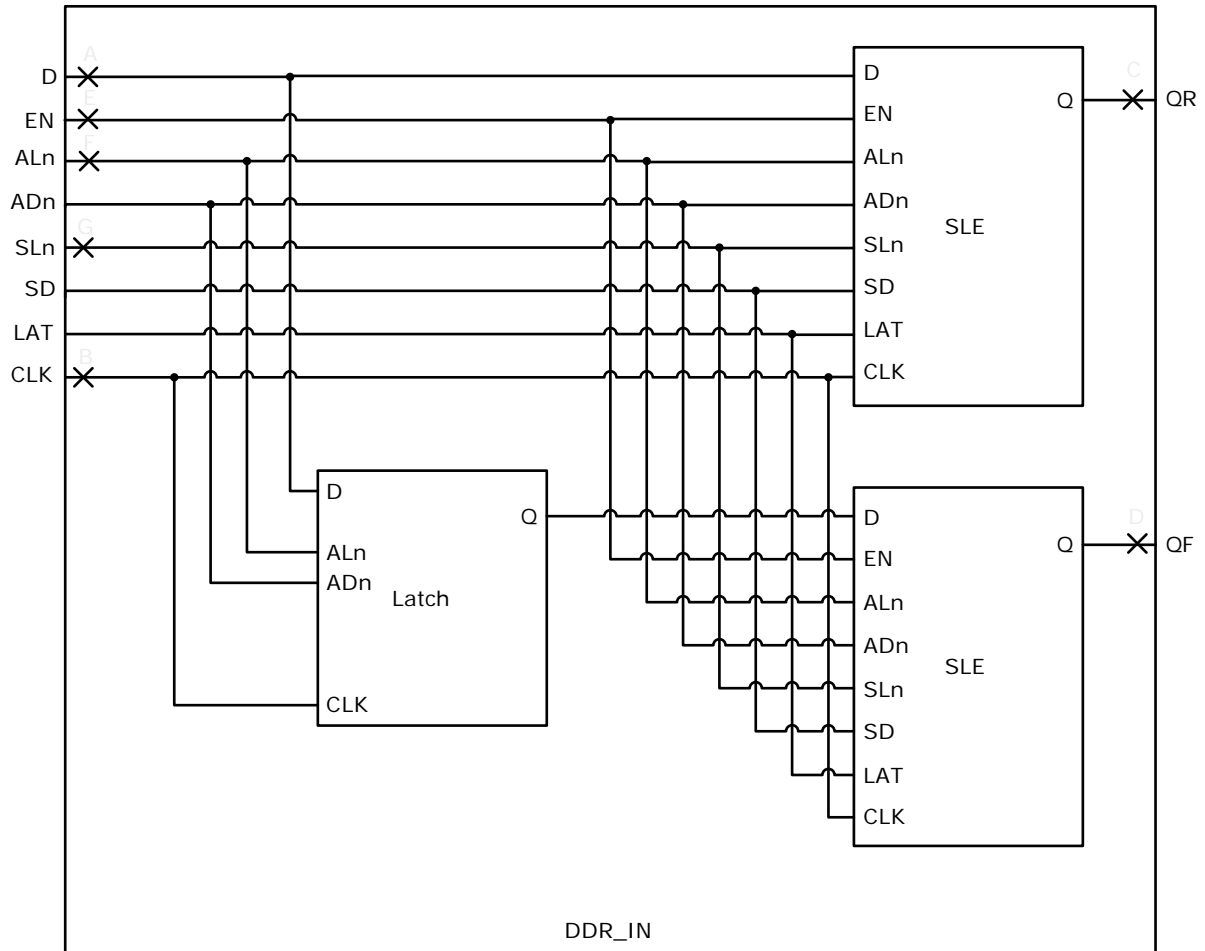
1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

### 2.3.9 DDR Module Specification

This section describes input and output DDR module and timing specifications.

#### 2.3.9.1 Input DDR Module

Figure 10 • Input DDR Module



**Table 232 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 (continued)**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Address setup time	$T_{\text{ADDRSU}}$	0.475		0.559		ns
Address hold time	$T_{\text{ADDRHD}}$	0.274		0.322		ns
Data setup time	$T_{\text{DSU}}$	0.336		0.395		ns
Data hold time	$T_{\text{DHD}}$	0.082		0.096		ns
Block select setup time	$T_{\text{BLKSU}}$	0.207		0.244		ns
Block select hold time	$T_{\text{BLKHD}}$	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	$T_{\text{BLK2Q}}$		1.529		1.799	ns
Block select minimum pulse width	$T_{\text{BLKMPW}}$	0.186		0.219		ns
Read enable setup time	$T_{\text{RDESU}}$	0.485		0.57		ns
Read enable hold time	$T_{\text{RDEHD}}$	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{\text{RDPLESU}}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{\text{RDPLEHD}}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	$T_{\text{R2Q}}$		1.514		1.781	ns
Asynchronous reset removal time	$T_{\text{RSTREM}}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{\text{RSTREC}}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	$T_{\text{RSTMPW}}$	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{\text{PLRSTREM}}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{\text{PLRSTREC}}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{\text{PLRSTMPW}}$	0.282		0.332		ns
Synchronous reset setup time	$T_{\text{SRSTSU}}$	0.226		0.265		ns
Synchronous reset hold time	$T_{\text{SRSTHD}}$	0.036		0.043		ns
Write enable setup time	$T_{\text{WESU}}$	0.415		0.488		ns
Write enable hold time	$T_{\text{WEHD}}$	0.048		0.057		ns
Maximum frequency	$F_{\text{MAX}}$		400		340	MHz

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{\text{DD}} = 1.14\text{ V}$ .

**Table 233 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	$T_{\text{CY}}$	2.5		2.941		ns
Clock minimum pulse width high	$T_{\text{CLKMPWH}}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{\text{CLKMPWL}}$	1.125		1.323		ns
Pipelined clock period	$T_{\text{PLCY}}$	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{\text{PLCLKMPWH}}$	1.125		1.323		ns

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 8K × 2 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 234 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	$T_{CY}$	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	$T_{PLCY}$	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register				0.32	0.377	ns
Read access time without pipeline register	$T_{CLK2Q}$			2.272	2.673	ns
Access time with feed-through write timing				1.511	1.778	ns
Address setup time	$T_{ADDRSU}$	0.612		0.72		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.33		0.388		ns
Data hold time	$T_{DHD}$	0.082		0.096		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns
Block select hold time	$T_{BLKHD}$	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$			1.511	1.778	ns
Block select minimum pulse width	$T_{BLKMPW}$	0.186		0.219		ns
Read enable setup time	$T_{RDESU}$	0.529		0.622		ns
Read enable hold time	$T_{RDEHD}$	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	$T_{R2Q}$			1.528	1.797	ns
Asynchronous reset removal time	$T_{RSTREM}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTREC}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	$T_{RSTMPW}$	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTSU}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTHD}$	0.036		0.043		ns
Write enable setup time	$T_{WESU}$	0.488		0.574		ns
Write enable hold time	$T_{WEHD}$	0.048		0.057		ns
Maximum frequency	$F_{MAX}$			400	340	MHz

**Table 242 •  $\mu$ SRAM (RAM512x2) in 512 x 2 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Write clock period	$T_{CCY}$	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	$T_{BLKCSU}$	0.404		0.476		ns
Write block hold time	$T_{BLKCHD}$	0.007		0.008		ns
Write input data setup time	$T_{DINCSU}$	0.101		0.118		ns
Write input data hold time	$T_{DINCHD}$	0.137		0.161		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.247		0.29		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.03		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

The following table lists the  $\mu$ SRAM in 1024 x 1 mode in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 243 •  $\mu$ SRAM (RAM1024x1) in 1024 x 1 Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	$T_{CY}$	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	$T_{PLCY}$	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	$T_{CLK2Q}$		0.27		0.31	ns
Read access time without pipeline register				1.78		2.1
Read address setup time in synchronous mode	$T_{ADDRSU}$	0.301		0.354		ns
Read address setup time in asynchronous mode			1.978		2.327	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.137		0.161		ns
Read address hold time in asynchronous mode			-0.6		-0.71	
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHHD}$	-0.65		-0.77		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.16		2.54	ns
Read asynchronous reset removal time (pipelined clock)	$T_{RSTREM}$	-0.02		-0.03		ns
Read asynchronous reset removal time (non-pipelined clock)			0.046		0.054	



The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 270 • Math Block with Input Register Used and Output in Bypass Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input register setup time	$T_{MISU}$	0.149		0.176		ns
Input register hold time	$T_{MIHD}$	0.185		0.218		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	0.08		0.094		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	-0.012		-0.014		ns
Asynchronous reset removal time	$T_{MARSTREM}$	-0.005		-0.005		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.088		0.104		ns
Input register clock to output delay	$T_{MICQ}$		2.52		2.964	ns
CDIN to output delay	$T_{MCDIN2Q}$		1.951		2.295	ns

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 271 • Math Block with Input and Output in Bypass Mode**

Parameter	Symbol	-1	-Std	Unit
		Max	Max	
Input to output delay	$T_{MIQ}$	2.568	3.022	ns
CDIN to output delay	$T_{MCDIN2Q}$	1.951	2.295	ns

### 2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when  $V_{DD} = 1.14\text{ V}$ ,  $V_{PPNVM} = V_{PP} = 2.375\text{ V}$ .

**Table 272 • eNVM Read Performance**

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
$T_J$	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$F_{MAXREAD}$	eNVM maximum read frequency	25	25	25	25	25	25	MHz

The following table lists the eNVM page programming in worst-case conditions when  $V_{DD} = 1.14\text{ V}$ ,  $V_{PPNVM} = V_{PP} = 2.375\text{ V}$ .

**Table 273 • eNVM Page Programming**

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
$T_J$	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$T_{PAGEPGM}$	eNVM page programming time	40	40	40	40	40	40	ms

## 2.3.17 Non-Deterministic Random Bit Generator (NRBG) Characteristics

For more information about NRBG, see *AC407: Using NRBG Services in SmartFusion2 and IGLOO2 Devices Application Note*. The following table lists the NRBG in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 275 • Non-Deterministic Random Bit Generator (NRBG)**

Service	Timing	Unit	Conditions	
			Prediction Resistance	Additional Input
Instantiate	85	ms	OFF	X
Generate (after Instantiate) <sup>1</sup>	4.5 ms + (6.25 us/byte x No. of Bytes)		OFF	0
	6.0 ms + (6.25 us/byte x No. of Bytes)		OFF	64
	7.0 ms + (6.25 us/byte x No. of Bytes)		OFF	128
Generate (after Instantiate)	47	ms	ON	X
Generate (subsequent) <sup>1</sup>	0.5 ms + (6.25 us/byte x No. of Bytes)		OFF	0
	2.0 ms + (6.25 us/byte x No. of Bytes)		OFF	64
	3.0 ms + (6.25 us/byte x No. of Bytes)		OFF	128
Generate (subsequent)	43	ms	ON	X
Reseed	40	ms		
Uninstantiate	0.16	ms		
Reset	0.10	ms		
Self test	20	ms	First time after power-up	
	6	ms	Subsequent	

1. If PUF\_OFF, generate will incur additional PUF delay time for consecutive service calls.

## 2.3.18 Cryptographic Block Characteristics

For more information about cryptographic block and associated services, see *AC410: Using AES System Services in SmartFusion2 and IGLOO2 Devices Application Note* and *AC432: Using SHA-256 System Services in SmartFusion2 and IGLOO2 Devices Application Note*.

The following table lists the cryptographic block characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 276 • Cryptographic Block Characteristics**

Service	Conditions	Timing	Unit
Any service	First certificate check penalty at boot	11.5	ms
AES128/256 (encoding / decoding) <sup>1</sup>	100 blocks up to 64k blocks	700	kbps

**Table 276 • Cryptographic Block Characteristics (continued)**

Service	Conditions	Timing	Unit
SHA256	512 bits	540	kbps
	1024 bits	780	kbps
	2048 bits	950	kbps
	24 kbits	1140	kbps
HMAC	512 bytes	820	kbps
	1024 bytes	890	kbps
	2048 bytes	930	kbps
	24 kbytes	980	kbps
KeyTree		1.8	ms
Challenge-response	PUF = OFF	25	ms
	PUF = ON	7	ms
ECC point multiplication		590	ms
ECC point addition		8	ms

1. Using cypher block chaining (CBC) mode.

## 2.3.19 Crystal Oscillator

The following table describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

**Table 277 • Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)**

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		20		MHz	
Accuracy	ACCXTAL			0.0047	%	005, 010, 025, 050, 060, and 090 devices
				0.0058	%	150 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		200	300	ps	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		200	300	ps	010, 025, 050, and 060 devices
			250	410	ps	150 devices
			250	550	ps	005 and 090 devices
Operating current	IDYNXTAL		1.5		mA	010, 050, and 060 devices
			1.65		mA	005, 025, 090, and 150 devices
Input logic level high	VIHXTAL	0.9 V <sub>PP</sub>			V	
Input logic level low	VILXTAL			0.1 V <sub>PP</sub>	V	

## 2.3.24 Power-up to Functional Times

The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 288 • Power-up to Functional Times for SmartFusion2**

Symbol	From	To	Description	Maximum Power-up to Functional Time for SmartFusion2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	647	500	531	483	474	524	647
$T_{POR2MSSRST}$	POWER_ON_RESET_N	MSS_RESE T_N_M2F	Fabric to MSS	644	497	528	480	468	518	641
$T_{MSSRST2OUT}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.6	3.6	3.6	3.4	4.9	4.8	4.8
$T_{VDD2OUT}$	$V_{DD}$	Output available at I/O	$V_{DD}$ at its minimum threshold level to output	3096	2975	3012	2959	2869	2992	3225
$T_{VDD2POR}$	$V_{DD}$	POWER_ON_RESET_N	$V_{DD}$ at its minimum threshold level to fabric	2476	2487	2496	2486	2406	2563	2602
$T_{VDD2MSSRST}$	$V_{DD}$	MSS_RESE T_N_M2F	$V_{DD}$ at its minimum threshold level to MSS	3093	2972	3008	2956	2864	2987	3220
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

**Note:** For more information about power-up times, see *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

**Table 291 • DEVRST\_N to Functional Times for SmartFusion2 (continued)**

Symbol	From	To	Description	Maximum Power-up to Functional Time for SmartFusion2 (uS)						
				005	010	025	050	060	090	150
$T_{DEVRST2POR}$	DEVRST_N	POWER_ON_RESET_N	$V_{DD}$ at its minimum threshold level to fabric	233	289	216	213	237	234	219
$T_{DEVRST2MSSRST}$	DEVRST_N	MSS_RESET_N_M2F	$V_{DD}$ at its minimum threshold level to MSS	702	765	712	688	636	630	866
$T_{DEVRST2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215

**Figure 19 • DEVRST\_N to Functional Timing Diagram for SmartFusion2**

