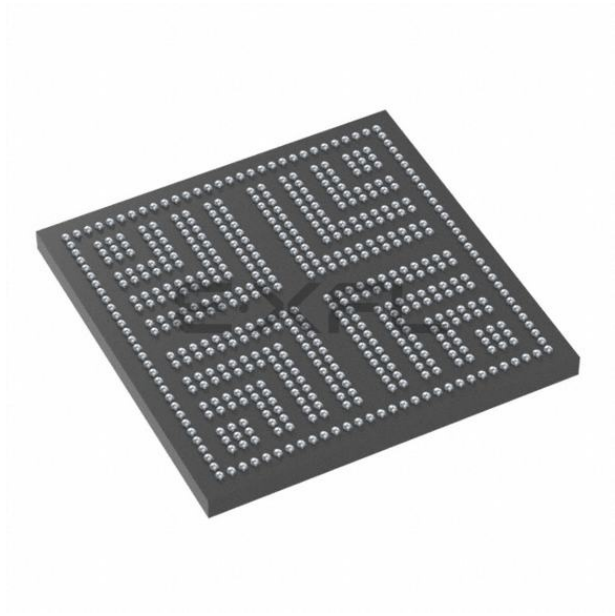

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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | ARM® Cortex®-M3 |
| Flash Size | 512KB |
| RAM Size | 64KB |
| Peripherals | DDR, PCIe, SERDES |
| Connectivity | CANbus, Ethernet, I²C, SPI, UART/USART, USB |
| Speed | 166MHz |
| Primary Attributes | FPGA - 150K Logic Modules |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 536-LFBGA, CSPBGA |
| Supplier Device Package | 536-CSPBGA (16x16) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2s150-1fcsg536i |

1. For flash programming and retention maximum limits, see Table 5, page 7. For recommended operating conditions, see Table 4, page 6.

***Table 4 •*** Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Operating junction temperature | $T_J$ | 0 | 25 | 85 | °C | Commercial |
| | | –40 | 25 | 100 | °C | Industrial |
| Programming junction temperatures[1] | $T_J$ | 0 | 25 | 85 | °C | Commercial |
| | | –40 | 25 | 100 | °C | Industrial |
| DC core supply voltage. Must always power this pin. | $V_{DD}$ | 1.14 | 1.2 | 1.26 | V | |
| Power supply for charge pumps (for normal operation and programming) for the 005, 010, 025, 050, 060 devices | $V_{PP}$ | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Power supply for charge pumps (for normal operation and programming) for the 090 and 150 devices | $V_{PP}$ | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for MDDR PLL | MSS_MDDR_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for MDDR PLL | HPMS_MDDR_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for FDDR PLL | FDDR_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for MDDR PLL | PLL0_PLL1_MSS_MDDR_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for MDDR PLL | PLL0_PLL1_HPMS_MDDR_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for PLL0 to PLL5 | CCC_XX[01]_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| High supply voltage for PLL SerDes[01] | SERDES_[01]_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power for SerDes[01] PLL Lane 0 to Lane 3. This is a 2.5 V SerDes internal PLL supply. | SERDES_[01]_L[0123]_VDDAPLL | 2.375 | 2.5 | 2.625 | V | |
| TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply. | SERDES_[01]_L[0123]_VDDAIO | 1.14 | 1.2 | 1.26 | V | |
| PCIe/PCS power supply | SERDES_[01]_VDD | 1.14 | 1.2 | 1.26 | V | |
| 1.2 V DC supply voltage | $V_{DDIx}$ | 1.14 | 1.2 | 1.26 | V | |
| 1.5 V DC supply voltage | $V_{DDIx}$ | 1.425 | 1.5 | 1.575 | V | |
| 1.8 V DC supply voltage | $V_{DDIx}$ | 1.71 | 1.8 | 1.89 | V | |
| 2.5 V DC supply voltage | $V_{DDIx}$ | 2.375 | 2.5 | 2.625 | V | |

***Table 19 •*** Maximum Data Rate Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---|---|---|---|---|
| LPDDR | | | 400 | Mbps |
| HSTL1.5 V | | | 400 | Mbps |
| SSTL 2.5 V | 510 | 700 | 400 | Mbps |
| SSTL 1.8 V | | | 667 | Mbps |
| SSTL 1.5 V | | | 667 | Mbps |

***Table 20 •*** Maximum Data Rate Summa ry Table for Differential I/O in Worst-Case Industrial Conditions

| I/O | MSIO | MSIOD | Unit |
|---|---|---|---|
| LVPECL (input only) | 900 | | Mbps |
| LVDS 3.3 V | 535 | | Mbps |
| LVDS 2.5 V | 535 | 700 | Mbps |
| RSDS | 520 | 700 | Mbps |
| BLVDS | 500 | | Mbps |
| MLVDS | 500 | | Mbps |
| Mini-LVDS | 520 | 700 | Mbps |

***Table 21 •*** Maximum Frequency Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---|---|---|---|---|
| PCI 3.3 V | 315 | | | MHz |
| LVTTL 3.3 V | 300 | | | MHz |
| LVCMOS 3.3 V | 300 | | | MHz |
| LVCMOS 2.5 V | 205 | 210 | 200 | MHz |
| LVCMOS 1.8 V | 147.5 | 200 | 200 | MHz |
| LVCMOS 1.5 V | 80 | 110 | 118 | MHz |
| LVCMOS 1.2 V | 60 | 80 | 100 | MHz |
| LPDDR– LVCMOS 1.8 V mode | | | 200 | MHz |

***Table 43 •*** LVCMOS 2.5 V AC Test Parameter Specifications

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 1.2 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ωσ |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

***Table 44 •*** LVCMOS 2.5 V Transmitter Drive Strength Specifications

| Output Drive Selection | | | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA |
|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank (With Software Default Fixed Code) | Min | Max | | |
| 2 mA | 2 mA | 2 mA | $V_{DDI}$ – 0.4 | 0.4 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | $V_{DDI}$ – 0.4 | 0.4 | 4 | 4 |
| 6 mA | 6 mA | 6 mA | $V_{DDI}$ – 0.4 | 0.4 | 6 | 6 |
| 8 mA | 8 mA | 8 mA | $V_{DDI}$ – 0.4 | 0.4 | 8 | 8 |
| 12 mA | 12 mA | 12 mA | $V_{DDI}$ – 0.4 | 0.4 | 12 | 12 |
| 16 mA | | 16 mA | $V_{DDI}$ – 0.4 | 0.4 | 16 | 16 |

Note: For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V

***Table 45 •*** LVCMOS 2.5 V Receiver Charac teristics (Input Buffers)

| | On-Die Termination (ODT) | $T_{PY}$ | | $T_{PYS}$ | | Unit |
|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | |
| LVCMOS 2.5 V (for DDRIO I/O bank) | None | 1.823 | 2.145 | 1.932 | 2.274 | ns |
| LVCMOS 2.5 V (for MSIO I/O bank) | None | 2.486 | 2.925 | 2.495 | 2.935 | ns |
| LVCMOS 2.5 V (for MSIOD I/O bank) | None | 2.29 | 2.694 | 2.305 | 2.712 | ns |

***Table 46 •*** LVCMOS 2.5 V Transmitter Characteristics fo r DDRIO Bank (Output and Tristate Buffers)

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 3.657 | 4.302 | 3.393 | 3.991 | 3.675 | 4.323 | 3.894 | 4.582 | 3.552 | 4.18 | ns |
| | Medium | 3.374 | 3.97 | 3.139 | 3.693 | 3.396 | 3.995 | 3.635 | 4.277 | 3.253 | 3.828 | ns |
| | Medium fast | 3.239 | 3.811 | 3.036 | 3.572 | 3.261 | 3.836 | 3.519 | 4.141 | 3.128 | 3.681 | ns |
| | Fast | 3.224 | 3.793 | 3.029 | 3.563 | 3.246 | 3.818 | 3.512 | 4.132 | 3.119 | 3.67 | ns |

***Table 48 •*** LVCMOS 2.5 V Transmitter Characteristics fo r MSIOD Bank (Output and Tristate Buffers)

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 2.206 | 2.596 | 2.678 | 3.15 | 2.64 | 3.106 | 4.935 | 5.805 | 4.74 | 5.576 | ns |
| 4 mA | Slow | 1.835 | 2.159 | 2.242 | 2.637 | 2.256 | 2.654 | 5.413 | 6.368 | 5.15 | 6.059 | ns |
| 6 mA | Slow | 1.709 | 2.01 | 2.132 | 2.508 | 2.167 | 2.549 | 5.813 | 6.838 | 5.499 | 6.469 | ns |
| 8 mA | Slow | 1.63 | 1.918 | 1.958 | 2.303 | 2.012 | 2.367 | 6.226 | 7.324 | 5.816 | 6.842 | ns |
| 12 mA | Slow | 1.648 | 1.939 | 1.86 | 2.187 | 1.921 | 2.259 | 6.519 | 7.669 | 6.027 | 7.09 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### *2.3.5.8 1.8 V LVCMOS*

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

Minimum and Maximum DC/AC Input and Output Levels Specification

***Table 49 •*** LVCMOS 1.8 V DC Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LVCMOS 1.8 V DC Recommended Operating Conditions | | | | | |
| Supply voltage | $V_{DDI}$ | 1.710 | 1.8 | 1.89 | V |

***Table 50 •*** LVCMOS 1.8 V DC Input Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high (for MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 1.89 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.35 × $V_{DDI}$ | V |
| Input current high[1] | $I_{IH}$ (DC) | | | – |
| Input current low[1] | $I_{IL}$ (DC) | | | – |

1. See Table 24, page 22.

***Table 51 •*** LVCMOS 1.8 V DC Output Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | $V_{DDI}$ – 0.45 | | V |
| DC output logic low | $V_{OL}$ | | 0.45 | V |

***Table 52 •*** LVCMOS 1.8 V Minimum and Maximum AC Switching Speed

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank)[1] | $D_{MAX}$ | 400 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 295 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank)[1] | $D_{MAX}$ | 400 | Mbps | AC loading: 17 pF load, maximum drive/slew |

1. Maximum Data Rate applies for Drive Strength 8 mA and above, All Slews.

***Table 62 •*** LVCMOS 1.5 V DC Output Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | VOH | $V_{DDI}$ × 0.75 | | V |
| DC output logic low | VOL | | $V_{DDI}$ × 0.25 | V |

***Table 63 •*** LVCMOS 1.5 V AC Minimum and Maximum Switching Speed

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 235 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 160 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 220 | Mbps | AC loading: 17 pF load, maximum drive/slew |

***Table 64 •*** LVCMOS 1.5 V AC Calibrated Impedance Option

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | RODT_CAL | 75, 60, 50, 40 | Ω |

***Table 65 •*** LVCMOS 1.5 V AC Test Parameter Specifications

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point | $V_{TRIP}$ | 0.75 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

***Table 66 •*** LVCMOS 1.5 V Transmitter Drive Strength Specifications

| Output Drive Selection | | | $V_{OH}$ (V) | $V_{OL}$ (V) | IOH (at $V_{OH}$) | IOL (at $V_{OL}$) |
|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank | Min | Max | mA | mA |
| 2 mA | 2 mA | 2 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 4 | 4 |
| 6 mA | 6 mA | 6 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 6 | 6 |
| 8 mA | | 8 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 8 | 8 |
| | | 10 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 10 | 10 |
| | | 12 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 12 | 12 |

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

***Table 107 •*** SSTL2 AC Differential Voltage Specifications

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| AC input differential voltage | $V_{DIFF}$ (AC) | 0.7 | | V |
| AC differential cross point voltage | $V_x$ (AC) | 0.5 × $V_{DDI}$ – 0.2 | 0.5 × $V_{DDI}$ + 0.2 | V |

***Table 108 •*** SSTL2 Minimum and Maximum AC Switching Speeds

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 400 | Mbps | AC loading: per JEDEC specifications |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 575 | Mbps | AC loading: 17pF load |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 700 | Mbps | AC loading: 3 pF / 50 Ω load |
| | | 510 | Mbps | AC loading: 17pF load |

***Table 109 •*** SSTL2 AC Impedance Specifications

| Parameter | Typ | Unit | Conditions |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | 20, 42 | Ω | Reference resistor = 150 Ω |

***Table 110 •*** DDR1/SSTL2 AC Test Para meter Specifications

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 1.25 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for SSTL2 Class I ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Reference resistance for data test path for SSTL2 Class II ($T_{DP}$) | RTT_TEST | 25 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V

***Table 111 •*** SSTL2 Receiver Characteristics fo r DDRIO I/O Bank (Input Buffers)

| | On-Die Termination (ODT) | $T_{PY}$ | | |
|---|---|---|---|---|
| | | –1 | –Std | Unit |
| Pseudo differential | None | 1.549 | 1.821 | ns |
| True differential | None | 1.589 | 1.87 | ns |

***Table 112 •*** SSTL2 Receiver Characteristics fo r MSIO I/O Bank (Input Buffers)

| | On-Die Termination (ODT) | $T_{PY}$ | | |
|---|---|---|---|---|
| | | –1 | –Std | Unit |
| Pseudo differential | None | 2.798 | 3.293 | ns |
| True differential | None | 2.733 | 3.215 | ns |

***Table 113 •*** DDR1/SSTL2 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

| | On-Die Termination (ODT) | $T_{PY}$ | | |
|---|---|---|---|---|
| | | –1 | –Std | Unit |
| Pseudo differential | None | 2.476 | 2.913 | ns |
| True differential | None | 2.475 | 2.911 | ns |

***Table 114 •*** SSTL2 Class I Transmitter Char acteristics for DDRIO I/O Bank (Output and Tristate Buffers)

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 2.26 | 2.66 | 1.99 | 2.341 | 1.985 | 2.335 | 2.135 | 2.512 | 2.13 | 2.505 | ns |
| Differential | 2.26 | 2.658 | 2.202 | 2.591 | 2.201 | 2.589 | 2.393 | 2.815 | 2.392 | 2.814 | ns |

***Table 115 •*** DDR1/SSTL2 Class I Transmitter Char acteristics for MSIO I/O Bank (Output and Tristate Buffers)

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 2.055 | 2.417 | 2.037 | 2.396 | 2.03 | 2.388 | 2.068 | 2.433 | 2.061 | 2.425 | ns |
| Differential | 2.192 | 2.58 | 2.434 | 2.864 | 2.425 | 2.852 | 2.164 | 2.545 | 2.156 | 2.536 | ns |

***Table 116 •*** DDR1/SSTL2 Class I Transmitter Ch aracteristics for MSIOD I/O Bank (Output and Tristate Buffers)

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 1.512 | 1.779 | 1.462 | 1.72 | 1.462 | 1.72 | 1.676 | 1.972 | 1.676 | 1.971 | ns |
| Differential | 1.676 | 1.971 | 1.774 | 2.087 | 1.766 | 2.077 | 1.854 | 2.181 | 1.845 | 2.171 | ns |

***Table 117 •*** DDR1/SSTL2 Class II Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 2.122 | 2.497 | 1.906 | 2.243 | 1.902 | 2.237 | 2.061 | 2.424 | 2.056 | 2.418 | ns |
| Differential | 2.127 | 2.501 | 2.042 | 2.402 | 2.043 | 2.403 | 2.363 | 2.78 | 2.365 | 2.781 | ns |

**Table 131 •** SSTL15 DC Output Voltage Specifi cation (for DDRIO I/O Bank Only)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DDR3/SSTL15 Class I (DDR3 Reduced Drive) | | | | |
| DC output logic high | $V_{OH}$ | 0.8 × $V_{DDI}$ | | V |
| DC output logic low | $V_{OL}$ | | 0.2 × $V_{DDI}$ | V |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 6.5 | | mA |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –6.5 | | mA |
| DDR3/SSTL15 Class II (DDR3 Full Drive) | | | | |
| DC output logic high | $V_{OH}$ | 0.8 × $V_{DDI}$ | | V |
| DC output logic low | $V_{OL}$ | | 0.2 × $V_{DDI}$ | V |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 7.6 | | mA |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –7.6 | | mA |

**Table 132 •** SSTL15 DC Differential Voltage Specifi cation (for DDRIO I/O Bank Only)

| Parameter | Symbol | Min | Unit |
|---|---|---|---|
| DC input differential voltage | $V_{ID}$ | 0.2 | V |

Note: To meet JEDEC electrical compliance, use DDR3 full drive transmitter.

**Table 133 •** SSTL15 AC SSTL15 Minimum an d Maximum AC Switching Speed (for DDRIO I/O Bank Only)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| AC input differential voltage | $V_{DIFF}$ (AC) | 0.3 | | V |
| AC differential cross point voltage | $V_X$ (AC) | 0.5 × $V_{DDI}$ – 0.150 | 0.5 × $V_{DDI}$ + 0.150 | V |

**Table 134 •** SSTL15 Minimum and Maximu m AC Switching Speed (for DDRIO I/O Bank Only)

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | 667 | Mbps | AC loading: per JEDEC specifications |

**Table 135 •** SSTL15 AC Calibrated Impedance Option (for DDRIO I/O Bank Only)

| Parameter | Symbol | Typ | Unit | Conditions |
|---|---|---|---|---|
| Supported output driver calibrated impedance | $R_{REF}$ | 34, 40 | Ω | Reference resistor = 240 Ω |
| Effective impedance value (ODT) | $R_{TT}$ | 20, 30, 40, 60, 120 | Ω | Reference resistor = 240 Ω |

AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V.

**Table 180 •** B-LVDS AC Switching Ch aracteristics for Receiver for MSIO I/O Bank (Input Buffers)

| | $T_{PY}$ | | |
|---|---|---|---|
| On-Die Termination (ODT) | –1 | –Std | Unit |
| None | 2.738 | 3.221 | ns |
| 100 | 2.735 | 3.218 | ns |

**Table 181 •** B-LVDS AC Switching Ch aracteristics for Receiver for MSIOD I/O Bank (Input Buffers)

| | $T_{PY}$ | | |
|---|---|---|---|
| On-Die Termination (ODT) | –1 | –Std | Unit |
| None | 2.495 | 2.934 | ns |
| 100 | 2.495 | 2.935 | ns |

**Table 182 •** B-LVDS AC Switching Characteristics for Tr ansmitter (for MSIO I/O Bank - Output and Tristate Buffers)

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2.258 | 2.656 | 2.343 | 2.756 | 2.329 | 2.74 | 2.12 | 2.494 | 2.123 | 2.497 | ns |

### 2.3.7.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum Input and Output Levels

**Table 183 •** M-LVDS Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage[1] | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

1. Only M-LVDS TYPE I is supported.

**Table 184 •** M-LVDS DC Input Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input voltage | $V_I$ | 0 | 2.925 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[2] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

**Table 191 •** M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)

| | $T_{PY}$ | | |
|---|---|---|---|
| On-Die Termination (ODT) | –1 | –Std | Unit |
| None | 2.495 | 2.934 | ns |
| 100 | 2.495 | 2.935 | ns |

**Table 192 •** M-LVDS AC Switching Characteristics for Tran smitter (for MSIO I/O Bank - Output and Tristate Buffers)

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2.258 | 2.656 | 2.348 | 2.762 | 2.334 | 2.746 | 2.123 | 2.497 | 2.125 | 2.5 | ns |

### 2.3.7.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

Mini-LVDS Minimum and Maximu m Input and Output Levels

**Table 193 •** Mini-LVDS Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

**Table 194 •** Mini-LVDS DC Input Vo ltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC Input voltage | $V_I$ | 0 | 2.925 | V |

**Table 195 •** Mini-LVDS DC Output Vo ltage Specification

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

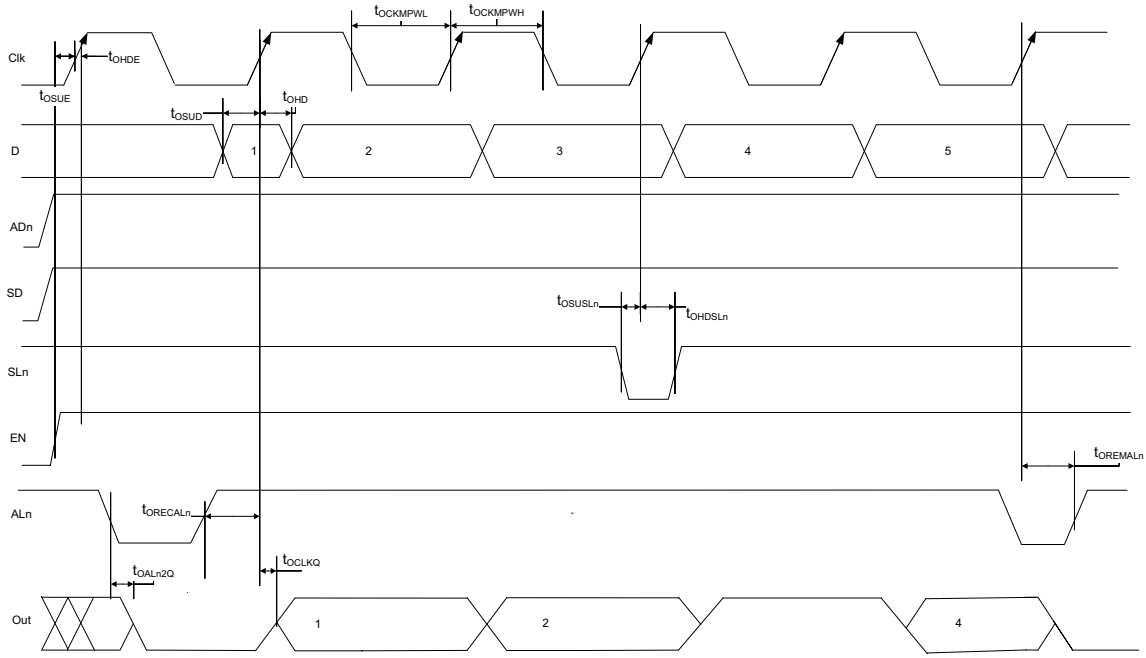
**Table 196 •** Mini-LVDS DC Differential Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Differential output voltage swing | $V_{OD}$ | 300 | 600 | mV |
| Output common mode voltage | $V_{OCM}$ | 1 | 1.4 | V |
| Input common mode voltage | $V_{ICM}$ | 0.3 | 1.2 | V |
| Input differential voltage | $V_{ID}$ | 100 | 600 | mV |

**Table 197 •** Mini-LVDS Minimum and Maxi mum AC Switching Speed

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 520 | Mbps | AC loading: 2 pF / 100 Ω differential load |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 700 | Mbps | AC loading: 2 pF / 100 Ω differential load |

***Figure 9 •*** I/O Register Output Timing Diagram




The following table lists the output/enable propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 220 •*** Output/Enable Data Register Propagation Delays

| Parameter | Symbol | Measuring Nodes (from, to) [1] | –1 | –Std | Unit |
|---|---|---|---|---|---|
| Bypass delay of the output/enable register | $T_{OBYP}$ | F, G or H, I | 0.353 | 0.415 | ns |
| Clock-to-Q of the output/enable register | $T_{OCLKQ}$ | E, G or E, I | 0.263 | 0.309 | ns |
| Data setup time for the output/enable register | $T_{OSUD}$ | A, E or J, E | 0.19 | 0.223 | ns |
| Data hold time for the output/enable register | $T_{OHD}$ | A, E or J, E | 0 | 0 | ns |
| Enable setup time for the output/enable register | $T_{OSUE}$ | B, E | 0.419 | 0.493 | ns |
| Enable hold time for the output/enable register | $T_{OHE}$ | B, E | 0 | 0 | ns |
| Synchronous load setup time for the output/enable register | $T_{OSUSL}$ | D, E | 0.196 | 0.231 | ns |
| Synchronous load hold time for the output/enable register | $T_{OHSL}$ | D, E | 0 | 0 | ns |
| Asynchronous clear-to-q of the output/enable register (ADn = 1) | $T_{OALN2Q}$ | C, G or C, I | 0.505 | 0.594 | ns |
| Asynchronous preset-to-q of the output/enable register (ADn = 0) | | C, G or C, I | 0.528 | 0.621 | ns |
| Asynchronous load removal time for the output/enable register | $T_{OREMALN}$ | C, E | 0 | 0 | ns |
| Asynchronous load recovery time for the output/enable register | $T_{ORECALN}$ | C, E | 0.034 | 0.04 | ns |
| Asynchronous load minimum pulse width for the output/enable register | $T_{OWALN}$ | C, C | 0.304 | 0.357 | ns |
| Clock minimum pulse width high for the output/enable register | $T_{OCKMPWH}$ | E, E | 0.075 | 0.088 | ns |
| Clock minimum pulse width low for the output/enable register | $T_{OCKMPWL}$ | E, E | 0.159 | 0.187 | ns |

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

### 2.3.12.2 FPGA Fabric Micro SRAM (µSRAM)

The following table lists the µSRAM in 64 × 18 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 237 •*** µSRAM (RAM64x18) in 64 × 18 Mode

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.266 | | 0.313 | ns |
| Read access time without pipeline register | | | 1.677 | | 1.973 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.856 | | 2.184 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.091 | | 0.107 | | ns |
| Read address hold time in asynchronous mode | | –0.778 | | –0.915 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.765 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.036 | | 2.396 | ns |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.023 | | –0.027 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.839 | | 0.987 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.115 | | 0.135 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.15 | | 0.177 | | ns |

***Table 243 •*** µSRAM (RAM1024x1) in 1024 × 1 Mode ***(continued)***

| Parameter | Symbol | –1 | | –Std | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.83 | | 0.98 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.003 | | 0.004 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.137 | | 0.161 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.247 | | 0.29 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.03 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

## 2.3.13 Programming Times

The following tables list the programming times in typical conditions when $T_J$ = 25 °C, $V_{DD}$ = 1.2 V. External SPI flash part# AT25DF641-s3H is used during this measurement.

***Table 244 •*** JTAG Programming (Fabric Only)

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 302672 | 22 | 10 | Sec |
| 010 | 568784 | 28 | 18 | Sec |
| 025 | 1223504 | 51 | 26 | Sec |
| 050 | 2424832 | 66 | 54 | Sec |
| 060 | 2418896 | 77 | 54 | Sec |
| 090 | 3645968 | 113 | 126 | Sec |
| 150 | 6139184 | 155 | 193 | Sec |

## 2.3.16 SRAM PUF

For more details on static random-access memory (SRAM) physical unclonable functions (PUF) services, see *AC434: Using SRAM PUF System Service in SmartFusion2 Application Note*.

The following table lists the SRAM PUF in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 274 •*** SRAM PUF

| | PUF Off | | PUF On | | |
|---|---|---|---|---|---|
| Service | Typ | Max | Typ | Max | Unit |
| Create activation code | 709.1 | 746.4 | 754.4 | 762.5 | ms |
| Delete activation code | 1329.3 | 1399.3 | 1414.1 | 1429.3 | ms |
| Create intrinsic keycode | 656.6 | 691.1 | 698.5 | 706.0 | ms |
| Create extrinsic keycode | 656.6 | 691.1 | 698.5 | 706.0 | ms |
| Get number of keys | 1.3 | 1.4 | 1.4 | 1.4 | ms |
| Export (Kc0, Kc1) | 998.0 | 1050.5 | 1061.7 | 1073.1 | ms |
| Export 2 keycodes | 2020.2 | 2126.5 | 2149.2 | 2172.3 | ms |
| Export 4 keycodes | 3065.7 | 3227.0 | 3261.3 | 3296.4 | ms |
| Export 8 keycodes | 5101.0 | 5369.5 | 5426.6 | 5485.0 | ms |
| Export 16 keycodes | 9212.1 | 9697.0 | 9800.1 | 9905.5 | ms |
| Import (Kc0, Kc1) | 39.7 | 41.8 | 42.2 | 42.7 | ms |
| Import 2 keycodes | 50.1 | 52.7 | 53.3 | 53.9 | ms |
| Import 4 keycodes | 60.6 | 63.8 | 64.5 | 65.2 | ms |
| Import 8 keycodes | 80.9 | 85.1 | 86.1 | 87.0 | ms |
| Import 16 keycodes | 123.8 | 130.4 | 131.7 | 133.2 | ms |
| Delete keycode | 552.5 | 581.6 | 587.8 | 594.1 | ms |
| Fetch key | 31.4 | 33.0 | 33.4 | 33.7 | ms |
| Fetch ecc key | 20.0 | 21.1 | 21.3 | 21.5 | ms |
| Get seed | 2.0 | 2.1 | 2.2 | 2.2 | ms |

## 2.3.17 Non-Deterministic Random Bit Generator (NRBG) Characteristics

For more information about NRBG, see *AC407: Using NRBG Services in SmartFusion2 and IGLOO2 Devices Application Note.* The following table lists the NRBG in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 275 •*** Non-Deterministic Random Bit Generator (NRBG)

| | | | Conditions | |
|---|---|---|---|---|
| Service | Timing | Unit | Prediction Resistance | Additional Input |
| Instantiate | 85 | ms | OFF | X |
| Generate (after Instantiate)[1] | 4.5 ms + (6.25 us/byte x No. of Bytes) | | OFF | 0 |
| | 6.0 ms + (6.25 us/byte x No. of Bytes) | | OFF | 64 |
| | 7.0 ms + (6.25 us/byte x No. of Bytes) | | OFF | 128 |
| Generate (after Instantiate) | 47 | ms | ON | X |
| Generate (subsequent)[1] | 0.5 ms + (6.25 us/byte x No. of Bytes) | | OFF | 0 |
| | 2.0 ms + (6.25 us/byte x No. of Bytes) | | OFF | 64 |
| | 3.0 ms + (6.25 us/byte x No. of Bytes) | | OFF | 128 |
| Generate (subsequent) | 43 | ms | ON | X |
| Reseed | 40 | ms | | |
| Uninstantiate | 0.16 | ms | | |
| Reset | 0.10 | ms | | |
| Self test | 20 | ms | First time after power-up | |
| | 6 | ms | Subsequent | |

1. If PUF_OFF, generate will incur additional PUF delay time for consecutive service calls.

## 2.3.18 Cryptographic Block Characteristics

For more information about cryptographic block and associated services, see *AC410: Using AES System Services in SmartFusion2 and IGLOO2 Devices Application Note* and *AC432: Using SHA-256 System Services in SmartFusion2 and IGLOO2 Devices Application Note*.

The following table lists the cryptographic block characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 276 •*** Cryptographic Block Characteristics

| Service | Conditions | Timing | Unit |
|---|---|---|---|
| Any service | First certificate check penalty at boot | 11.5 | ms |
| AES128/256 (encoding / decoding)[1] | 100 blocks up to 64k blocks | 700 | kbps |

***Table 277 •*** Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz) ***(continued)***

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 0.8 | ms | 005, 010, 025, and 050 devices |
| | | | | 1.0 | ms | 090 and 150 devices |

***Table 278 •*** Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 2 | | MHz | |
| Accuracy | ACCXTAL | | | 0.00105 | % | 050 devices |
| | | | | 0.003 | % | 005, 010, 025, 090, and 150 devices |
| | | | | 0.004 | % | 060 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 1 | 5 | ns | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 1 | 5 | ns | |
| Operating current | IDYNXTAL | | 0.3 | | mA | |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 4.5 | ms | 010 and 050 devices |
| | | | | 5 | ms | 005 and 025 devices |
| | | | | 7 | ms | 090 and 150 devices |

***Table 279 •*** Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 32 | | kHz | |
| Accuracy | ACCXTAL | | | 0.004 | % | 005, 010, 025, 050, 060, and 090 devices |
| | | | | 0.005 | % | 150 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 150 | 300 | ns | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 150 | 300 | ns | |
| Operating current | IDYNXTAL | | 0.044 | | mA | 010 and 050 devices |
| | | | 0.060 | | mA | 005, 025, 060, 090, and 150 devices |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 115 | ms | 005, 025, 050, 090, and 150 devices |
| | | | | 126 | ms | 010 devices |

## 2.3.22 JTAG

***Table 284 •*** JTAG 1532 for 005, 010, 025, and 050 Devices

| | | 005 | | 010 | | 025 | | 050 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| Clock to Q (data out) | $T_{TCK2Q}$ | 7.47 | 8.79 | 7.73 | 9.09 | 7.75 | 9.12 | 7.89 | 9.28 | ns |
| Reset to Q (data out) | $T_{RSTB2Q}$ | 7.65 | 9 | 6.43 | 7.56 | 6.13 | 7.21 | 7.40 | 8.70 | ns |
| Test data input setup time | $T_{DISU}$ | –1.05 | –0.89 | –0.69 | –0.59 | –0.67 | –0.57 | –0.30 | –0.25 | ns |
| Test data input hold time | $T_{DIHD}$ | 2.38 | 2.8 | 2.38 | 2.8 | 2.42 | 2.85 | 2.09 | 2.45 | ns |
| Test mode select setup time | $T_{TMSSU}$ | –0.73 | –0.62 | –1.03 | –1.21 | –1.1 | –0.94 | 0.28 | 0.33 | ns |
| Test mode select hold time | $T_{TMDHD}$ | 1.36 | 1.6 | 1.43 | 1.68 | 1.93 | 2.27 | 0.16 | 0.19 | ns |
| ResetB removal time | $T_{TRSTREM}$ | –0.77 | –0.65 | –1.08 | –0.92 | –1.33 | –1.13 | –0.45 | –0.38 | ns |
| ResetB recovery time | $T_{TRSTREC}$ | –0.76 | –0.65 | –1.07 | –0.91 | –1.34 | –1.14 | –0.45 | –0.38 | ns |
| TCK maximum frequency | $F_{TCKMAX}$ | 25 | 21.25 | 25 | 21.25 | 25 | 21.25 | 25.00 | 21.25 | MHz |

***Table 285 •*** JTAG 1532 for 060, 090, and 150 Devices

| | | 060 | | 090 | | 150 | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Clock to Q (data out) | $T_{TCK2Q}$ | 8.38 | 9.86 | 8.96 | 10.54 | 8.66 | 10.19 | ns |
| Reset to Q (data out) | $T_{RSTB2Q}$ | 8.54 | 10.04 | 7.75 | 9.12 | 8.79 | 10.34 | ns |
| Test data input setup time | $T_{DISU}$ | –1.18 | –1 | –1.31 | –1.11 | –0.96 | –0.82 | ns |
| Test data input hold time | $T_{DIHD}$ | 2.52 | 2.97 | 2.68 | 3.15 | 2.57 | 3.02 | ns |
| Test mode select setup time | $T_{TMSSU}$ | –0.97 | –0.83 | –1.02 | –0.87 | –0.53 | –0.45 | ns |
| Test mode select hold time | $T_{TMDHD}$ | 1.7 | 2 | 1.67 | 1.96 | 1.02 | 1.2 | ns |
| ResetB removal time | $T_{TRSTREM}$ | –1.21 | –1.03 | –0.76 | –0.65 | –1.03 | –0.88 | ns |
| ResetB recovery time | $T_{TRSTREC}$ | –1.21 | –1.03 | –0.77 | –0.65 | –1.03 | –0.88 | ns |
| TCK maximum frequency | $F_{TCKMAX}$ | 25 | 21.25 | 25 | 21.25 | 25 | 21.25 | MHz |

## 2.3.23 System Controller SPI Characteristics

The following table lists the IGLOO2 DEVRST_N to functional times in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 292 •*** DEVRST_N to Functional Times for IGLOO2

| | | | | Maximum Power-up to Functional Time for IGLOO2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | From | To | Description | 005 | 010 | 025 | 050 | 060 | 090 | 150 |
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 114 | 116 | 113 | 113 | 115 | 115 | 114 |
| $T_{DEVRST2OUT}$ | DEVRST_N | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 314 | 353 | 314 | 307 | 343 | 341 | 341 |
| $T_{DEVRST2POR}$ | DEVRST_N | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 200 | 238 | 201 | 195 | 230 | 229 | 227 |
| $T_{DEVRST2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |