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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 150K Logic Modules
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s150-fc1152i">https://www.e-xfl.com/product-detail/microchip-technology/m2s150-fc1152i</a>



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**Table 4 • Recommended Operating Conditions (continued)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
3.3 V DC supply voltage	$V_{DDIX}$	3.15	3.3	3.45	V	
LVDS differential I/O	$V_{DDIX}$	2.375	2.5	3.45	V	
B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O	$V_{DDIX}$	2.375	2.5	2.625	V	
LVPECL differential I/O	$V_{DDIX}$	3.15	3.3	3.45	V	
Reference voltage supply for FDDR (Bank0) and MDDR (Bank5)	$V_{REFX}$	0.49 × $V_{DDIX}$	0.5 × $V_{DDIX}$	0.51 × $V_{DDIX}$	V	
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to $V_{PP}$ .	$V_{PPNVM}$	2.375 3.15	2.5 3.3	2.625 3.45	V	2.5 V range 3.3 V range

1. Programming at Industrial temperature range is available only with  $V_{PP} = 3.3$  V.

**Note:** Power supply ramps must all be strictly monotonic, without plateaus.

**Table 5 • FPGA Operating Limits**

Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Digest Temperature	Digest Cycles	Retention (Biased/Unbiased)
Commercial	FPGA	Min $T_J = 0$ °C Max $T_J = 85$ °C	Min $T_J = 0$ °C Max $T_J = 85$ °C	500	Min $T_J = 0$ °C Max $T_J = 85$ °C	2000	20 years
Industrial <sup>1</sup>	FPGA	Min $T_J = -40$ °C Max $T_J = 100$ °C	Min $T_J = -40$ °C Max $T_J = 100$ °C	500	Min $T_J = -40$ °C Max $T_J = 100$ °C	2000	20 years

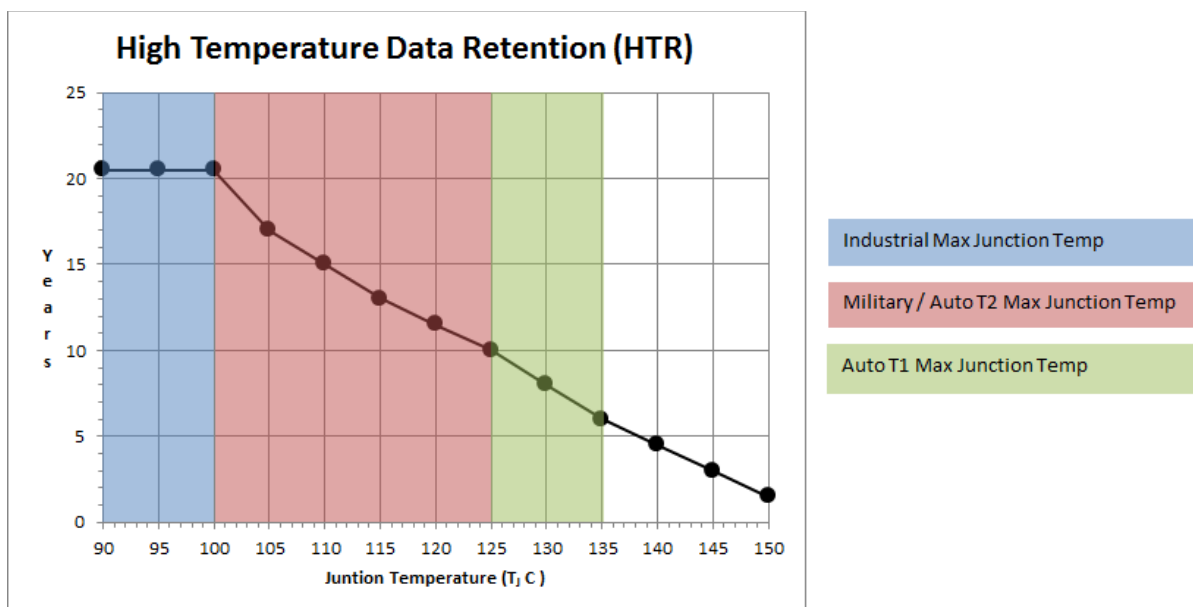
1. Programming at Industrial temperature range is available only with  $V_{PP} = 3.3$  V.

**Note:** The retention specification is defined as the total number of programming and digest cycles. For example, 20 years of retention after 500 programming cycles.

**Note:** The digest cycle specification is 2000 digest cycles for every program cycle with a maximum of 500 programming cycles.

**Note:** If your product qualification requires accelerated programming cycles, see [Microsemi SoC Products Quality and Reliability Report](#) about recommended methodologies.

Figure 1 • High Temperature Data Retention (HTR)



### 2.3.1.1 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to V<sub>CC1</sub> + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

**Note:** The above specifications do not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant with the PCI standard including the PCI overshoot/undershoot specifications.

### 2.3.1.2 Thermal Characteristics

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ1 through EQ3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P} \tag{EQ 1}$$

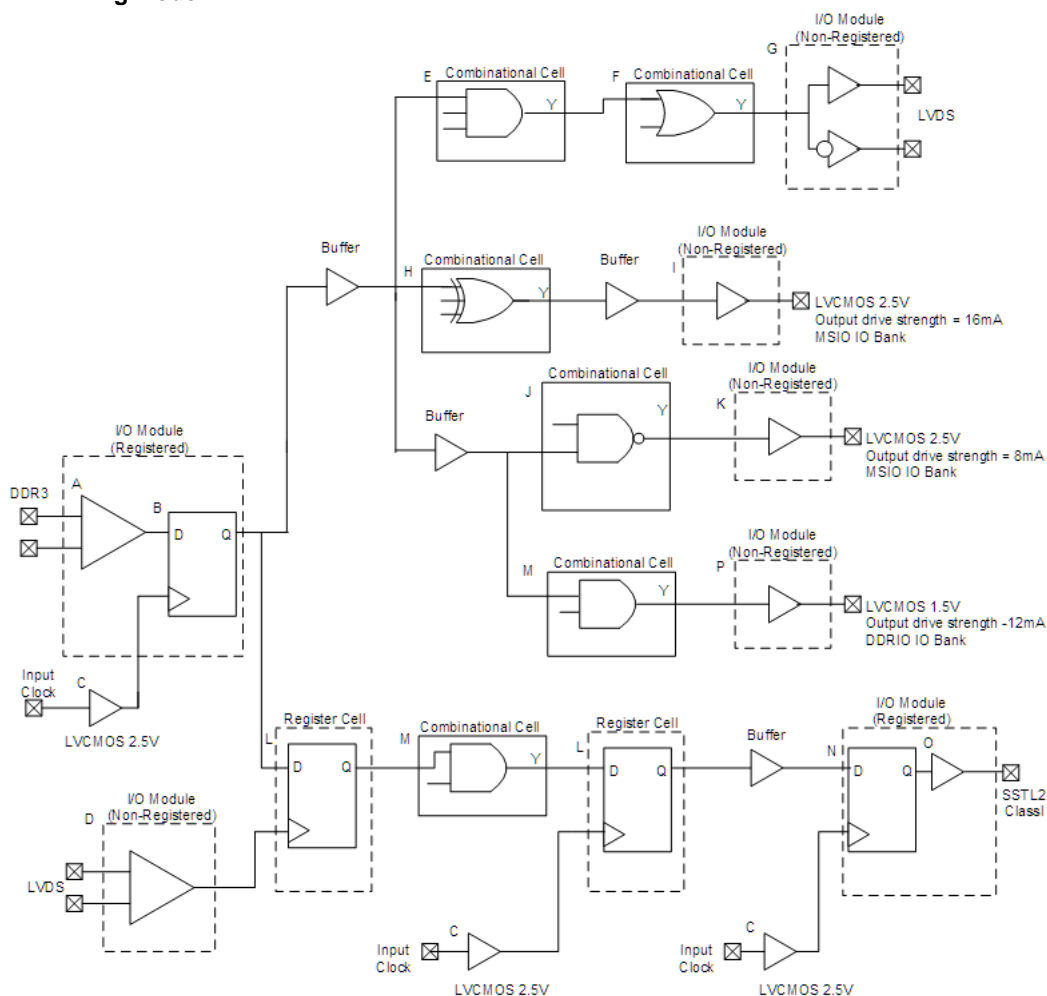
$$\theta_{JB} = \frac{T_J - T_B}{P} \tag{EQ 2}$$

$$\theta_{JC} = \frac{T_J - T_C}{P} \tag{EQ 3}$$

### 2.3.4 Timing Model

This section describes timing model and timing parameters.

Figure 2 • Timing Model



The following table lists the timing model parameters in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 17 • Timing Model Parameters

Index	Symbol	Description	-1	Unit	For More Information
A	$T_{PY}$	Propagation delay of DDR3 receiver	1.605	ns	See Table 137, page 50
B	$T_{ICLKQ}$	Clock-to-Q of the input data register	0.16	ns	See Table 221, page 71
		Setup time of the input data register	0.357	ns	See Table 221, page 71
C	$T_{RCKH}$	Input high delay for global clock	1.53	ns	See Table 227, page 78
		Input low delay for global clock	0.897	ns	See Table 227, page 78
D	$T_{PY}$	Input propagation delay of LVDS receiver	2.774	ns	See Table 167, page 56
E	$T_{DP}$	Propagation delay of a three-input AND gate	0.198	ns	See Table 223, page 76

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIO I/O bank at  $V_{OH}/V_{OL}$  Level.

**Table 26 • I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank**

$V_{DDI}$ Domain	R(WEAK PULL-UP) at $V_{OH}$ ( $\Omega$ )		R(WEAK PULL-DOWN) at $V_{OL}$ ( $\Omega$ )	
	Min	Max	Min	Max
3.3 V	9.9K	17.1K	9.98K	17.5K
2.5 V <sup>1, 2</sup>	10K	17.6K	10.1K	18.4K
1.8 V <sup>1, 2</sup>	10.4K	19.1K	10.4K	20.4K
1.5 V <sup>1, 2</sup>	10.7K	20.4K	10.8K	22.2K
1.2 V <sup>1, 2</sup>	11.3K	23.2K	11.5K	26.7K

1.  $R(\text{WEAK PULL-DOWN}) = (V_{OL\text{spec}})/I(\text{WEAK PULL-DOWN MAX})$ .
2.  $R(\text{WEAK PULL-UP}) = (V_{DDI\text{max}} - V_{OH\text{spec}})/I(\text{WEAK PULL-UP MIN})$ .

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIOD I/O bank at  $V_{OH}/V_{OL}$  Level.

**Table 27 • I/O Weak Pull-up/Pull-down Resistances for MSIOD I/O Bank**

$V_{DDI}$ Domain	R(WEAK PULL-UP) at $V_{OH}$ ( $\Omega$ )		R(WEAK PULL-DOWN) at $V_{OL}$ ( $\Omega$ )	
	Min	Max	Min	Max
2.5 V <sup>1, 2</sup>	9.6K	16.6K	9.5K	16.4K
1.8 V <sup>1, 2</sup>	9.7K	17.3K	9.7K	17.1K
1.5 V <sup>1, 2</sup>	9.9K	18K	9.8K	17.6K
1.2 V <sup>1, 2</sup>	10.3K	19.6K	10K	19.1K

1.  $R(\text{WEAK PULL-DOWN}) = (V_{OL\text{spec}})/I(\text{WEAK PULL-DOWN MAX})$ .
2.  $R(\text{WEAK PULL-UP}) = (V_{DDI\text{max}} - V_{OH\text{spec}})/I(\text{WEAK PULL-UP MIN})$ .

The following table lists the hysteresis voltage value for schmitt trigger mode input buffers.

**Table 28 • Schmitt Trigger Input Hysteresis**

Input Buffer Configuration	Hysteresis Value (Typical, unless otherwise noted)
3.3 V LVTTTL/LVCMOS/ PCI/PCI-X	$0.05 \times V_{DDI}$ (worst-case)
2.5 V LVCMOS	$0.05 \times V_{DDI}$ (worst-case)
1.8 V LVCMOS	$0.1 \times V_{DDI}$ (worst-case)
1.5 V LVCMOS	60 mV
1.2 V LVCMOS	20 mV



## 2.3.5.6 Single-Ended I/O Standards

### 2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

### 2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 29 • LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	3.15	3.3	3.45	V

**Table 30 • LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}$ (DC)	2.0	3.45	V
DC input logic low	$V_{IL}$ (DC)	-0.3	0.8	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 31 • LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC output logic high <sup>1</sup>	$V_{OH}$	$V_{DDI} - 0.4$		V
DC output logic low <sup>1</sup>	$V_{OL}$		0.4	V

1. The  $V_{OH}/V_{OL}$  test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

**Table 32 • LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
DC output logic high	$V_{OH}$	2.4		V
DC output logic low	$V_{OL}$		0.4	V

**Table 33 • LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	600	Mbps	AC loading: 17 pF load, maximum drive/slew

**Table 43 • LVCMOS 2.5 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	1.2	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega\sigma$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**Table 44 • LVCMOS 2.5 V Transmitter Drive Strength Specifications**

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (With Software Default Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	4 mA	4 mA	$V_{DDI} - 0.4$	0.4	4	4
6 mA	6 mA	6 mA	$V_{DDI} - 0.4$	0.4	6	6
8 mA	8 mA	8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	12 mA	12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA		16 mA	$V_{DDI} - 0.4$	0.4	16	16

**Note:** For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at: [www.microsemi.com/soc/download/ibis/default.aspx](http://www.microsemi.com/soc/download/ibis/default.aspx).

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

**Table 45 • LVCMOS 2.5 V Receiver Characteristics (Input Buffers)**

	On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
		-1	-Std	-1	-Std	
LVCMOS 2.5 V (for DDRIO I/O bank)	None	1.823	2.145	1.932	2.274	ns
LVCMOS 2.5 V (for MSIO I/O bank)	None	2.486	2.925	2.495	2.935	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	None	2.29	2.694	2.305	2.712	ns

**Table 46 • LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.657	4.302	3.393	3.991	3.675	4.323	3.894	4.582	3.552	4.18	ns
	Medium	3.374	3.97	3.139	3.693	3.396	3.995	3.635	4.277	3.253	3.828	ns
	Medium fast	3.239	3.811	3.036	3.572	3.261	3.836	3.519	4.141	3.128	3.681	ns
	Fast	3.224	3.793	3.029	3.563	3.246	3.818	3.512	4.132	3.119	3.67	ns

**Table 95 • HSTL DC Output Voltage Specification Applicable to DDRIO I/O Bank Only**

Parameter	Symbol	Min	Max	Unit
<b>HSTL Class I</b>				
DC output logic high	$V_{OH}$	$V_{DDI} - 0.4$		V
DC output logic low	$V_{OL}$		0.4	V
Output minimum source DC current (MSIO and DDRIO I/O banks)	$I_{OH}$ at $V_{OH}$	-8.0		mA
Output minimum sink current (MSIO and DDRIO I/O banks)	$I_{OL}$ at $V_{OL}$	8.0		mA
<b>HSTL Class II</b>				
DC output logic high	$V_{OH}$	$V_{DDI} - 0.4$		V
DC output logic low	$V_{OL}$		0.4	V
Output minimum source DC current	$I_{OH}$ at $V_{OH}$	-16.0		mA
Output minimum sink current	$I_{OL}$ at $V_{OL}$	16.0		mA

**Table 96 • HSTL DC Differential Voltage Specification**

Parameter	Symbol	Min	Unit
DC input differential voltage	$V_{ID}$ (DC)	0.2	V

**Table 97 • HSTL AC Differential Voltage Specifications**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	$V_{DIFF}$	0.4		V
AC differential cross point voltage	$V_x$	0.68	0.9	V

**Table 98 • HSTL Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	$D_{MAX}$	400	Mbps	AC loading: per JEDEC specifications

**Table 99 • HSTL Impedance Specification**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	$R_{REF}$	25.5, 47.8	$\Omega$	Reference resistance = 191 $\Omega$
Effective impedance value (ODT for DDRIO I/O bank only)	$R_{TT}$	47.8	$\Omega$	Reference resistance = 191 $\Omega$

**Table 107 • SSTL2 AC Differential Voltage Specifications**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	$V_{DIFF} (AC)$	0.7		V
AC differential cross point voltage	$V_x (AC)$	$0.5 \times V_{DDI} - 0.2$	$0.5 \times V_{DDI} + 0.2$	V

**Table 108 • SSTL2 Minimum and Maximum AC Switching Speeds**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	$D_{MAX}$	400	Mbps	AC loading: per JEDEC specifications
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	575	Mbps	AC loading: 17pF load
Maximum data rate (for MSIOD I/O bank)	$D_{MAX}$	700	Mbps	AC loading: 3 pF / 50 $\Omega$ load
		510	Mbps	AC loading: 17pF load

**Table 109 • SSTL2 AC Impedance Specifications**

Parameter	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	20, 42	$\Omega$	Reference resistor = 150 $\Omega$

**Table 110 • DDR1/SSTL2 AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	1.25	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Reference resistance for data test path for SSTL2 Class I ( $T_{DP}$ )	$R_{TT\_TEST}$	50	$\Omega$
Reference resistance for data test path for SSTL2 Class II ( $T_{DP}$ )	$R_{TT\_TEST}$	25	$\Omega$
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

**Table 111 • SSTL2 Receiver Characteristics for DDRIO I/O Bank (Input Buffers)**

	On-Die Termination (ODT)	$T_{PY}$		Unit
		-1	-Std	
Pseudo differential	None	1.549	1.821	ns
True differential	None	1.589	1.87	ns

**Table 118 • DDR1/SSTL2 Class II Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.29	2.693	1.988	2.338	1.978	2.326	1.989	2.34	1.979	2.328	ns
Differential	2.418	2.846	2.304	2.711	2.297	2.702	2.131	2.506	2.124	2.499	ns

**2.3.6.4 Stub-Series Terminated Logic 1.8 V (SSTL18)**

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification****Table 119 • SSTL18 DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	1.71	1.8	1.89	V
Termination voltage	$V_{TT}$	0.838	0.900	0.964	V
Input reference voltage	$V_{REF}$	0.838	0.900	0.964	V

**Table 120 • SSTL18 DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}$ (DC)	$V_{REF} + 0.125$	1.89	V
DC input logic low	$V_{IL}$ (DC)	-0.3	$V_{REF} - 0.125$	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 121 • SSTL18 DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
<b>SSTL18 Class I (DDR2 Reduced Drive)</b>				
DC output logic high	$V_{OH}$	$V_{TT} + 0.603$		V
DC output logic low	$V_{OL}$		$V_{TT} - 0.603$	V
Output minimum source DC current (DDRIO I/O bank only)	$I_{OH}$ at $V_{OH}$	6.5		mA
Output minimum sink current (DDRIO I/O bank only)	$I_{OL}$ at $V_{OL}$	-6.5		mA
<b>SSTL18 Class II (DDR2 Full Drive)<sup>1</sup></b>				
DC output logic high	$V_{OH}$	$V_{TT} + 0.603$		V
DC output logic low	$V_{OL}$		$V_{TT} - 0.603$	V
Output minimum source DC current (DDRIO I/O bank only)	$I_{OH}$ at $V_{OH}$	13.4		mA
Output minimum sink current (DDRIO I/O bank only)	$I_{OL}$ at $V_{OL}$	-13.4		mA

1. To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$ .

**Table 210 • RSDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.855	3.359	ns
100	2.85	3.353	ns

**Table 211 • RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.602	3.061	ns
100	2.597	3.055	ns

**Table 212 • RSDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.097	2.467	2.303	2.709	2.291	2.695	1.961	2.307	1.947	2.29	ns

**Table 213 • RSDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
No pre-emphasis	1.614	1.899	1.559	1.834	1.55	1.823	1.59	1.87	1.575	1.852	ns
Min pre-emphasis	1.604	1.887	1.742	2.05	1.728	2.032	1.889	2.222	1.858	2.185	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

**2.3.7.6 LVPECL**

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

**Minimum and Maximum Input and Output Levels (Applicable to MSIO I/O Bank Only)**

**Table 214 • LVPECL Recommended DC Operating Conditions**

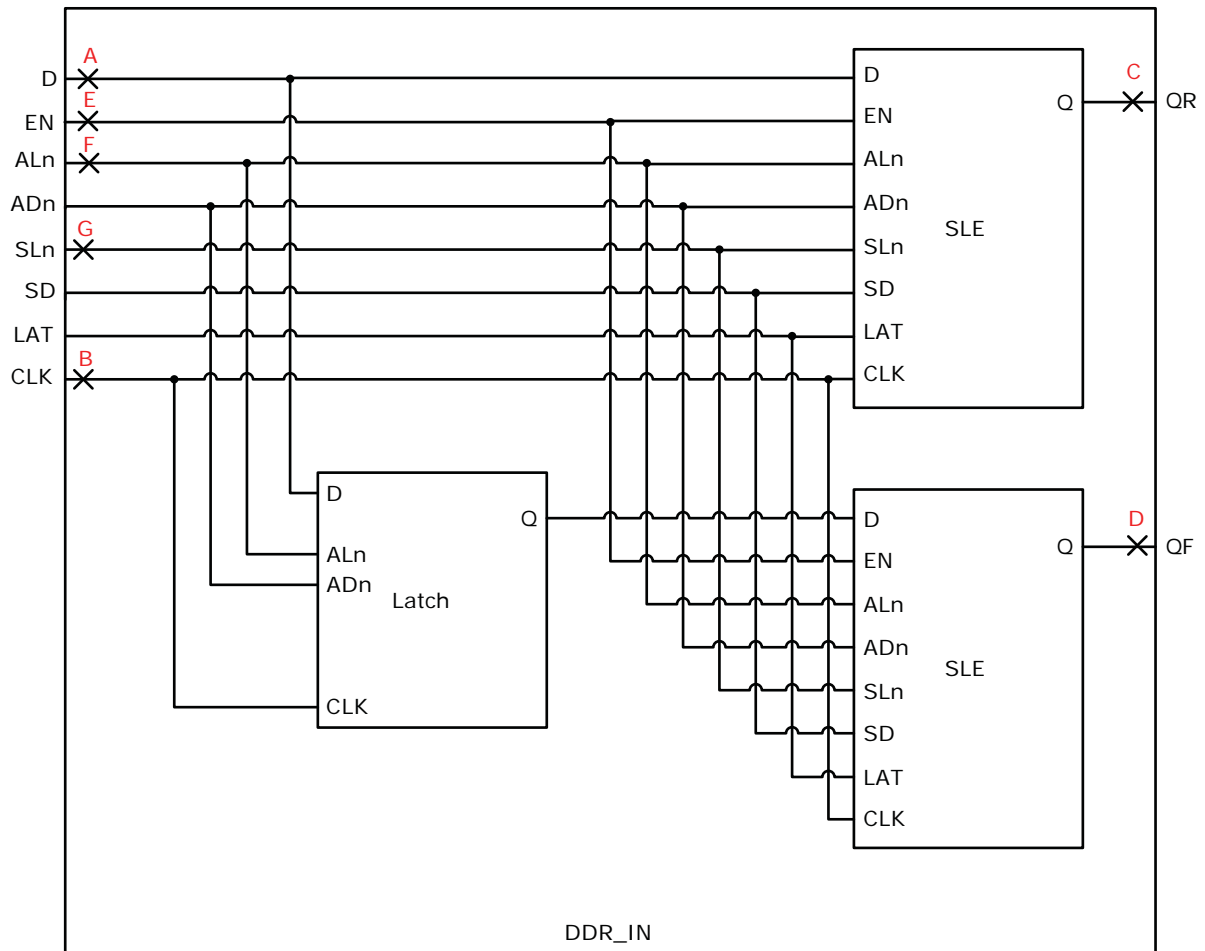
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	3.15	3.3	3.45	V

### 2.3.9 DDR Module Specification

This section describes input and output DDR module and timing specifications.

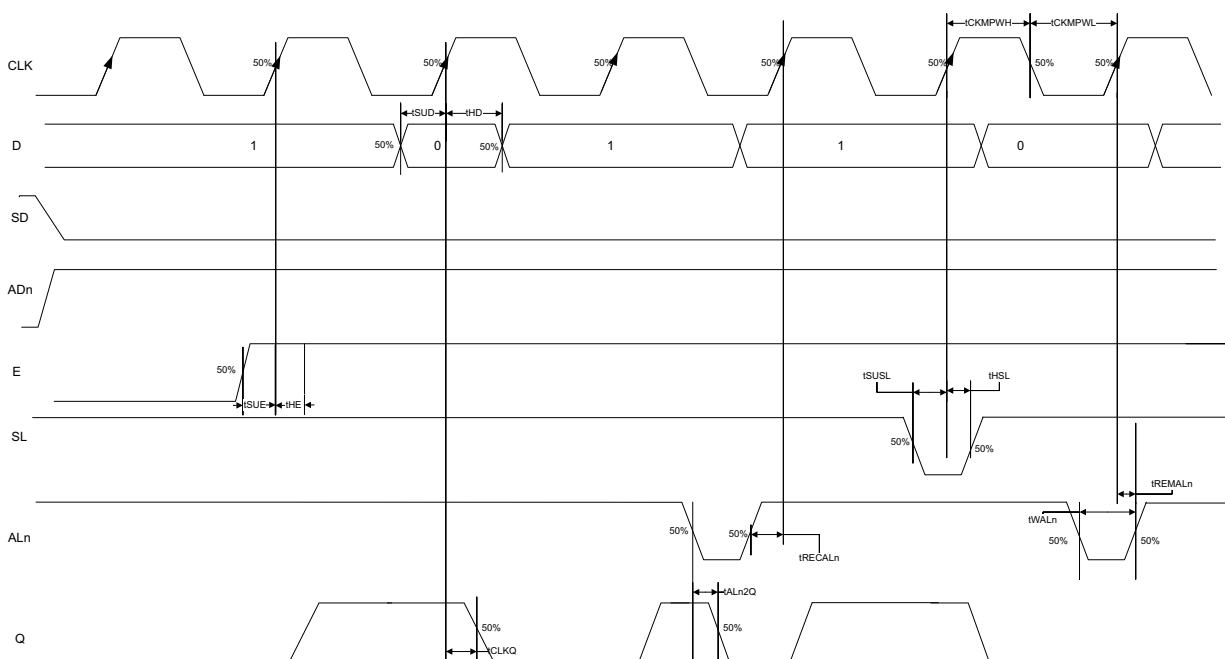
#### 2.3.9.1 Input DDR Module

Figure 10 • Input DDR Module



The following figure shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

**Figure 16 • Sequential Module Timing Diagram**



### 2.3.10.3.1 Timing Characteristics

The following table lists the register delays in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 224 • Register Delays**

Parameter	Symbol	-1	-Std	Unit
Clock-to-Q of the core register	$T_{CLKQ}$	0.108	0.127	ns
Data setup time for the core register	$T_{SUD}$	0.254	0.298	ns
Data hold time for the core register	$T_{HD}$	0	0	ns
Enable setup time for the core register	$T_{SUE}$	0.335	0.394	ns
Enable hold time for the core register	$T_{HE}$	0	0	ns
Synchronous load setup time for the core register	$T_{SUSL}$	0.335	0.394	ns
Synchronous load hold time for the core register	$T_{HSL}$	0	0	ns
Asynchronous Clear-to-Q of the core register (ADn = 1)	$T_{ALn2Q}$	0.473	0.556	ns
Asynchronous preset-to-Q of the core register (ADn = 0)		0.451	0.531	ns
Asynchronous load removal time for the core register	$T_{RECALN}$	0	0	ns
Asynchronous load recovery time for the core register	$T_{RECALN}$	0.353	0.415	ns
Asynchronous load minimum pulse width for the core register	$T_{WALN}$	0.266	0.313	ns
Clock minimum pulse width high for the core register	$T_{CKMPWH}$	0.065	0.077	ns
Clock minimum pulse width low for the core register	$T_{CKMPWL}$	0.139	0.164	ns



The following table lists the 010 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 229 • 010 Device Global Resource**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	$T_{RCKL}$	0.626	0.669	0.627	0.668	ns
Input high delay for global clock	$T_{RCKH}$	1.112	1.182	1.308	1.393	ns
Maximum skew for global clock	$T_{RCKSW}$		0.07		0.085	ns

The following table lists the 005 device global resources in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 230 • 005 Device Global Resource**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	$T_{RCKL}$	0.625	0.66	0.628	0.66	ns
Input high delay for global clock	$T_{RCKH}$	1.126	1.187	1.325	1.397	ns
Maximum skew for global clock	$T_{RCKSW}$		0.061		0.072	ns

## 2.3.12 FPGA Fabric SRAM

See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for more information.

### 2.3.12.1 FPGA Fabric Large SRAM (LSRAM)

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 1K × 18 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 231 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Clock period	$T_{CY}$	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	$T_{PLCY}$	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register				0.334	0.393	ns
Read access time without pipeline register	$T_{CLK2Q}$			2.273	2.674	ns
Access time with feed-through write timing				1.529	1.799	ns
Address setup time	$T_{ADDRSU}$	0.441		0.519		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.341		0.401		ns
Data hold time	$T_{DHD}$	0.107		0.126		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns

**Table 238 •  $\mu$ SRAM (RAM64x16) in 64 x 16 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read synchronous reset hold time	$T_{SRSTHD}$	0.061		0.071		ns
Write clock period	$T_{CCY}$	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	$T_{BLKCSU}$	0.404		0.476		ns
Write block hold time	$T_{BLKCHD}$	0.007		0.008		ns
Write input data setup time	$T_{DINCSU}$	0.115		0.135		ns
Write input data hold time	$T_{DINCHD}$	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.026		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

The following table lists the  $\mu$ SRAM in 128 x 9 mode in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 239 •  $\mu$ SRAM (RAM128x9) in 128 x 9 Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	$T_{CY}$	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	$T_{PLCY}$	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	$T_{CLK2Q}$		0.266		0.313	ns
Read access time without pipeline register				1.677		1.973
Read address setup time in synchronous mode	$T_{ADDRSU}$	0.301		0.354		ns
Read address setup time in asynchronous mode			1.856		2.184	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.091		0.107		ns
Read address hold time in asynchronous mode			-0.778		-0.915	
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHD}$	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.036		2.396	ns

**Table 262 • SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

<b>M2S/M2GL Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	302672	6	41	8	Sec
010	568784	10	48	14	Sec
025	1223504	21	61	29	Sec
050	2424832	39	82	50	Sec
060	2418896	44	87	54	Sec
090	3645968	66	112	79	Sec
150	6139184	108	162	128	Sec

**Table 263 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

<b>M2S/M2GL Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	137536	3	64	4	Sec
010	274816	4	104	7	Sec
025	274816	4	104	8	Sec
050	2,78,528	4	102	8	Sec
060	268480	6	102	8	Sec
090	544496	10	179	15	Sec
150	544496	10	180	15	Sec

**Table 264 • SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

<b>M2S/M2GL Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	439296	9	83	11	Sec
010	842688	15	129	21	Sec
025	1497408	26	143	35	Sec
050	2695168	43	163	55	Sec
060	2686464	48	165	60	Sec
090	4190208	75	266	91	Sec
150	6682768	117	318	141	Sec

**Table 265 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	69	49	50	Sec
010	99	57	57	Sec
025	150	64	63	Sec
050	55 <sup>1</sup>	Not Supported	Not Supported	Sec
060	313	105	104	Sec
090	449	131	130	Sec
150	730	179	183	Sec

1. Auto programming in 050 device is done through SC\_SPI, and SPI CLK is set to 6.25 MHz.

**Table 266 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	63	70	71	Sec
010	108	109	109	Sec
025	109	107	108	Sec
050	107	Not Supported	Not Supported	Sec
060	100	108	108	Sec
090	176	184	184	Sec
150	183	183	183	Sec

**Table 267 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	109	89	88	Sec
010	183	135	135	Sec
025	251	142	143	Sec
050	134	Not Supported	Not Supported	Sec
060	390	183	180	Sec
090	604	283	282	Sec
150	889	331	332	Sec

**Table 303 • I2C Characteristics (continued)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Maximum data rate	$D_{MAX}$			400	Kbps	Fast mode
				100	Kbps	Standard mode
Pulse width of spikes which must be suppressed by the input filter	$T_{FILT}$		50		ns	Fast mode

1. These values are provided for MSIO Bank–LVTTTL 8 mA Low Drive at 25 °C, typical conditions. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on  $V_{DDIX}$ , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
3.  $R(PULL-DOWN-MAX) = (VOLspec)/IOLspec$ .
4.  $R(PULL-UP-MAX) = (VDDImax-VOHspec)/IOHspec$ .

The following table lists the I<sup>2</sup>C switching characteristics in worst-case industrial conditions when  $T_J = 100\text{ °C}$ ,  $V_{DD} = 1.14\text{ V}$

**Table 304 • I2C Switching Characteristics**

Parameter	Symbol	-1		Unit
		Min	Min	
Low period of I2C_x_SCL	$T_{LOW}$	1	1	PCLK cycles
High period of I2C_x_SCL	$T_{HIGH}$	1	1	PCLK cycles
START hold time	$T_{HD;STA}$	1	1	PCLK cycles
START setup time	$T_{SU;STA}$	1	1	PCLK cycles
DATA hold time	$T_{HD;DAT}$	1	1	PCLK cycles
DATA setup time	$T_{SU;DAT}$	1	1	PCLK cycles
STOP setup time	$T_{SU;STO}$	1	1	PCLK cycles

**Figure 21 • I<sup>2</sup>C Timing Parameter Definition**

