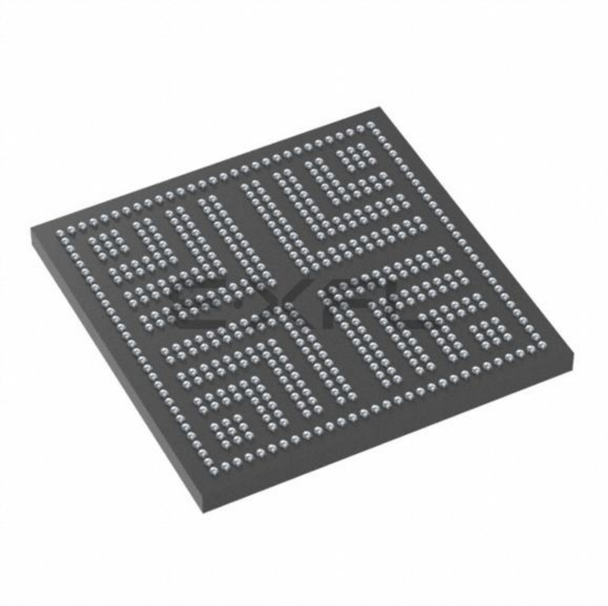

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 150K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	536-LFBGA, CSPBGA
Supplier Device Package	536-CSPBGA (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s150-fcsg536

1. For flash programming and retention maximum limits, see Table 5, page 7. For recommended operating conditions, see Table 4, page 6.

Table 4 • **Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Operating junction temperature	T_J	0	25	85	°C	Commercial
		–40	25	100	°C	Industrial
Programming junction temperatures[1]	T_J	0	25	85	°C	Commercial
		–40	25	100	°C	Industrial
DC core supply voltage. Must always power this pin.	V_{DD}	1.14	1.2	1.26	V	
Power supply for charge pumps (for normal operation and programming) for the 005, 010, 025, 050, 060 devices	V_{PP}	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Power supply for charge pumps (for normal operation and programming) for the 090 and 150 devices	V_{PP}	3.15	3.3	3.45	V	3.3 V range
Analog power pad for MDDR PLL	MSS_MDDR_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for MDDR PLL	HPMS_MDDR_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for FDDR PLL	FDDR_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for MDDR PLL	PLL0_PLL1_MSS_MDDR_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for MDDR PLL	PLL0_PLL1_HPMS_MDDR_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power pad for PLL0 to PLL5	CCC_XX[01]_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
High supply voltage for PLL SerDes[01]	SERDES_[01]_PLL_VDDA	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range
Analog power for SerDes[01] PLL Lane 0 to Lane 3. This is a 2.5 V SerDes internal PLL supply.	SERDES_[01]_L[0123]_VDDAPLL	2.375	2.5	2.625	V	
TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply.	SERDES_[01]_L[0123]_VDDAIO	1.14	1.2	1.26	V	
PCIe/PCS power supply	SERDES_[01]_VDD	1.14	1.2	1.26	V	
1.2 V DC supply voltage	V_{DDIx}	1.14	1.2	1.26	V	
1.5 V DC supply voltage	V_{DDIx}	1.425	1.5	1.575	V	
1.8 V DC supply voltage	V_{DDIx}	1.71	1.8	1.89	V	
2.5 V DC supply voltage	V_{DDIx}	2.375	2.5	2.625	V	

Table 9 • **Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices *(continued)***

Device	Still Air	1.0 m/s	2.5 m/s	θ_{JB}	θ_{JC}	Unit
	θ_{JA}					
150						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W
FCS536	15.01	12.06	10.76	3.69	1.55	°C/W
FCV484	16.21	13.11	11.84	6.73	0.10	°C/W

2.3.1.2.1 Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in the actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package with another.

The maximum power dissipation allowed is calculated using EQ4.

$$\text{Maximum power allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100 °C. EQ5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where:

θ_{JA} = 14.7 °C/W (taken from Table 9, page 10).

T_A = 85 °C

$$\text{Maximum power allowed} = \frac{100\ °C - 85\ °C}{14.7\ °C/W} = 1.088\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink may be attached to the top of the case, or the airflow inside the system must be increased.

2.3.1.2.2 Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from the junction to the board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

2.3.1.2.3 Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable to packages used with external heat sinks. Constant temperature is applied to the surface, which acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

2.3.1.3 ESD Performance

See *RT0001: Microsemi Corporation - SoC Products Reliability Report* for information about ESD.

Table 46 • **LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers) *(continued)***

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	Unit
4 mA	Slow	3.095	3.641	2.705	3.182	3.088	3.633	4.738	5.575	4.348	5.116	ns
	Medium	2.825	3.324	2.488	2.927	2.823	3.321	4.492	5.285	4.063	4.781	ns
	Medium fast	2.701	3.178	2.384	2.804	2.698	3.173	4.364	5.135	3.945	4.642	ns
	Fast	2.69	3.165	2.377	2.796	2.687	3.161	4.359	5.129	3.94	4.636	ns
6 mA	Slow	2.919	3.434	2.491	2.93	2.902	3.414	5.085	5.983	4.674	5.5	ns
	Medium	2.65	3.118	2.279	2.681	2.642	3.108	4.845	5.701	4.375	5.148	ns
	Medium fast	2.529	2.975	2.176	2.56	2.521	2.965	4.724	5.558	4.259	5.011	ns
	Fast	2.516	2.96	2.168	2.551	2.508	2.95	4.717	5.55	4.251	5.002	ns
8 mA	Slow	2.863	3.368	2.427	2.855	2.844	3.346	5.196	6.114	4.769	5.612	ns
	Medium	2.599	3.058	2.217	2.608	2.59	3.047	4.952	5.827	4.471	5.261	ns
	Medium fast	2.483	2.921	2.114	2.487	2.473	2.91	4.832	5.685	4.364	5.134	ns
	Fast	2.467	2.902	2.106	2.478	2.457	2.89	4.826	5.678	4.348	5.116	ns
12 mA	Slow	2.747	3.232	2.296	2.701	2.724	3.204	5.39	6.342	4.938	5.81	ns
	Medium	2.493	2.934	2.102	2.473	2.483	2.921	5.166	6.078	4.65	5.471	ns
	Medium fast	2.382	2.803	2.006	2.36	2.371	2.789	5.067	5.962	4.546	5.349	ns
	Fast	2.369	2.787	1.999	2.352	2.357	2.773	5.063	5.958	4.538	5.339	ns
16 mA	Slow	2.677	3.149	2.213	2.604	2.649	3.116	5.575	6.56	5.08	5.977	ns
	Medium	2.432	2.862	2.028	2.386	2.421	2.848	5.372	6.32	4.801	5.649	ns
	Medium fast	2.324	2.734	1.937	2.278	2.311	2.718	5.297	6.233	4.7	5.531	ns
	Fast	2.313	2.721	1.929	2.269	2.3	2.706	5.296	6.231	4.699	5.529	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 47 • **LVCMOS 2.5 V Transmitter Characteristics for MSIO Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	Unit
2 mA	Slow	3.48	4.095	3.855	4.534	3.785	4.453	2.12	2.494	3.45	4.059	ns
4 mA	Slow	2.583	3.039	3.042	3.579	3.138	3.691	4.143	4.874	4.687	5.513	ns
6 mA	Slow	2.392	2.815	2.669	3.139	2.82	3.317	4.909	5.775	5.083	5.98	ns
8 mA	Slow	2.309	2.717	2.565	3.017	2.74	3.223	5.812	6.837	5.523	6.497	ns
12 mA	Slow	2.333	2.745	2.437	2.867	2.626	3.089	6.131	7.213	5.712	6.72	ns
16 mA	Slow	2.412	2.838	2.335	2.747	2.533	2.979	6.54	7.694	6.007	7.067	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 82 • LVCMOS 1.2 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

	T_{PY}		T_{PYS}		
On-Die Termination (ODT)	**–1**	**–Std**	**–1**	**–Std**	**Unit**
None	4.154	4.887	4.114	4.84	ns
50	6.918	8.139	6.806	8.008	ns
75	5.613	6.603	5.533	6.509	ns
150	4.716	5.549	4.657	5.479	ns

Table 83 • LVCMOS 1.2 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		Unit
		–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	
2 mA	Slow	6.713	7.897	5.362	6.308	6.723	7.909	7.233	8.51	6.375	7.499	ns
	Medium	5.912	6.955	4.616	5.43	5.915	6.959	6.887	8.102	6.009	7.069	ns
	Medium fast	5.5	6.469	4.231	4.978	5.5	6.471	6.672	7.849	5.835	6.865	ns
	Fast	5.462	6.426	4.194	4.935	5.463	6.427	6.646	7.819	5.828	6.857	ns
4 mA	Slow	6.109	7.186	4.708	5.539	6.098	7.174	8.005	9.418	7.033	8.274	ns
	Medium	5.355	6.299	4.034	4.746	5.338	6.28	7.637	8.985	6.672	7.849	ns
	Medium fast	4.953	5.826	3.685	4.336	4.932	5.802	7.44	8.752	6.499	7.646	ns
	Fast	4.911	5.777	3.658	4.303	4.89	5.754	7.427	8.737	6.488	7.632	ns
6 mA	Slow	5.89	6.929	4.506	5.301	5.874	6.911	8.337	9.808	7.315	8.605	ns
	Medium	5.176	6.089	3.862	4.543	5.155	6.065	7.986	9.394	6.943	8.168	ns
	Medium fast	4.792	5.637	3.523	4.145	4.765	5.606	7.808	9.186	6.775	7.97	ns
	Fast	4.754	5.593	3.486	4.101	4.728	5.563	7.777	9.149	6.769	7.963	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 84 • LVCMOS 1.2 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		Unit
		–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	
2 mA	Slow	6.746	7.937	7.458	8.774	8.172	9.614	9.867	11.608	8.393	9.874	ns
4 mA	Slow	7.068	8.315	6.678	7.857	7.474	8.793	10.986	12.924	9.043	10.638	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 95 • **HSTL DC Output Voltage Specification Applicable to DDRIO I/O Bank Only**

Parameter	Symbol	Min	Max	Unit
	HSTL Class I			
DC output logic high	V_{OH}	V_{DDI} – 0.4		V
DC output logic low	V_{OL}		0.4	V
Output minimum source DC current (MSIO and DDRIO I/O banks)	I_{OH} at V_{OH}	–8.0		mA
Output minimum sink current (MSIO and DDRIO I/O banks)	I_{OL} at V_{OL}	8.0		mA
	HSTL Class II			
DC output logic high	V_{OH}	V_{DDI} – 0.4		V
DC output logic low	V_{OL}		0.4	V
Output minimum source DC current	I_{OH} at V_{OH}	–16.0		mA
Output minimum sink current	I_{OL} at V_{OL}	16.0		mA

Table 96 • **HSTL DC Differential Voltage Specification**

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID} (DC)	0.2	V

Table 97 • **HSTL AC Differential Voltage Specifications**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF}	0.4		V
AC differential cross point voltage	V_x	0.68	0.9	V

Table 98 • **HSTL Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	400	Mbps	AC loading: per JEDEC specifications

Table 99 • **HSTL Impedance Specification**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	R_{REF}	25.5, 47.8	Ω	Reference resistance = 191 Ω
Effective impedance value (ODT for DDRIO I/O bank only)	R_{TT}	47.8	Ω	Reference resistance = 191 Ω

Table 100 • **HSTL AC Test Parameter Specification**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.75	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for HSTL15 Class I (T_{DP})	RTT_TEST	50	Ω
Reference resistance for data test path for HSTL15 Class II (T_{DP})	RTT_TEST	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst-case commercial conditions: T_J = 85 °C, V_{DD} = 1.14 V, worst-case V_{DDI}.

Table 101 • **HSTL Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)**

		T_{PY}		
	On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
Pseudo differential	None	1.605	1.888	ns
	47.8	1.614	1.898	ns
True differential	None	1.622	1.909	ns
	47.8	1.628	1.916	ns

Table 102 • **HSTL Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
	–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
HSTL Class I											
Single-ended	2.6	3.059	2.514	2.958	2.514	2.958	2.431	2.86	2.431	2.86	ns
Differential	2.621	3.083	2.648	3.115	2.647	3.113	2.925	3.442	2.923	3.44	ns
HSTL Class II											
Single-ended	2.511	2.954	2.488	2.927	2.49	2.93	2.409	2.833	2.411	2.836	ns
Differential	2.528	2.974	2.552	3.003	2.551	3.001	2.897	3.409	2.896	3.408	ns

2.3.6.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V.

Table 210 • **RSDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.855	3.359	ns
100	2.85	3.353	ns

Table 211 • **RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.602	3.061	ns
100	2.597	3.055	ns

Table 212 • **RSDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
2.097	2.467	2.303	2.709	2.291	2.695	1.961	2.307	1.947	2.29	ns

Table 213 • **RSDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
	–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
No pre-emphasis	1.614	1.899	1.559	1.834	1.55	1.823	1.59	1.87	1.575	1.852	ns
Min pre-emphasis	1.604	1.887	1.742	2.05	1.728	2.032	1.889	2.222	1.858	2.185	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

2.3.7.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

Minimum and Maximum Input and Output Levels (Applicable to MSIO I/O Bank Only)

Table 214 • **LVPECL Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

Table 222 • **Output DDR Propagation Delays *(continued)***

Symbol	Description	Measuring Nodes (from, to)	–1	–Std	Unit
$T_{DDROWAL}$	Asynchronous load minimum pulse width for output DDR	C, C	0.304	0.357	ns
$T_{DDROCKMPWH}$	Clock minimum pulse width high for the output DDR	E, E	0.075	0.088	ns
$T_{DDROCKMPWL}$	Clock minimum pulse width low for the output DDR	E, E	0.159	0.187	ns

2.3.10 Logic Element Specifications

2.3.10.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, see *SmartFusion2 and IGLOO2 Macro Library Guide*.

Figure 14 • **LUT-4**

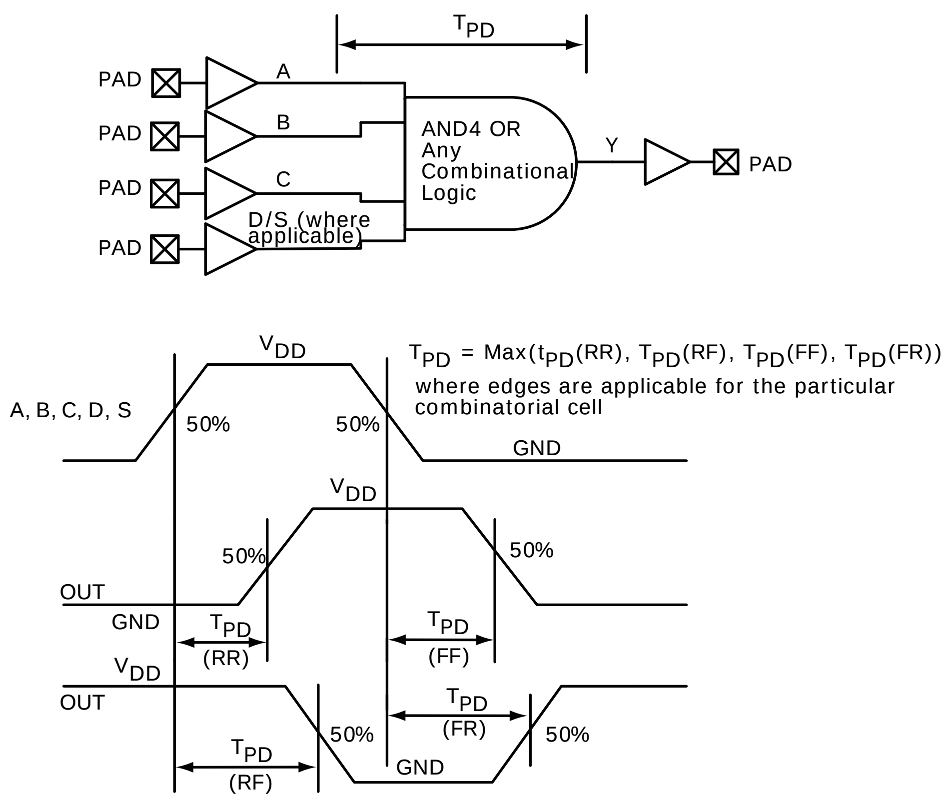


Table 233* • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4 *(continued)

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register	T_{CLK2Q}		0.323		0.38	ns
Read access time without pipeline register			2.273		2.673	ns
Access time with feed-through write timing			1.511		1.778	ns
Address setup time	T_{ADDRSU}	0.543		0.638		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.334		0.393		ns
Data hold time	T_{DHD}	0.082		0.096		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		1.511		1.778	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.516		0.607		ns
Read enable hold time	T_{RDEHD}	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}		1.507		1.773	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.458		0.539		ns
Write enable hold time	T_{WEHD}	0.048		0.057		ns
Maximum frequency	F_{MAX}		400		340	MHz

Table 243 • **µSRAM (RAM1024x1) in 1024 × 1 Mode *(continued)***

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.83		0.98	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.003		0.004		ns
Write input data hold time	T_{DINCHD}	0.137		0.161		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.247		0.29		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.03		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

2.3.13 Programming Times

The following tables list the programming times in typical conditions when T_J = 25 °C, V_{DD} = 1.2 V. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 244 • **JTAG Programming (Fabric Only)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	302672	22	10	Sec
010	568784	28	18	Sec
025	1223504	51	26	Sec
050	2424832	66	54	Sec
060	2418896	77	54	Sec
090	3645968	113	126	Sec
150	6139184	155	193	Sec

Table 251 • **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only) *(continued)***

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
150	544496	10	158	15	Sec

Table 252 • **SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	9	61	11	Sec
010	842688	15	107	21	Sec
025	1497408	26	121	35	Sec
050	2695168	43	141	55	Sec
060	2686464	48	143	60	Sec
090	4190208	75	244	91	Sec
150	6682768	117	296	141	Sec

Table 253 • **Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	
	100 kHz	25 MHz	12.5 MHz	Unit
005	47	27	28	Sec
010	77	35	35	Sec
025	150	42	41	Sec
050	33[1]	Not Supported	Not Supported	Sec
060	291	83	82	Sec
090	427	109	108	Sec
150	708	157	160	Sec

1. Auto Programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

Table 254 • **Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)**

M2S/M2GL Device	Auto Programming	Auto Update	Programming Recovery	
	100 kHz	25 MHz	12.5 MHz	Unit
005	41	48	49	Sec
010	86	87	87	Sec
025	87	85	86	Sec
050	85	Not Supported	Not Supported	Sec
060	78	86	86	Sec
090	154	162	162	Sec

The following table lists the programming times in worst-case conditions when T_J = 100 °C, V_{DD} = 1.14 V. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 256 • **JTAG Programming (Fabric Only)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	302672	44	10	Sec
010	568784	50	18	Sec
025	1223504	73	26	Sec
050	2424832	88	54	Sec
060	2418896	99	54	Sec
090	3645968	135	126	Sec
150	6139184	177	193	Sec

Table 257 • **JTAG Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	137536	61	4	Sec
010	274816	100	9	Sec
025	274816	100	9	Sec
050	2,78,528	106	8	Sec
060	268480	98	8	Sec
090	544496	176	15	Sec
150	544496	177	15	Sec

Table 258 • **JTAG Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Program	Verify	Unit
005	439296	71	11	Sec
010	842688	129	20	Sec
025	1497408	142	35	Sec
050	2695168	184	59	Sec
060	2686464	180	70	Sec
090	4190208	288	147	Sec
150	6682768	338	231	Sec

2.3.16 SRAM PUF

For more details on static random-access memory (SRAM) physical unclonable functions (PUF) services, see *AC434: Using SRAM PUF System Service in SmartFusion2 Application Note*.

The following table lists the SRAM PUF in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 274 • **SRAM PUF**

	PUF Off		PUF On		
Service	**Typ**	**Max**	**Typ**	**Max**	**Unit**
Create activation code	709.1	746.4	754.4	762.5	ms
Delete activation code	1329.3	1399.3	1414.1	1429.3	ms
Create intrinsic keycode	656.6	691.1	698.5	706.0	ms
Create extrinsic keycode	656.6	691.1	698.5	706.0	ms
Get number of keys	1.3	1.4	1.4	1.4	ms
Export (Kc0, Kc1)	998.0	1050.5	1061.7	1073.1	ms
Export 2 keycodes	2020.2	2126.5	2149.2	2172.3	ms
Export 4 keycodes	3065.7	3227.0	3261.3	3296.4	ms
Export 8 keycodes	5101.0	5369.5	5426.6	5485.0	ms
Export 16 keycodes	9212.1	9697.0	9800.1	9905.5	ms
Import (Kc0, Kc1)	39.7	41.8	42.2	42.7	ms
Import 2 keycodes	50.1	52.7	53.3	53.9	ms
Import 4 keycodes	60.6	63.8	64.5	65.2	ms
Import 8 keycodes	80.9	85.1	86.1	87.0	ms
Import 16 keycodes	123.8	130.4	131.7	133.2	ms
Delete keycode	552.5	581.6	587.8	594.1	ms
Fetch key	31.4	33.0	33.4	33.7	ms
Fetch ecc key	20.0	21.1	21.3	21.5	ms
Get seed	2.0	2.1	2.2	2.2	ms

Table 276 • Cryptographic Block Characteristics *(continued)*

Service	Conditions	Timing	Unit
SHA256	512 bits	540	kbps
	1024 bits	780	kbps
	2048 bits	950	kbps
	24 kbits	1140	kbps
HMAC	512 bytes	820	kbps
	1024 bytes	890	kbps
	2048 bytes	930	kbps
	24 kbytes	980	kbps
KeyTree		1.8	ms
Challenge-response	PUF = OFF	25	ms
	PUF = ON	7	ms
ECC point multiplication		590	ms
ECC point addition		8	ms

1. Using cypher block chaining (CBC) mode.

2.3.19 Crystal Oscillator

The following table describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

Table 277 • Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		20		MHz	
Accuracy	ACCXTAL			0.0047	%	005, 010, 025, 050, 060, and 090 devices
				0.0058	%	150 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		200	300	ps	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		200	300	ps	010, 025, 050, and 060 devices
			250	410	ps	150 devices
			250	550	ps	005 and 090 devices
Operating current	IDYNXTAL		1.5		mA	010, 050, and 060 devices
			1.65		mA	005, 025, 090, and 150 devices
Input logic level high	VIHXTAL	0.9 V_{PP}			V	
Input logic level low	VILXTAL			0.1 V_{PP}	V	

2.3.20 On-Chip Oscillator

The following tables describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

Table 280 • **Electrical Characteristics of the 50 MHz RC Oscillator**

Parameter	Symbol	Typ	Max	Unit	Condition
Operating frequency	F50RC	50		MHz	
Accuracy	ACC50RC	1	4	%	050 devices
		1	5	%	005, 025, and 060 devices
		1	6.3	%	090 devices
		1	7.1	%	010 and 150 devices
Output duty cycle	CYC50RC	49–51	46.5–53.5	%	
Output jitter (peak to peak)	JIT50RC				Period Jitter
		200	300	ps	005, 010, 050, and 060 devices
		200	400	ps	150 devices
		300	500	ps	025 and 090 devices
					Cycle-to-Cycle Jitter
		200	300	ps	005 and 050 devices
		320	420	ps	010, 060, and 150 devices
		320	850	ps	025 and 090 devices
Operating current	IDYN50RC	6.5		mA	

Table 281 • **Electrical Characteristics of the 1 MHz RC Oscillator**

Parameter	Symbol	Typ	Max	Unit	Condition
Operating frequency	F1RC	1		MHz	
Accuracy	ACC1RC	1	3	%	005, 010, 025, and 050 devices
		1	4.5	%	060, and 150 devices
		1	5.6	%	090 devices
Output duty cycle	CYC1RC	49–51	46.5–53.5	%	005, 010, 025, 050, 090 and 150 devices
		49-51	46.0-54.0	%	060 devices
Output jitter (peak to peak)	JIT1RC				Period Jitter
		10	20	ns	005, 010, 025, and 050 devices
		10	28	ns	060, 090 and 150 devices
					Cycle-to-Cycle Jitter
		10	20	ns	005, 010, and 050 devices
		10	35	ns	025, 060, and 150 devices
		10	45	ns	090 devices
Operating current	IDYN1RC	0.1		mA	
Startup time	SU1RC		17	μs	050, 090, and 150 devices
			18	μs	005, 010, and 025 devices

1. The minimum output clock frequency is limited by the PLL. For more information, see *UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide*.
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance is limited by the CCC output frequency.

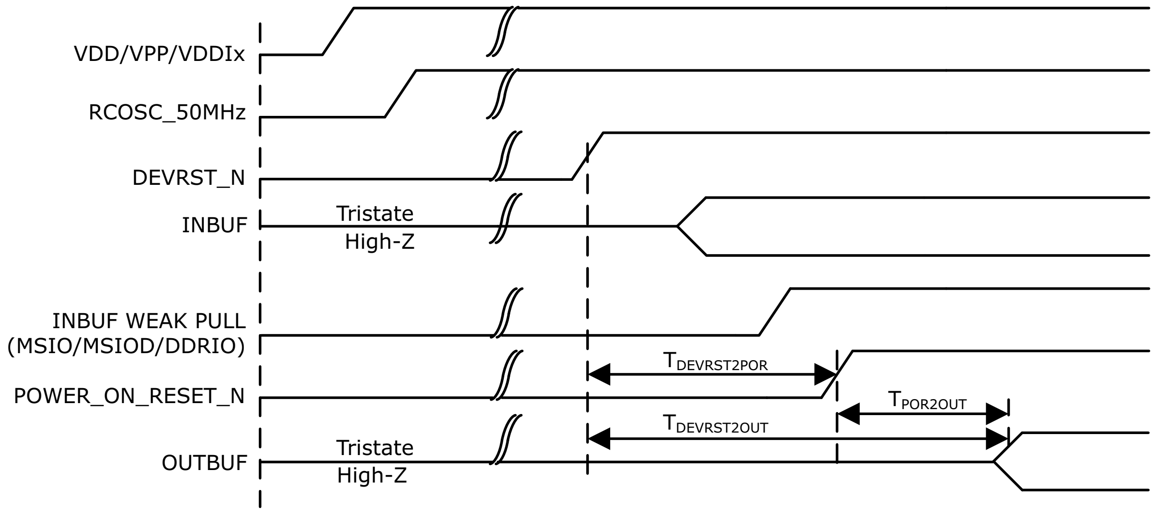
The following table lists the CCC/PLL jitter specifications in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 283 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications**

CCC Output Maximum Peak-to-Peak Period Jitter F_{OUT_CCC}						
Parameter	**Conditions/Package Combinations**					**Unit**
10 FG484, 050 FG896/FG484/FCS325 Packages[1]	SSO = 0	0 < SSO <= 2	SSO <= 4	SSO <= 8	SSO <= 16	
20 MHz to 100 MHz	Max(110, ± 1% x $(1/F_{OUT\_CCC})$)	Max(150, ± 1% x $(1/F_{OUT\_CCC})$)				ps
100 MHz to 400 MHz	Max(120, ± 1% x $(1/F_{OUT\_CCC})$)	Max(150, ± 1% x $(1/F_{OUT\_CCC})$)			Max(170, ± 1% x $(1/F_{OUT\_CCC})$)	ps
025 FG484/FCS325 Package[1]	0 < SSO <=16					
20 MHz to 74 MHz	± 1% x $(1/F_{OUT\_CCC})$)					ps
74 MHz to 400 MHz	210					ps
005 FG484 Package[1]	0 < SSO <=16					
20 MHz to 53 MHz	± 1% x $(1/F_{OUT\_CCC})$)					ps
53 MHz to 400 MHz	270					ps
090 FG676 and FC325 Package[1]	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x $(1/F_{OUT\_CCC})$)					ps
100 MHz to 400 MHz	150					ps
060 FG676 Package[1]	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x $(1/F_{OUT\_CCC})$					ps
100 MHz to 400 MHz	150					
150 FC1152 Package[1]	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x $(1/F_{OUT\_CCC})$)					ps
100 MHz to 400 MHz	120					ps

1. SSO data is based on LVCMOS 2.5 V MSIO and/or MSIOD bank I/Os.

Figure 20 • **DEVRST_N to Functional Timing Diagram for IGLOO2**



2.3.27 Flash*Freeze Timing Characteristics

The following table lists the Flash*Freeze entry and exit times in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 293 • **Flash*Freeze Entry and Exit Times**

		Entry/Exit Timing FCLK = 100MHz		**Entry/Exit Timing FCLK = 3 MHz**		
Parameter	**Symbol**	**005, 010, 025, 060, 090, and 150**	**050**	**All Devices**	**Unit**	**Conditions**
Entry time	TFF_ENTRY	160	150	320	µs	eNVM and MSS/HPMS PLL = ON
		215	200	430	µs	eNVM and MSS/HPMS PLL= OFF
Exit time with respect to the MSS PLL Lock	TFF_EXIT	100	100	140	µs	eNVM and MSS/HPMS PLL = ON during F*F
		136	120	190	µs	eNVM = ON and MSS/HPMS PLL = OFF during F*F and MSS/HPMS PLL turned back on at exit
		200	200	285	µs	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit
		200	200	285	µs	eNVM = OFF and MSS/HPMS PLL = ON during F*F and eNVM turned back on at exit

The following table lists the receiver pa in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 297 • **Receiver Parameters**

Symbol	Description	Min	Typ	Max	Unit
VRX-IN-PP-CC	Differential input peak-to-peak sensitivity (2.5 Gbps)	0.238		1.2	V
	Differential input peak-to-peak sensitivity (2.5 Gbps, de-emphasized)	0.219		1.2	V
	Differential input peak-to-peak sensitivity (5.0 Gbps)	0.300		1.2	V
	Differential input peak-to-peak sensitivity (5.0 Gbps, de-emphasized)	0.300		1.2	V
VRX-CM-AC-P	Input common mode range (AC coupled)			150	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset			15	μs
RLRX-DIFF	Return loss differential mode (2.5 Gbps)	–10			dB
	Return loss differential mode (5.0 Gbps) 0.05 GHz to 1.25 GHz	–10			dB
	1.25 GHz to 2.5 GHz	–8			dB
RLRX-CM	Return loss common mode (2.5 Gbps, 5.0 Gbps)	–6			dB
RX-CID[1]	CID limit PCIe Gen1/2			200	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65		175	mV

1. AC-coupled, BER = e^{-12}, using synchronous clock.

Table 298 • **SerDes Protocol Compliance**

Protocol	Maximum Data Rate (Gbps)	–1	–Std
PCIe Gen 1	2.5	Yes	Yes
PCIe Gen 2	5.0	Yes	
XAUI	3.125	Yes	
Generic EPCS	3.2	Yes	
Generic EPCS	2.5	Yes	Yes

2.3.31.2 SmartFusion2 Inter-Integrated Circuit (I^2C) Characteristics

This section describes the DC and switching of the I^2C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, see Figure 21, page 125.

The following table lists the I^2C characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V

Table 303 • **I2C Characteristics**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input low voltage	V_{IL}	–0.3		0.8	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive.
Input high voltage	V_{IH}	2		3.45	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive.
Hysteresis of schmitt triggered inputs for V_{DDI} > 2 V	V_{HYS}	0.05 × V_{DDI}			V	See Table 28, page 23 for more information.
Input current high	I_{IL}			10	µA	See Single-Ended I/O Standards, page 24 for more information.
Input current low	I_{IH}			10	µA	See Single-Ended I/O Standards, page 24 for more information.
Input rise time	T_{ir}			1000	ns	Standard mode
				300	ns	Fast mode
Input fall time	T_{if}			300	ns	Standard mode
				300	ns	Fast mode
Maximum output voltage low (open drain) at 3 mA sink current for V_{DDI} > 2 V	V_{OL}			0.4	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive.
Pin capacitance	Cin			10	pF	V_{IN} = 0, f = 1.0 MHz
Output fall time from VIHMin to VILMax[1]	t_{OF}[1]		21.04		ns	V_{IHmin} to V_{ILMax}, CLOAD = 400 pF
			5.556		ns	V_{IHmin} to V_{ILMax}, CLOAD = 100 pF
Output rise time from VILMax to VIHMin[1]	t_{OR}[1]		19.887		ns	V_{ILMax} to V_{IHmin}, CLOAD = 400 pF
			5.218		ns	V_{ILMax} to V_{IHmin}, CLOAD = 100 pF
Output buffer maximum pull-down resistance[2, 3]	$R_{pull-up}$[2,3]			50	Ω	
Output buffer maximum pull-up resistance[2, 4]	$R_{pull-down}$[2,4]			131.25	Ω	

Table 305 • **SPI Characteristics for All Devices *(continued)***

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp5	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS fall time (10%–90%)[1]		2.906		ns	IO Configuration: LVCMOS 2.5 V-8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0|1]_DI setup time[2]	12			ns	
sp9m	SPI_[0|1]_DI hold time[2]	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0|1]_DI setup time[2]	2			ns	
sp9s	SPI_[0|1]_DI hold time[2]	7			ns	
SPI master configuration (applicable for 060, 090, and 150 devices)						
sp6m	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 7.0			ns	
sp7m	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) – 9.5			ns	
sp8m	SPI_[0|1]_DI setup time[2]	15			ns	
sp9m	SPI_[0|1]_DI hold time[2]	–2.5			ns	
SPI slave configuration (applicable for 060, 090, and 150 devices)						
sp6s	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 16.0			ns	
sp7s	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) - 3.5			ns	
sp8s	SPI_[0|1]_DI setup time[2]	3			ns	
sp9s	SPI_[0|1]_DI hold time[2]	2.5			ns	

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. For allowable pclk configurations, see Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.