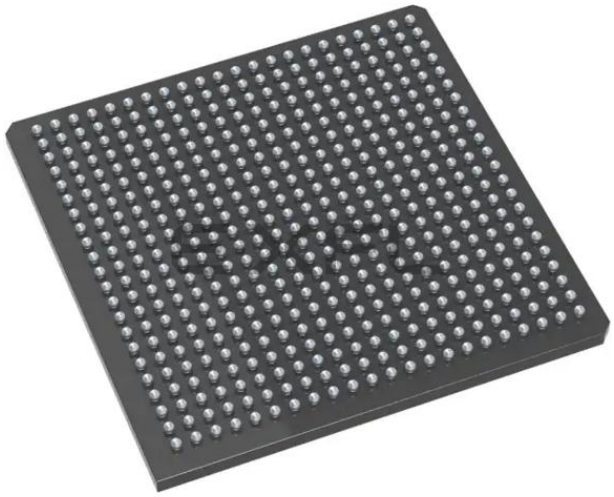

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| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
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| Flash Size | 512KB |
| RAM Size | 64KB |
| Peripherals | DDR, PCIe, SERDES |
| Connectivity | CANbus, Ethernet, I²C, SPI, UART/USART, USB |
| Speed | 166MHz |
| Primary Attributes | FPGA - 150K Logic Modules |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 484-BFBGA |
| Supplier Device Package | 484-FBGA (19x19) |
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# Contents

*Table 9 •* **Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices *(continued)***

| Device | Still Air $\theta_{JA}$ | 1.0 m/s $\theta_{JA}$ | 2.5 m/s $\theta_{JA}$ | $\theta_{JB}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|---|---|---|
| **150** | | | | | | |
| FC1152 | 9.08 | 6.81 | 5.87 | 2.56 | 0.38 | °C/W |
| FCS536 | 15.01 | 12.06 | 10.76 | 3.69 | 1.55 | °C/W |
| FCV484 | 16.21 | 13.11 | 11.84 | 6.73 | 0.10 | °C/W |

#### 2.3.1.2.1 Theta-JA

Junction-to-ambient thermal resistance ($\theta_{JA}$) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in the actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package with another.

The maximum power dissipation allowed is calculated using EQ4.

$$\text{Maximum power allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

*EQ 4*

The absolute maximum junction temperature is 100 °C. EQ5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where:

$\theta_{JA}$ = 14.7 °C/W (taken from Table 9, page 10).

$T_A$ = 85 °C

$$\text{Maximum power allowed} = \frac{100\ °C - 85\ °C}{14.7\ °C/W} = 1.088\ W$$

*EQ 5*

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink may be attached to the top of the case, or the airflow inside the system must be increased.

#### 2.3.1.2.2 Theta-JB

Junction-to-board thermal resistance ($\theta_{JB}$) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from the junction to the board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

#### 2.3.1.2.3 Theta-JC

Junction-to-case thermal resistance ($\theta_{JC}$) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable to packages used with external heat sinks. Constant temperature is applied to the surface, which acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

### 2.3.1.3 ESD Performance

See *RT0001: Microsemi Corporation - SoC Products Reliability Report* for information about ESD.

***Table 22 •*** **Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---|---|---|---|---|
| LPDDR | | | 200 | MHz |
| HSTL1.5 V | | | 200 | MHz |
| SSTL 2.5 V | 255 | 350 | 200 | MHz |
| SSTL 1.8 V | | | 334 | MHz |
| SSTL 1.5 V | | | 334 | MHz |

***Table 23 •*** **Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | Unit |
|---|---|---|---|
| LVPECL (input only) | 450 | | MHz |
| LVDS 3.3 V | 267.5 | | MHz |
| LVDS 2.5 V | 267.5 | 350 | MHz |
| RSDS | 260 | 350 | MHz |
| BLVDS | 250 | | MHz |
| MLVDS | 250 | | MHz |
| Mini-LVDS | 260 | 350 | MHz |

### 2.3.5.7 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs that are in compliance with the JEDEC specification JESD8-5A.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 38 •*** **LVCMOS 2.5 V DC Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

***Table 39 •*** **LVCMOS 2.5 V DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high (for MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 1.7 | 2.625 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 1.7 | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.7 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 40 •*** **LVCMOS 2.5 V DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$[1] | $V_{DDI}$ – 0.4 | – | V |
| DC output logic low | $V_{OL}$[2] | | 0.4 | V |

1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

***Table 41 •*** **LVCMOS 2.5 V AC Minimum and Maximum Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 400 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 410 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 420 | Mbps | AC loading: 17 pF load, maximum drive/slew |

***Table 42 •*** **LVCMOS 2.5 V AC Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | Rodt_cal | 75, 60, 50, 33, 25, 20 | Ω |

***Table 57 •*** **LVCMOS 1.8 V Transmitter Characteristics for DDRIO I/O Bank with Fixed Code (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2 mA | Slow | 4.234 | 4.981 | 3.646 | 4.29 | 4.245 | 4.995 | 4.908 | 5.774 | 4.434 | 5.216 | ns |
| | Medium | 3.824 | 4.498 | 3.282 | 3.861 | 3.834 | 4.511 | 4.625 | 5.441 | 4.116 | 4.843 | ns |
| | Medium fast | 3.627 | 4.267 | 3.111 | 3.66 | 3.637 | 4.279 | 4.481 | 5.272 | 3.984 | 4.687 | ns |
| | Fast | 3.605 | 4.241 | 3.097 | 3.644 | 3.615 | 4.253 | 4.472 | 5.262 | 3.973 | 4.674 | ns |
| 4 mA | Slow | 3.923 | 4.615 | 3.314 | 3.9 | 3.918 | 4.61 | 5.403 | 6.356 | 4.894 | 5.757 | ns |
| | Medium | 3.518 | 4.138 | 2.961 | 3.484 | 3.515 | 4.135 | 5.121 | 6.025 | 4.561 | 5.366 | ns |
| | Medium fast | 3.321 | 3.907 | 2.783 | 3.275 | 3.317 | 3.903 | 4.966 | 5.843 | 4.426 | 5.206 | ns |
| | Fast | 3.301 | 3.883 | 2.77 | 3.259 | 3.296 | 3.878 | 4.957 | 5.831 | 4.417 | 5.196 | ns |
| 6 mA | Slow | 3.71 | 4.364 | 3.104 | 3.652 | 3.702 | 4.355 | 5.62 | 6.612 | 5.08 | 5.977 | ns |
| | Medium | 3.333 | 3.921 | 2.779 | 3.27 | 3.325 | 3.913 | 5.346 | 6.289 | 4.777 | 5.62 | ns |
| | Medium fast | 3.155 | 3.712 | 2.62 | 3.083 | 3.146 | 3.702 | 5.21 | 6.13 | 4.657 | 5.479 | ns |
| | Fast | 3.134 | 3.688 | 2.608 | 3.068 | 3.125 | 3.677 | 5.202 | 6.12 | 4.648 | 5.468 | ns |
| 8 mA | Slow | 3.619 | 4.258 | 3.007 | 3.538 | 3.607 | 4.244 | 5.815 | 6.841 | 5.249 | 6.175 | ns |
| | Medium | 3.246 | 3.819 | 2.686 | 3.16 | 3.236 | 3.807 | 5.542 | 6.52 | 4.936 | 5.807 | ns |
| | Medium fast | 3.066 | 3.607 | 2.525 | 2.971 | 3.054 | 3.593 | 5.405 | 6.359 | 4.811 | 5.66 | ns |
| | Fast | 3.046 | 3.584 | 2.513 | 2.957 | 3.034 | 3.57 | 5.401 | 6.353 | 4.803 | 5.651 | ns |
| 10 mA | Slow | 3.498 | 4.115 | 2.878 | 3.386 | 3.481 | 4.096 | 6.046 | 7.113 | 5.444 | 6.404 | ns |
| | Medium | 3.138 | 3.692 | 2.569 | 3.023 | 3.126 | 3.678 | 5.782 | 6.803 | 5.129 | 6.034 | ns |
| | Medium fast | 2.966 | 3.489 | 2.414 | 2.841 | 2.951 | 3.472 | 5.666 | 6.665 | 5.013 | 5.897 | ns |
| | Fast | 2.945 | 3.464 | 2.401 | 2.826 | 2.93 | 3.448 | 5.659 | 6.658 | 5.003 | 5.886 | ns |
| 12 mA | Slow | 3.417 | 4.02 | 2.807 | 3.303 | 3.401 | 4.002 | 6.083 | 7.156 | 5.464 | 6.428 | ns |
| | Medium | 3.076 | 3.618 | 2.519 | 2.964 | 3.063 | 3.604 | 5.828 | 6.856 | 5.176 | 6.089 | ns |
| | Medium fast | 2.913 | 3.427 | 2.376 | 2.795 | 2.898 | 3.41 | 5.725 | 6.736 | 5.072 | 5.966 | ns |
| | Fast | 2.894 | 3.405 | 2.362 | 2.78 | 2.879 | 3.388 | 5.715 | 6.724 | 5.064 | 5.957 | ns |
| 16 mA | Slow | 3.366 | 3.96 | 2.751 | 3.237 | 3.348 | 3.939 | 6.226 | 7.324 | 5.576 | 6.56 | ns |
| | Medium | 3.03 | 3.565 | 2.47 | 2.906 | 3.017 | 3.55 | 5.981 | 7.036 | 5.282 | 6.214 | ns |
| | Medium fast | 2.87 | 3.377 | 2.328 | 2.739 | 2.854 | 3.358 | 5.895 | 6.935 | 5.18 | 6.094 | ns |
| | Fast | 2.853 | 3.357 | 2.314 | 2.723 | 2.837 | 3.338 | 5.889 | 6.929 | 5.177 | 6.09 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 100 •*** **HSTL AC Test Parameter Specification**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.75 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for HSTL15 Class I ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Reference resistance for data test path for HSTL15 Class II ($T_{DP}$) | RTT_TEST | 25 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

**AC Switching Characteristics**

Worst-case commercial conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, worst-case $V_{DDI}$.

***Table 101 •*** **HSTL Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)**

| | | $T_{PY}$ | | |
|---|---|---|---|---|
| | **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| Pseudo differential | None | 1.605 | 1.888 | ns |
| | 47.8 | 1.614 | 1.898 | ns |
| True differential | None | 1.622 | 1.909 | ns |
| | 47.8 | 1.628 | 1.916 | ns |

***Table 102 •*** **HSTL Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| **HSTL Class I** | | | | | | | | | | | |
| Single-ended | 2.6 | 3.059 | 2.514 | 2.958 | 2.514 | 2.958 | 2.431 | 2.86 | 2.431 | 2.86 | ns |
| Differential | 2.621 | 3.083 | 2.648 | 3.115 | 2.647 | 3.113 | 2.925 | 3.442 | 2.923 | 3.44 | ns |
| **HSTL Class II** | | | | | | | | | | | |
| Single-ended | 2.511 | 2.954 | 2.488 | 2.927 | 2.49 | 2.93 | 2.409 | 2.833 | 2.411 | 2.836 | ns |
| Differential | 2.528 | 2.974 | 2.552 | 3.003 | 2.551 | 3.001 | 2.897 | 3.409 | 2.896 | 3.408 | ns |

### 2.3.6.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

**Table 156 • LPDDR-LVCMOS 1.8 V AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.9 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

**Table 157 • LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification for DDRIO Bank**

| Output Drive Selection | $V_{OH}$ (V) Min | $V_{OL}$ (V) Max | $I_{OH}$ (at $V_{OH}$) mA | $I_{OL}$ (at $V_{OL}$) mA |
|---|---|---|---|---|
| 2 mA | $V_{DDI}$ – 0.45 | 0.45 | 2 | 2 |
| 4 mA | $V_{DDI}$ – 0.45 | 0.45 | 4 | 4 |
| 6 mA | $V_{DDI}$ – 0.45 | 0.45 | 6 | 6 |
| 8 mA | $V_{DDI}$ – 0.45 | 0.45 | 8 | 8 |
| 10 mA | $V_{DDI}$ – 0.45 | 0.45 | 10 | 10 |
| 12 mA | $V_{DDI}$ – 0.45 | 0.45 | 12 | 12 |
| 16 mA[1] | $V_{DDI}$ – 0.45 | 0.45 | 16 | 16 |

1. 16 mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance.

**Table 158 • LPDDR-LVCMOS 1.8V AC Switching Characteristics for Receiver (for DDRIO I/O Bank with Fixed Code - Input Buffers)**

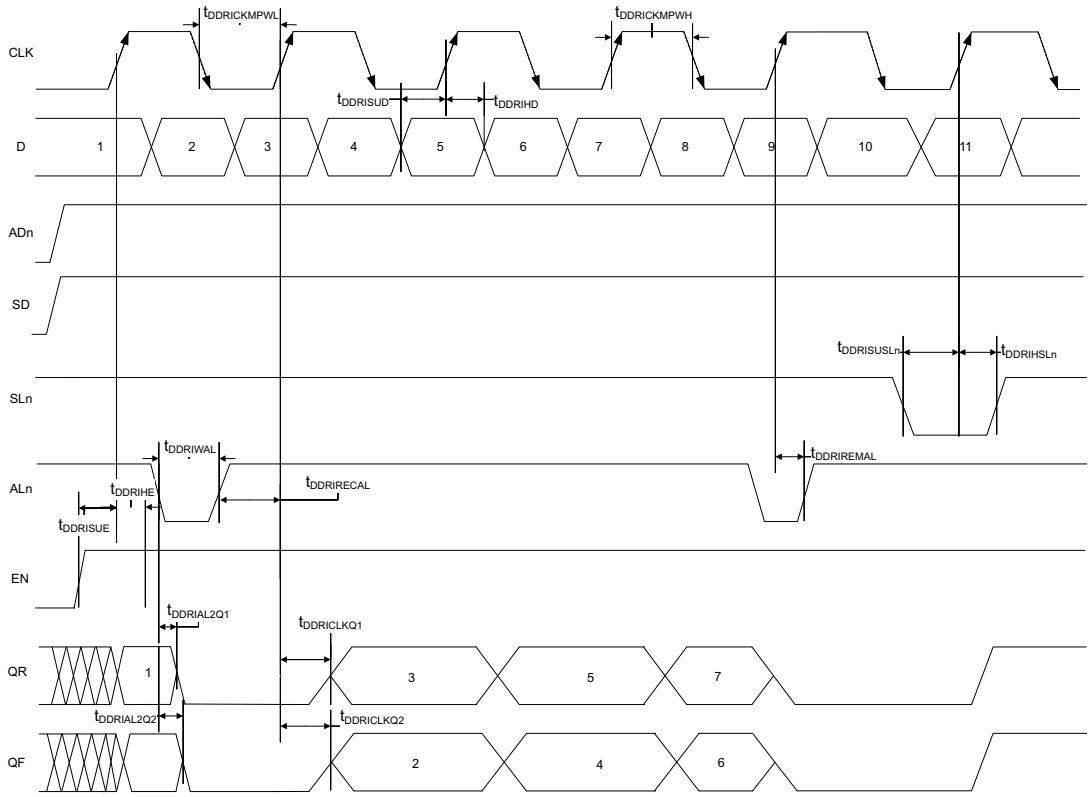
| ODT (On Die Termination) | –1 | –Std | –1 | –Std | Unit |
|---|---|---|---|---|---|
| None | 1.968 | 2.315 | 2.099 | 2.47 | ns |

**Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2 mA | slow | 4.234 | 4.981 | 3.646 | 4.29 | 4.245 | 4.995 | 4.908 | 5.774 | 4.434 | 5.216 | ns |
| | medium | 3.824 | 4.498 | 3.282 | 3.861 | 3.834 | 4.511 | 4.625 | 5.441 | 4.116 | 4.843 | ns |
| | medium_fast | 3.627 | 4.267 | 3.111 | 3.66 | 3.637 | 4.279 | 4.481 | 5.272 | 3.984 | 4.687 | ns |
| | fast | 3.605 | 4.241 | 3.097 | 3.644 | 3.615 | 4.253 | 4.472 | 5.262 | 3.973 | 4.674 | ns |
| 4 mA | slow | 3.923 | 4.615 | 3.314 | 3.9 | 3.918 | 4.61 | 5.403 | 6.356 | 4.894 | 5.757 | ns |
| | medium | 3.518 | 4.138 | 2.961 | 3.484 | 3.515 | 4.135 | 5.121 | 6.025 | 4.561 | 5.366 | ns |
| | medium_fast | 3.321 | 3.907 | 2.783 | 3.275 | 3.317 | 3.903 | 4.966 | 5.843 | 4.426 | 5.206 | ns |
| | fast | 3.301 | 3.883 | 2.77 | 3.259 | 3.296 | 3.878 | 4.957 | 5.831 | 4.417 | 5.196 | ns |
| 6 mA | slow | 3.71 | 4.364 | 3.104 | 3.652 | 3.702 | 4.355 | 5.62 | 6.612 | 5.08 | 5.977 | ns |
| | medium | 3.333 | 3.921 | 2.779 | 3.27 | 3.325 | 3.913 | 5.346 | 6.289 | 4.777 | 5.62 | ns |
| | medium_fast | 3.155 | 3.712 | 2.62 | 3.083 | 3.146 | 3.702 | 5.21 | 6.13 | 4.657 | 5.479 | ns |
| | fast | 3.134 | 3.688 | 2.608 | 3.068 | 3.125 | 3.677 | 5.202 | 6.12 | 4.648 | 5.468 | ns |
| 8 mA | slow | 3.619 | 4.258 | 3.007 | 3.538 | 3.607 | 4.244 | 5.815 | 6.841 | 5.249 | 6.175 | ns |

### 2.3.9.2 Input DDR Timing Diagram

***Figure 11 •*** **Input DDR Timing Diagram**




### 2.3.9.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 221 •*** **Input DDR Propagation Delays**

| Symbol | Description | Measuring Nodes (from, to) | –1 | –Std | Unit |
|---|---|---|---|---|---|
| $T_{DDRICLKQ1}$ | Clock-to-Out Out_QR for input DDR | B, C | 0.16 | 0.188 | ns |
| $T_{DDRICLKQ2}$ | Clock-to-Out Out_QF for input DDR | B, D | 0.166 | 0.195 | ns |
| $T_{DDRISUD}$ | Data setup for input DDR | A, B | 0.357 | 0.421 | ns |
| $T_{DDRIHD}$ | Data hold for input DDR | A, B | 0 | 0 | ns |
| $T_{DDRISUE}$ | Enable setup for input DDR | E, B | 0.46 | 0.542 | ns |
| $T_{DDRIHE}$ | Enable hold for input DDR | E, B | 0 | 0 | ns |
| $T_{DDRISUSLN}$ | Synchronous load setup for input DDR | G, B | 0.46 | 0.542 | ns |
| $T_{DDRIHSLN}$ | Synchronous load hold for input DDR | G, B | 0 | 0 | ns |
| $T_{DDRIAL2Q1}$ | Asynchronous load-to-out QR for input DDR | F, C | 0.587 | 0.69 | ns |
| $T_{DDRIAL2Q2}$ | Asynchronous load-to-out QF for input DDR | F, D | 0.541 | 0.636 | ns |
| $T_{DDRIREMAL}$ | Asynchronous load removal time for input DDR | F, B | 0 | 0 | ns |
| $T_{DDRIRECAL}$ | Asynchronous load recovery time for input DDR | F, B | 0.074 | 0.087 | ns |

***Table 231 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18 *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.529 | | 1.799 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.449 | | 0.528 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.167 | | 0.197 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | – | 1.506 | – | 1.772 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.39 | | 0.458 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.242 | | 0.285 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 2K × 9 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 232 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.334 | | 0.393 | ns |
| Read access time without pipeline register | | | 2.273 | | 2.674 | ns |
| Access time with feed-through write timing | | | 1.529 | | 1.799 | ns |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 16K × 1 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 235 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.32 | | 0.377 | ns |
| Read access time without pipeline register | | | 2.269 | | 2.669 | ns |
| Access time with feed-through write timing | | | 1.51 | | 1.777 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.626 | | 0.737 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.322 | | 0.378 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.51 | | 1.777 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.53 | | 0.624 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.547 | | 1.82 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.454 | | 0.534 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

***Table 241 •*** **µSRAM (RAM256x4) in 256 × 4 Mode *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Write address hold time | $T_{ADDRCHD}$ | 0.245 | | 0.288 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.03 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 512 × 2 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 242 •*** **µSRAM (RAM512x2) in 512 × 2 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.27 | | 0.31 | ns |
| Read access time without pipeline register | | | 1.76 | | 2.08 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.96 | | 2.306 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.137 | | 0.161 | | ns |
| Read address hold time in asynchronous mode | | –0.58 | | –0.68 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.77 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.14 | | 2.52 | ns |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.02 | | –0.03 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.83 | | 0.98 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |

***Table 245 •*** **JTAG Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 137536 | 39 | 4 | Sec |
| 010 | 274816 | 78 | 9 | Sec |
| 025 | 274816 | 78 | 9 | Sec |
| 050 | 278528 | 84 | 8 | Sec |
| 060 | 268480 | 76 | 8 | Sec |
| 090 | 544496 | 154 | 15 | Sec |
| 150 | 544496 | 155 | 15 | Sec |

***Table 246 •*** **JTAG Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Program | Verify | Unit |
|---|---|---|---|---|
| 005 | 439296 | 59 | 11 | Sec |
| 010 | 842688 | 107 | 20 | Sec |
| 025 | 1497408 | 120 | 35 | Sec |
| 050 | 2695168 | 162 | 59 | Sec |
| 060 | 2686464 | 158 | 70 | Sec |
| 090 | 4190208 | 266 | 147 | Sec |
| 150 | 6682768 | 316 | 231 | Sec |

***Table 247 •*** **2 Step IAP Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 302672 | 4 | 17 | 6 | Sec |
| 010 | 568784 | 7 | 23 | 12 | Sec |
| 025 | 1223504 | 14 | 33 | 23 | Sec |
| 050 | 2424832 | 29 | 52 | 40 | Sec |
| 060 | 2418896 | 39 | 61 | 50 | Sec |
| 090 | 3645968 | 60 | 84 | 73 | Sec |
| 150 | 6139184 | 100 | 132 | 120 | Sec |

**Table 254 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only) *(continued)***

| M2S/M2GL Device | Auto Programming 100 kHz | Auto Update 25 MHz | Programming Recovery 12.5 MHz | Unit |
|---|---|---|---|---|
| 150 | 161 | 161 | 161 | Sec |

**Table 255 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

| M2S/M2GL Device | Auto Programming 100 kHz | Auto Update 25 MHz | Programming Recovery 12.5 MHz | Unit |
|---|---|---|---|---|
| 005 | 47 | 27 | 28 | Sec |
| 010 | 77 | 35 | 35 | Sec |
| 025 | 150 | 42 | 41 | Sec |
| 050 | 33[1] | Not Supported | Not Supported | Sec |
| 060 | 291 | 83 | 82 | Sec |
| 090 | 427 | 109 | 108 | Sec |
| 150 | 708 | 157 | 160 | Sec |
| 005 | 41 | 48 | 49 | Sec |
| 010 | 86 | 87 | 87 | Sec |
| 025 | 87 | 85 | 86 | Sec |
| 050 | 85 | Not Supported | Not Supported | Sec |
| 060 | 78 | 86 | 86 | Sec |
| 090 | 154 | 162 | 162 | Sec |
| 150 | 161 | 161 | 161 | Sec |
| 005 | 87 | 67 | 66 | Sec |
| 010 | 161 | 113 | 113 | Sec |
| 025 | 229 | 120 | 121 | Sec |
| 050 | 112 | Not Supported | Not Supported | Sec |
| 060 | 368 | 161 | 158 | Sec |
| 090 | 582 | 261 | 260 | Sec |
| 150 | 867 | 309 | 310 | Sec |

1. Auto Programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

***Table 276 •*** **Cryptographic Block Characteristics *(continued)***

| Service | Conditions | Timing | Unit |
|---|---|---|---|
| SHA256 | 512 bits | 540 | kbps |
| | 1024 bits | 780 | kbps |
| | 2048 bits | 950 | kbps |
| | 24 kbits | 1140 | kbps |
| HMAC | 512 bytes | 820 | kbps |
| | 1024 bytes | 890 | kbps |
| | 2048 bytes | 930 | kbps |
| | 24 kbytes | 980 | kbps |
| KeyTree | | 1.8 | ms |
| Challenge-response | PUF = OFF | 25 | ms |
| | PUF = ON | 7 | ms |
| ECC point multiplication | | 590 | ms |
| ECC point addition | | 8 | ms |

1. Using cypher block chaining (CBC) mode.

## 2.3.19 Crystal Oscillator

The following table describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

***Table 277 •*** **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 20 | | MHz | |
| Accuracy | ACCXTAL | | | 0.0047 | % | 005, 010, 025, 050, 060, and 090 devices |
| | | | | 0.0058 | % | 150 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 200 | 300 | ps | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 200 | 300 | ps | 010, 025, 050, and 060 devices |
| | | | 250 | 410 | ps | 150 devices |
| | | | 250 | 550 | ps | 005 and 090 devices |
| Operating current | IDYNXTAL | | 1.5 | | mA | 010, 050, and 060 devices |
| | | | 1.65 | | mA | 005, 025, 090, and 150 devices |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |

***Table 277 •*** **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)** ***(continued)***

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 0.8 | ms | 005, 010, 025, and 050 devices |
| | | | | 1.0 | ms | 090 and 150 devices |

***Table 278 •*** **Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 2 | | MHz | |
| Accuracy | ACCXTAL | | | 0.00105 | % | 050 devices |
| | | | | 0.003 | % | 005, 010, 025, 090, and 150 devices |
| | | | | 0.004 | % | 060 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 1 | 5 | ns | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 1 | 5 | ns | |
| Operating current | IDYNXTAL | | 0.3 | | mA | |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 4.5 | ms | 010 and 050 devices |
| | | | | 5 | ms | 005 and 025 devices |
| | | | | 7 | ms | 090 and 150 devices |

***Table 279 •*** **Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 32 | | kHz | |
| Accuracy | ACCXTAL | | | 0.004 | % | 005, 010, 025, 050, 060, and 090 devices |
| | | | | 0.005 | % | 150 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 150 | 300 | ns | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 150 | 300 | ns | |
| Operating current | IDYNXTAL | | 0.044 | | mA | 010 and 050 devices |
| | | | 0.060 | | mA | 005, 025, 060, 090, and 150 devices |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 115 | ms | 005, 025, 050, 090, and 150 devices |
| | | | | 126 | ms | 010 devices |

## 2.3.20 On-Chip Oscillator

The following tables describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

***Table 280 •*** **Electrical Characteristics of the 50 MHz RC Oscillator**

| Parameter | Symbol | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|
| Operating frequency | F50RC | 50 | | MHz | |
| Accuracy | ACC50RC | 1 | 4 | % | 050 devices |
| | | 1 | 5 | % | 005, 025, and 060 devices |
| | | 1 | 6.3 | % | 090 devices |
| | | 1 | 7.1 | % | 010 and 150 devices |
| Output duty cycle | CYC50RC | 49–51 | 46.5–53.5 | % | |
| Output jitter (peak to peak) | JIT50RC | | | | Period Jitter |
| | | 200 | 300 | ps | 005, 010, 050, and 060 devices |
| | | 200 | 400 | ps | 150 devices |
| | | 300 | 500 | ps | 025 and 090 devices |
| | | | | | Cycle-to-Cycle Jitter |
| | | 200 | 300 | ps | 005 and 050 devices |
| | | 320 | 420 | ps | 010, 060, and 150 devices |
| | | 320 | 850 | ps | 025 and 090 devices |
| Operating current | IDYN50RC | 6.5 | | mA | |

***Table 281 •*** **Electrical Characteristics of the 1 MHz RC Oscillator**

| Parameter | Symbol | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|
| Operating frequency | F1RC | 1 | | MHz | |
| Accuracy | ACC1RC | 1 | 3 | % | 005, 010, 025, and 050 devices |
| | | 1 | 4.5 | % | 060, and 150 devices |
| | | 1 | 5.6 | % | 090 devices |
| Output duty cycle | CYC1RC | 49–51 | 46.5–53.5 | % | 005, 010, 025, 050, 090 and 150 devices |
| | | 49-51 | 46.0-54.0 | % | 060 devices |
| Output jitter (peak to peak) | JIT1RC | | | | Period Jitter |
| | | 10 | 20 | ns | 005, 010, 025, and 050 devices |
| | | 10 | 28 | ns | 060, 090 and 150 devices |
| | | | | | Cycle-to-Cycle Jitter |
| | | 10 | 20 | ns | 005, 010, and 050 devices |
| | | 10 | 35 | ns | 025, 060, and 150 devices |
| | | 10 | 45 | ns | 090 devices |
| Operating current | IDYN1RC | 0.1 | | mA | |
| Startup time | SU1RC | | 17 | µs | 050, 090, and 150 devices |
| | | | 18 | µs | 005, 010, and 025 devices |

## 2.3.24 Power-up to Functional Times

The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 288 •*** **Power-up to Functional Times for SmartFusion2**

| | | | | Maximum Power-up to Functional Time for SmartFusion2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **From** | **To** | **Description** | **005** | **010** | **025** | **050** | **060** | **090** | **150** |
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 647 | 500 | 531 | 483 | 474 | 524 | 647 |
| $T_{POR2MSSRST}$ | POWER_ON_RESET_N | MSS_RESET_N_M2F | Fabric to MSS | 644 | 497 | 528 | 480 | 468 | 518 | 641 |
| $T_{MSSRST2OUT}$ | MSS_RESET_N_M2F | Output available at I/O | MSS to output | 3.6 | 3.6 | 3.6 | 3.4 | 4.9 | 4.8 | 4.8 |
| $T_{VDD2OUT}$ | $V_{DD}$ | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 3096 | 2975 | 3012 | 2959 | 2869 | 2992 | 3225 |
| $T_{VDD2POR}$ | $V_{DD}$ | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 2476 | 2487 | 2496 | 2486 | 2406 | 2563 | 2602 |
| $T_{VDD2MSSRST}$ | $V_{DD}$ | MSS_RESET_N_M2F | $V_{DD}$ at its minimum threshold level to MSS | 3093 | 2972 | 3008 | 2956 | 2864 | 2987 | 3220 |
| $T_{VDD2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2500 | 2487 | 2509 | 2475 | 2507 | 2519 | 2617 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2504 | 2491 | 2510 | 2478 | 2517 | 2525 | 2620 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2479 | 2468 | 2493 | 2458 | 2486 | 2499 | 2595 |

**Note:** For more information about power-up times, see *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

The following table lists the SerDes reference clock AC specifications in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 299 •*** **SerDes Reference Clock AC Specifications**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Reference clock frequency | $F_{REFCLK}$ | 100 | 160 | MHz |
| Reference clock rise time | $T_{RISE}$ | 0.6 | 4 | V/ns |
| Reference clock fall time | $T_{FALL}$ | 0.6 | 4 | V/ns |
| Reference clock duty cycle | $T_{CYC}$ | 40 | 60 | % |
| Reference clock mismatch | $M_{MREFCLK}$ | –300 | 300 | ppm |
| Reference spread spectrum clock | SSCref | 0 | 5000 | ppm |

***Table 300 •*** **HCSL Minimum and Maximum DC Input Levels (Applicable to SerDes REFCLK Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | |
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |
| **HCSL DC Input Voltage Specification** | | | | | |
| DC Input voltage | $V_I$ | 0 | | 2.625 | V |
| **HCSL Differential Voltage Specification** | | | | | |
| Input common mode voltage | $V_{ICM}$ | 0.05 | | 2.4 | V |
| Input differential voltage | $V_{IDIFF}$ | 100 | | 1100 | mV |

***Table 301 •*** **HCSL Minimum and Maximum AC Switching Speeds (Applicable to SerDes REFCLK Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **HCSL AC Specifications** | | | | | |
| Maximum data rate (for MSIO I/O bank) | $F_{MAX}$ | | | 350 | Mbps |
| **HCSL Impedance Specifications** | | | | | |
| Termination resistance | Rt | | 100 | | Ω |

## 2.3.31 SmartFusion2 Specifications

### 2.3.31.1 MSS Clock Frequency

The following table lists the maximum frequency for MSS main clock in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 302 •*** **Maximum Frequency for MSS Main Clock**

| Symbol | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| M3_CLK | Maximum frequency for the MSS main clock | 166 | 142 | MHz |

***Table 310 •*** **SPI Characteristics for All Devices *(continued)***

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| SPI master configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 7.0 | | | ns | |
| sp7m | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) – 9.5 | | | ns | |
| sp8m | SPI_[0\|1]_DI setup time[2] | 15 | | | ns | |
| sp9m | SPI_[0\|1]_DI hold time[2] | –2.5 | | | ns | |
| SPI slave configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 16.0 | | | ns | |
| sp7s | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) - 3.5 | | | ns | |
| sp8s | SPI_[0\|1]_DI setup time[2] | 3 | | | ns | |
| sp9s | SPI_[0\|1]_DI hold time[2] | 2.5 | | | ns | |

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. For allowable pclk configurations, see the Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

***Figure 23 •*** **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**